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QUARTZ CRYSTAL OSCILLATOR CIRCUITS
DESIGN HANDBOOK


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LIST OF SYMBOLS

A	Voltage attenuation ratio of a network.
A_V	Voltage ratio of output and input signal voltage in crystal π network.
A'_V	A_V modified by presence of small capacitance in parallel with crystal unit.
A_{VC}	Voltage attenuation occurring across a series resonance crystal unit.
A_{V_t}	Voltage ratio of an impedance transforming network between amplifier output and crystal unit.
BV_{CEO}	Transistor collector-emitter breakdown voltage rating when the base is open-circuited.
BV_{CER}	Transistor collector-emitter breakdown voltage rating with the resistor R between base and emitter.
C_E	Emitter circuit decoupling capacitor.
C_M	Grounded cathode triode input capacitance due to feedback via C_{pg} .
C_K	Cathode decoupling capacitor.
C_L	Loading capacitance associated with crystal unit.
C_S	Capacitor in a crystal π network defined by Figure 1-17.
C_T	Capacitor in a crystal π network defined by Figure 1-17.
$C_{b'e}$	Defined in Section 3-13.
$C_{b'E}$	Equivalent of $C_{b'e}$ when using emitter degeneration.
$C_{cb'}$	Defined in Section 3-13.
C_{gk}	Tube grid-cathode capacitance.
$C_{in(p)}$	Parallel input capacitance of an amplifier.

LIST OF SYMBOLS (CONT)

C_l	Capacitor in a crystal π network defined by Figure 1-17.
C_o	Crystal unit shunt capacitance.
C_{ob}	Defined in Section 3-13.
$C_{o(p)}$	Amplifier parallel output capacitance.
$C_{(p)}$	Defined in Section 3-25.
C_{pg}	Tube grid-plate capacitance.
C_{pk}	Tube plate-cathode capacitance.
C_r	Capacitance from base to collector in transistor π equivalent circuit (Section 3-25).
C_1	Crystal unit motional arm equivalent capacitance. Also used for capacitor in capacitive divider impedance transformer.
C_2	Used for capacitor in capacitive divider.
$\frac{d\phi}{df}$	Rate of change of crystal unit phase angle as a function of frequency.
$\frac{d\phi}{dX_e}$	Used in crystal π network analysis as indicative of $\frac{d\phi}{df}$
Δb	Defined by Equation 3-26.
Δf	Incremental frequency change.
E	Power transfer efficiency of a network.
E_f	Heater voltage.
E_p	Tube DC plate voltage.
f_a	Crystal unit antiresonance frequency.
f'_a	Frequency of resonance of a crystal unit and a series or parallel loading capacitance.

LIST OF SYMBOLS (CONT)

f_m	Frequency of crystal unit minimum impedance.
f_n	Frequency of crystal unit maximum impedance.
f_p	Frequency at which the motional arm reactance equals that of C_o ($X_1 \gg R_1$).
f_r	Crystal unit resonance frequency.
f_s	Crystal unit motional arm resonance frequency.
f_T	Current gain-bandwidth product of a transistor.
f_V	Transistor amplifier voltage gain cut-off frequency.
f'_V	Extrinsic transconductance cut-off frequency.
f_α	Frequency at which h_{fe} is 3 DB down relative to α_o .
f_β	Frequency at which h_{fe} is 3 DB down relative to h_{FE} .
G_M	Defined in Section 3-23.
G_p	Amplifier power gain.
G'_p	Net power gain of oscillator loop.
G_V	Amplifier voltage gain.
G'_V	Actual amplifier voltage gain when limiting is occurring.
G_{VL}	Oscillator loop voltage gain.
G_{VO}	Transistor amplifier low frequency voltage gains.
G_{VR}	Net voltage gain of amplifier and crystal unit.
g_m	Mutual conductance of a vacuum tube. Defined for transistors in Section 3-13.
g'_m	Extrinsic transistor g_m (defined in Section 3-25).

LIST OF SYMBOLS (CONT)

$\left. \begin{array}{l} h_i \\ h_r \\ h_f \\ h_o \end{array} \right\}$	Low frequency transistor hybrid parameters. Second suffix refers to common electrode, e.g., h_{oe} denotes common emitter.
h_{FE}	Transistor common-emitter current gain at low frequencies.
$h_{FE \min}$	Minimum value of h_{FE} .
h_{fe}	Transistor common-emitter current gain.
h_{fb}	Transistor common-base current gain.
I_C	Transistor DC collector current.
I_E	Transistor DC emitter current.
I_p	Tube DC plate current.
K	Kilohms. Defined by Equation 7-6 for transistor series oscillators.
KC	Kilocycles per second.
K_A	Factor associated with crystal π network; equal to $\left(1 + \frac{R}{X_{CT}} \cdot \frac{R_{e \max}}{X_{Leff}} \right)$ and having a value of from 4 to 5.5.
k	Inductive coupling coefficient. Defined by Equation 6-7 for tube series oscillators.
$L(s)$	Transistor common-base series input inductance.
L_1	Crystal unit motional arm equivalent inductance.
M	Mutual inductance. Figure of Merit for crystal unit = X_{C_0}/R_1 .
MC	Megacycles per second.
MW	Milliwatts.

LIST OF SYMBOLS (CONT)

P_F	Picofarads.
PPM	Abbreviation for parts per million.
P_C	Crystal unit dissipation.
$P_{C\text{MAX}}$	Crystal unit dissipating rating.
$P_{C\text{ max}}$	Maximum crystal dissipation under specific operating conditions.
P_D	Transistor power dissipation.
$P_{D\text{ max}}$	Maximum permissible value of P_D at highest operating temperature.
P_{FB}	Oscillator feedback power.
P_L	Oscillator output power.
P_T	Amplifier total output power.
Q	Circuit magnification factor.
Q_s	Defined by Equation 1-28.
R	Resistor in crystal π network. Also used as a general term for a resistor.
R_D	Defined in Section 3-13.
R_E	Decoupled emitter resistor.
R_{FB}	Feedback network resistance reflected into the amplifier output circuit.
R_K	Cathode resistor.
R_L	Oscillator external load resistance reflected into the plate or collector circuits of the amplifier.
R_M	Grounded cathode triode input resistance due to feedback via C_{pg} .

LIST OF SYMBOLS (CONT)

R_T	Amplifier total load resistance.
$R_{T \min}$	Minimum value of R_T in basic Pierce circuit.
R_a	Crystal unit equivalent resistance at antiresonance.
$\left. \begin{matrix} R_{b1} \\ R_{b2} \end{matrix} \right\}$	Base biasing resistors.
$R_{b(p)}$	R_{b1} and R_{b2} in parallel.
$R_{b'e}$	Defined in Section 3-13.
$R_{b'E}$	Equivalent of $R_{b'e}$ when using emitter degeneration.
R_e	Crystal unit equivalent series resistance.
$R_{e \max}$	Maximum value of crystal unit equivalent series resistance when at series resonance with specified loading capacitance.
R_e'	Equivalent resistance of a crystal unit modified by a small parallel capacitance.
R_g	Grid leak resistor value.
R_i	Crystal unit terminating resistance at the amplifier input side of crystal unit.
$R_{in(p)}$	Amplifier parallel input resistance.
R_{in}''	Input resistance of $R_{b(p)}$ and $R_{in(p)}$ in parallel.
$R_{in(s)}$	Series input resistance of a grounded base transistor amplifier.
$R_{o(p)}$	Parallel output resistance of amplifier.
R_p	Plate resistance of a tube.
R_r	Resistance between base and collector in transistor π equivalent circuit (see Section 3-25).
R_r'	Part of R_r .

LIST OF SYMBOLS (CONT)

R_r''	Part of R_r (or $R_b'E$).
$R_{r \max}$	Maximum value of crystal unit resonance resistance.
R_π	Parallel input resistance of crystal π network as viewed across C_T .
$R_{\pi \min}$	Minimum value of R_π .
$R_{\pi \max}$	Maximum value of R_π .
R_1	Crystal unit motional arm equivalent resistance.
$R_{1 \max}$	Maximum value of R_1 .
r	Crystal unit capacitance ratio C_0/C_1 .
r'	Emitter ohmic resistance.
$r_{bb'}$	Defined in Section 3-13.
r_E	Unbypassed emitter degeneration resistance.
r_e	Defined in Section 3-13.
r_i	Effective value of R_i when transformed to series element in π network.
r_K	Tube cathode input resistance.
r_K'	R_K and r_K in parallel.
r_s	Load resistance of an impedance-transforming network.
r_ϵ	Defined in Section 3-13.
$\left. \begin{matrix} T_V \\ T_{V_o} \\ T_{V_i} \end{matrix} \right\}$	Voltage transformation ratio of an impedance transforming network.
T_r	Impedance transformation ratio of a network.

LIST OF SYMBOLS (CONT)

μ	Tube amplification factor.
V_{\max}	Maximum signal voltage allowed at the input terminal in series oscillator before crystal overdrive occurs.
V_G	Tube grid bias voltage.
V_p	Tube DC plate voltage.
V_{BG}	Base-to-ground DC voltage.
V_{CC}	Transistor circuit supply voltage.
V_{CE}	Transistor collector emitter DC voltage.
$V_{o\max}$	Maximum allowable signal voltage at the input of a crystal π network.
V_{π}	Signal voltage across C_T in crystal π network.
$V_{\pi A}$	Maximum value of V_{π} allowed by crystal dissipation.
X_1	Crystal unit motional arm reactance.
X'	Equivalent reactance of a crystal unit modified by a small parallel capacitance.
X_{C_0}	Crystal unit shunt capacitive reactance.
X_{C_1}	Reactance of crystal unit motional arm capacitance.
X_{C_E}	Reactance of C_E .
X_{C_L}	Reactance of crystal unit loading capacitance.
X_{C_M}	Reactance of C_M .
X_{C_S}	Reactance of C_S .
X_{C_T}	Reactance of C_T .
$X_{C_{b'E}}$	Reactance of $C_{b'E}$

LIST OF SYMBOLS (CONT)

$X_{C_{b'e}}$	Reactance of $C_{b'e}$.
$X_{C_{cb'}}$	Reactance of $C_{cb'}$.
X_{C_L}	Reactance of C_L .
$X_{C(p)}$	Reactance of $C(p)$.
X_{C_r}	Reactance of C_r .
X_e	Crystal unit equivalent reactance at f_a' · $X_e = X_{C_L}$.
X_K	Reactance of C_K .
X_{L_1}	Reactance of crystal unit motional arm inductance.
X_{Leff}	Equation 1-81. Defined for LC π -network in Section 4-2.
$X_{L(s)}$	Transistor common base series input inductive reactance.
Y, y	Admittance.
Y_M	Grounded cathode triode input admittance due to feedback via C_{pg} .
Y_f	Defined in Section 3-25.
Y_{in}	Defined in Section 3-25.
Z_{Tmin}	Total load impedance seen by amplifier in basic Pierce circuit.
α	Transistor common-base current gain.
α_0	Low frequency value of α .
ω	Angular frequency in radians per second.
ω_T	$= 2\pi f_T$.

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INTRODUCTION

In sinusoidal or semi-sinusoidal oscillators, the criteria governing operations are:

- (a) The loop power gain must be equal to 1.
- (b) The loop phase shift must be $0, 2\pi, 4\pi$, etc., radians.

That is, the power fed back to the input of the amplifier which maintains the oscillation because of its capability of providing power gain, must be such that the amplified output power is just sufficient to supply the oscillator output power, the circuit losses, and the amplifier input power. If this equality did not occur the feedback power would be either too large, causing the oscillation amplitude to grow, or too small, in which case the oscillation would decrease; the conditions of oscillation growth or decay being maintained until the unity loop gain condition is fulfilled.

This behavior also defines a further circuit requirement. Since at the commencement of oscillation the oscillation amplitude must grow from zero to a finite value and then stabilize, the circuit must initially provide a loop gain in excess of 1 to allow this buildup to occur. This loop gain must then decrease to unity at the desired oscillator power output level, thereby stabilizing the oscillation amplitude. This action is usually obtained by relying on the non-linear characteristics of over-driven amplifiers. The power gain of amplifiers tends to decrease with increasing signal level, thereby providing the necessary loop gain reduction as the oscillation grows. Condition (a) can therefore be more accurately stated as:

- (a') Under small signal conditions, the loop gain must be greater than unity.

These conditions can be defined in terms of Figure 1.

All sinusoidal electronic oscillators can be considered as consisting of a power amplifier and a network which selects a portion of the amplifier output power and returns it to the amplifier input.

Figure 1 (a) shows a generalized oscillator circuit of this form, and Figure 1 (b) shows the same circuit with the feedback connection broken at point A. In the latter circuit an additional load Z'_F , equal to the input impedance of the feedback network Z_F when terminated by the amplifier input impedance, is

placed across the amplifier output. (The prime sign is used to avoid ambiguity in the following discussion.) The amplifier is therefore terminated in identical loads in both (a) and (b) of Figure 1.

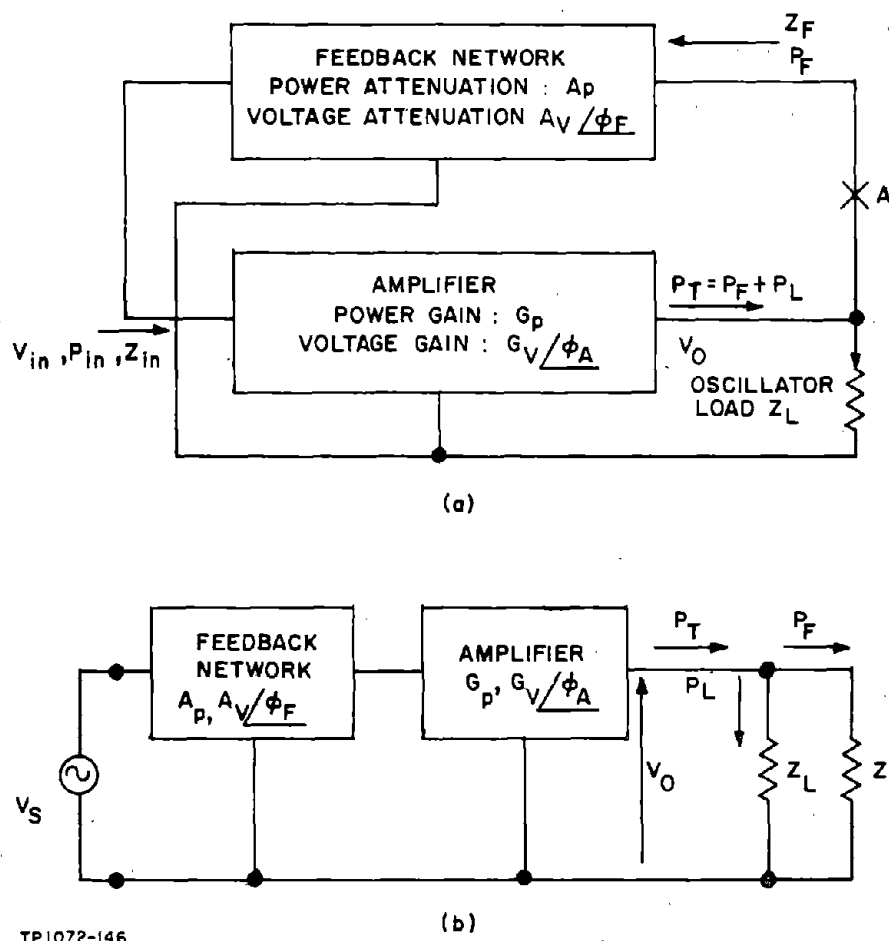


Figure 1. Generalized Oscillator Circuit

Applying a signal at the input of the feedback network in Figure 1 (b) will result in signal power being fed to Z'_F . The loop power gain is then defined as the ratio of the power into Z'_F to that applied at the feedback network input. This can also be stated in terms of voltage. In this case, since Z'_F and Z_F are identical, the loop power gain is equal to $(V_O/V_S)^2$. Similarly, the loop phase angle is defined as the phase shift of V_O relative to that of V_S . In order for oscillation to build up (when the input of the feedback network is reconnected to the amplifier output), V_O should be somewhat greater in amplitude than V_S , assuming linear operation, and their phase angles must be identical. If these conditions cannot be simultaneously satisfied for some input signal frequency in the circuit of Figure 1 (b), the network is incapable of oscillation.

There is a possible exception to the conditions given for an oscillator, which should be mentioned. Feedback circuits can be constructed which simultaneously have a loop gain greater than 1 and zero loop phase angle, and which do not oscillate. These circuits are then said to be conditionally stable. However, circuits having these characteristics are far more complex than those of the simple oscillator circuits considered here. A definite design effort is required to achieve these characteristics, and it is unlikely that conditionally stable operation will be achieved accidentally in an oscillator circuit. The condition as stated in (a') is therefore adequate.

The frequency at which oscillation occurs is entirely dependent on the zero loop phase angle condition, and the stability of the frequency of oscillation is related to the stability of the individual phase shifts in the oscillator component networks. Any net phase change within the oscillator loop due to ambient condition changes, component aging, oscillator power source variations, etc., will result in an oscillator frequency change which will depend on the rate of change of the loop phase angle with frequency and the extent of the phase change. When, as is normally the case, an oscillator output frequency essentially independent of external variables is required, there are two possible approaches:

- (a) To compensate the various networks of the oscillator to either produce mutual cancellation of phase changes due to external disturbances or, alternatively, to make each network phase insensitive to external disturbances.
- (b) To include a network in the oscillator circuit which has a high rate of change of phase angle with frequency and is itself relatively insensitive to external disturbance and which can, therefore, cancel the net phase change of the other oscillator networks with only a small change in oscillator frequency.

The first method (a) is idealistic if a wide operating temperature range is contemplated, and the second (b) is a more practical approach, particularly if combined with the concept expressed in (a) of minimizing the net phase change of the remainder of the oscillator circuit.

A familiar network which can have a high rate of change of phase angle with frequency and one that has been used from the inception of electronics for frequency control is the LC tuned circuit. Another component having analogous but superior characteristics, both in respect to rate of change of phase angle with frequency and phase angle insensitivity to external disturbance, is the quartz crystal resonator. It is therefore ideally suited to act as the frequency controlling element in stable frequency oscillators and as such finds wide application. However, its good characteristics can easily be degraded if care is not

taken in its use, since, like all devices, its good characteristics can only be applied advantageously under certain conditions of operation.

It is the purpose of this handbook to define these conditions of usage so that misapplication will be avoided and to detail acceptable oscillator design methods which will ensure this. The design methods developed are all based on the loop gain and phase concept used in the preceding discussion. Practical oscillator design examples are included together with evaluation data obtained from the oscillators constructed from these designs.

The emphasis has been placed on medium stability, wide temperature range oscillators having a frequency stability approaching that of the crystal unit, since these are the most widely used. However, the design approach for temperature-controlled crystal oscillators frequently used when better frequency stability is required is essentially the same, and the design concepts used in this handbook are equally valid for these circuits.

However, the present trend in military equipments is away from the use of temperature control in all but the most demanding requirements. The relatively high oven or temperature chamber power dissipation and physical bulk are not in keeping with the emphasis on compactness and minimal power consumption, and another approach developed extensively in recent years is now becoming widely used. This is the crystal oscillator which employs a temperature sensing network to partially correct for the effects of temperature on the crystal unit resonance frequency, thereby reducing the oscillator frequency instability with temperature. Using this approach, long-term frequency stabilities which hold over a 100°C temperature range of 3×10^{-7} have been attained, and the indications are that 1×10^{-7} or better is feasible. Here again, the handbook contents should prove useful insofar as the basic oscillator design is concerned. However, the crystal unit compensation techniques are the major part of this type of oscillator design, and the referenced sources should be consulted for details.

The criteria used in selecting the oscillator circuits for discussion have been primarily those of circuit simplicity and cost minimization. This in general has dictated the selection of circuits using only one tube or transistor wherever possible. This approach also has another desirable facet in that, in general, a more constant loop gain is obtained using only one active device under conditions of environmental stress and with active device interchange. This in turn tends to improve both oscillator frequency and amplitude stabilities.

Design Handbook Contents

The handbook is divided into ten sections. Section 1 presents a discussion of the electrical behavior of crystal units, methods of measurement,

and desirable methods of electrically terminating the crystal unit in order to optimize its oscillator frequency stabilizing properties. Section 2 considers the implications of the crystal unit terminating conditions determined in Section 1 on the remainder of the oscillator circuit. From these considerations it is then possible to construct a generalized block diagram of the oscillator loop and to define the loop gain in terms of the characteristics of the individual blocks. This process in turn defines the important characteristics of the individual oscillator blocks and, in particular, those of the amplifier and the impedance transforming networks. Section 3 describes the behavior of transistor and vacuum tube amplifiers in the frequency range of 1 KC to 200 MC and, where possible, presents design equations for amplifier gain, input impedance, and output impedance. Where this is not possible, experimental background information showing the influence of bias levels, etc., is given, together with a description of test methods that can be employed to measure the amplifier characteristics.

Section 4 presents analyses of several types of impedance transforming networks that are useful in oscillator design, together with design equations developed from the analyses.

Section 5 presents general information concerning the mating of the various oscillator component parts, oscillator frequency tolerance, frequency dependence of components, circuit layout, specification of oscillator requirements, the design process involved in arriving at an oscillator design, etc.

Sections 6, 7, 8, and 9 are the oscillator design sections where the relative characteristics of the amplifier and crystal unit are compared and a suitable design approach formulated. Sections 6 and 7 deal with tube and transistor series type oscillators, respectively, and Sections 8 and 9 with transistor and tube anti-resonance oscillators, respectively. These sections are further sub-divided for specific frequency ranges. Specimen oscillator design calculations are presented to illustrate the design procedures advocated, and in the majority of cases, experimental evaluation data are given for oscillators constructed from these designs. These evaluation results indicate the effect of ambient temperature, power supply, and oscillator load changes on the oscillator performance, and in many cases the effects of crystal unit and amplifying device changes are also given.

Section 10 contains a bibliography of reference sources.

As for utilization of this handbook, Sections 1, 3, and 4 should be used for reference purposes. The user should first refer to Sections 2 and 5 if unacquainted with the design approach used, and then turn to the applicable Section for the frequency range concerned. References contained therein will then show which parts of Sections 1, 3, and 4 are pertinent to the design.

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SECTION 1 QUARTZ CRYSTAL CHARACTERISTICS

1-1. GENERAL

A quartz crystal resonator is an electromechanical transducer having piezoelectric properties. The application of an electrical potential to the quartz crystal produces a mechanical stress within the crystal structure similar to that obtained by the application of mechanical force. Conversely, the application of mechanical force to the crystal creates a potential difference across the crystal structure. Therefore, by suitably connecting two or more electrodes to a quartz crystal, it can be made to vibrate by applying an alternating voltage to these electrodes.

If the output of the alternating voltage source is held constant and the frequency continuously varied, certain frequencies will be found at which the amplitude of the mechanical vibration becomes a maximum. These are the frequencies at which the quartz crystal goes into mechanical resonance. Because of the electromechanical coupling in the crystal, this mechanical motion of the crystal is reflected to the input terminals. And at frequencies in the immediate vicinity of the mechanical resonant frequencies, the electrical impedance presented at the input terminals exhibits characteristics similar to those of an electrical tuned circuit. Viewed as an electrical network, the important properties of the quartz crystal are:

- (a) The high effective Q ; that is, the high ratio of energy stored in the crystal relative to the energy dissipated in storing that energy.
- (b) The excellent stability of the electrical parameters of the quartz crystal when subjected to environmental changes.
- (c) The wide range of frequencies over which quartz crystals can be made to resonate.

These three properties account for their wide use in stable oscillator designs.

The simple equivalent electrical circuit of a quartz crystal resonator at frequencies close to that of the mechanical resonance is shown in Figure 1-1. L_1 and C_1 are primarily dependent on the mass and compliance of the quartz. R_1 which represents the losses of the circuit is, in the common type of crystal unit discussed here, mainly attributable to damping resulting from the electrodes, the crystal mounting structure, and the internal friction.

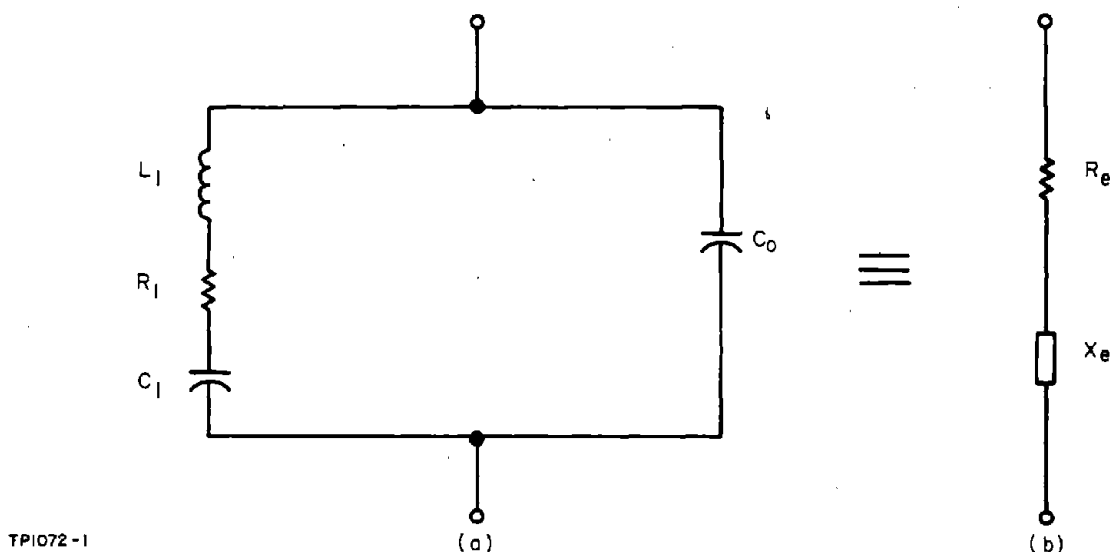


Figure 1-1. Equivalent Electrical Circuit of a Crystal

These are the motional impedance elements of the crystal, so called because they are the effective electrical equivalents of the vibratory motion of the crystal. C_0 is an actual electrical capacitance due to the electrodes on the quartz and to the stray capacitance in the mechanical assembly. Typical values of the parameters for 200-KC, 2-MC, and 30-MC crystals are shown in Table 1-1.

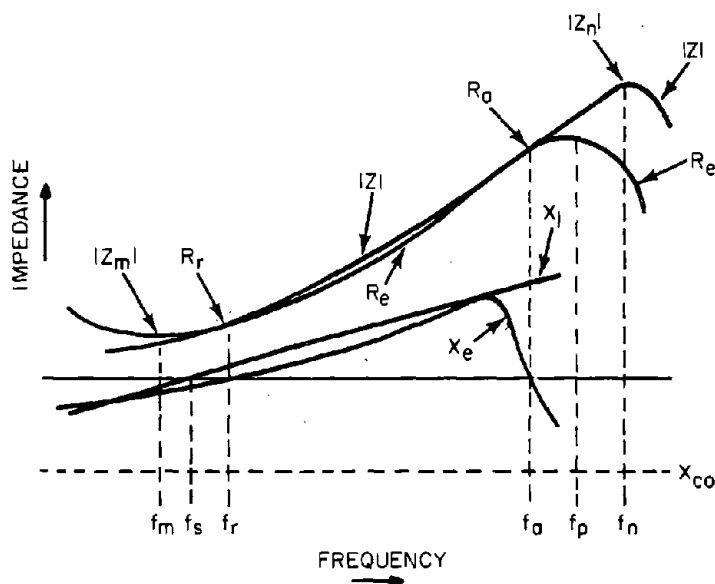
TABLE 1-1. TYPICAL CRYSTAL PARAMETER VALUES

Parameters	200 KC	2 MC	30 MC
R_1	2 K	100 ohms	20 ohms
L_1	27 H	520 MH	11 MH
C_1	0.024 PF	0.012 PF	0.0026 PF
C_0	9 PF	4 PF	6 PF
Q	18×10^3	54×10^3	10^5

At very high frequencies, the parasitic reactive elements of the mechanical mount start to influence the overall characteristics of the device. The input lead inductance then has a noticeable effect, and the shunt capacitance C_0 can no longer be regarded as a lumped element. However, from the oscillator design viewpoint, these effects while noticeable, do not invalidate the simple equivalent circuit of Figure 1-1 and are only mentioned to show that these effects occur.

This equivalent circuit is only representative of the electrical characteristics of a crystal over a limited frequency range. Every mechanical structure has several modes of resonance. A simple bar, for example, has flexural, torsional, shear, and extensional modes of oscillation in each of three axes. Furthermore, mechanical resonance can be excited at the overtones of each of these basic modes. The manufacturer shapes, proportions, and clamps the crystal so as to make one of these mechanical resonances predominant, while suppressing all others that may occur at frequencies immediately adjacent to this desired one. If, as is normally the case, sufficient suppression of the undesired resonances is achieved, the circuit of Figure 1-1 is a valid electrical equivalent of the electromechanical characteristics of the crystal in the frequency band immediately around the predominant mechanical resonance frequency and, with a change of component values, at overtone frequencies.

With this restriction, the behavior of the quartz crystal can be discussed in terms of the electrical equivalent circuit of Figure 1-1 (a), where L_1 , C_1 , R_1 , and C_0 are essentially independent of frequency. This circuit can be considered as a series combination of an equivalent resistance R_e and reactance X_e , as shown in Figure 1-1 (b). The values of R_e and X_e are frequency dependent and vary in the general manner indicated in Figure 1-2 as functions of frequency. The various symbols are defined in Table 1-2.



TP1072-2

Figure 1-2. Impedance $|Z|$, Resistance R_e , Reactance X_e , and Series Arm Reactance X_l of a Crystal as a Function of Frequency

TABLE 1-2. DEFINITIONS OF SYMBOLS IN FIGURE 1-2

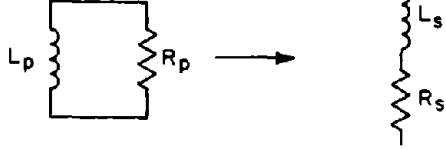
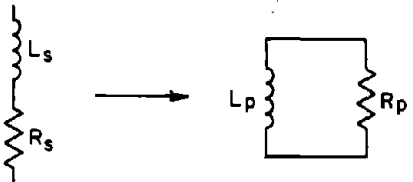
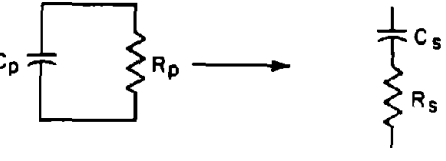
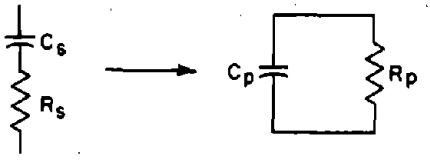
Symbol	Definition
r	Capacitance ratio = $\frac{C_0}{C_1}$
f_m	Frequency of minimum impedance
f_s	Motional arm resonance frequency = $\frac{1}{2\pi \sqrt{L_1 C_1}}$
f_r	Resonance frequency ($X_e = 0$)
f_a	Antiresonance frequency ($X_e = 0$)
f_p	Parallel resonance frequency = $\frac{1}{2\pi} \left[\frac{1}{L_1 C_1} \left(1 + \frac{1}{r}\right) \right]^{1/2}$
f_n	Frequency of maximum impedance
R_r	Resonance resistance ($X_e = 0$)
R_a	Antiresonance resistance ($X_e = 0$)
Z_m	Impedance at f_m (minimum crystal impedance)
Z_n	Impedance at f_n (maximum crystal impedance)

Figure 1-1 should only be regarded as of a qualitative nature. $|Z_n|$ and R_a are in practice many orders of magnitude larger than $|Z_m|$ and R_r , and the frequency spacing of f_a relative to f_r is a thousand or more times the spacings of f_m and f_r to f_s , and f_a and f_n to f_p .

Figure 1-2 and Table 1-2 are reproduced from the I.R.E. Standards on Piezoelectric Crystals "The Piezoelectric Vibrator: Definitions and Methods of Measurement, 1957" (I.R.E. Proc., March 1957).

Interpreting the points of interest on the curves of Figure 1-2 from left to right, f_s is the frequency at which the motional arm is series resonant. At this frequency the crystal appears at its terminals as a combination of R_1 in parallel with C_0 . Over almost the entire frequency range X_{C_0} the reactance of C_0 is much greater than R_1 , and consequently the crystal unit phase angle at f_s is small. Only at the very highest frequencies (above 100 MC) does the phase angle become appreciable. At a slightly higher frequency f_r , the motional arm reactance X_1 is inductive but small compared to R_1 and of such a value that its equivalent inductance when transformed to a parallel element (see Table 1-3 (b)) resonates with C_0 . The formulae illustrating this effect are:

TABLE 1-3. TABLE OF IMPEDANCE TRANSFORMATIONS

(a) 	$R_s = R_p \left[\frac{1}{1 + \frac{R_p^2}{\omega^2 L_p^2}} \right] = R_p \left[\frac{1}{1 + Q^2} \right]$ $L_s = L_p \left[\frac{1}{1 + \frac{\omega^2 L_p^2}{R_p^2}} \right] = L_p \left[\frac{1}{1 + \frac{1}{Q^2}} \right]$
(b) 	$R_p = R_s \left[1 + \frac{\omega^2 L_s^2}{R_s^2} \right] = R_s [1 + Q^2]$ $L_p = L_s \left[1 + \frac{R_s^2}{\omega^2 L_s^2} \right] = L_s \left[1 + \frac{1}{Q^2} \right]$
(c) 	$R_s = R_p \left[\frac{1}{1 + \omega^2 C_p^2 R_p^2} \right] = R_p \left[\frac{1}{1 + Q^2} \right]$ $C_s = C_p \left[1 + \frac{1}{\omega^2 C_p^2 R_p^2} \right] = C_p \left[1 + \frac{1}{Q^2} \right]$
(d) 	$R_p = R_s \left[1 + \frac{1}{\omega^2 C_s^2 R_s^2} \right] = R_s [1 + Q^2]$ $C_p = C_s \left[\frac{1}{1 + \omega^2 C_s^2 R_s^2} \right] = C_s \left[\frac{1}{1 + \frac{1}{Q^2}} \right]$

$$X_p = X_1 \left(1 + \frac{1}{Q_r^2} \right) = X_{C_0} \quad (1-1)$$

and

$$R_r = R_1 (1 + Q_r^2) \quad (1-2)$$

where

$$Q_r = \frac{X_1}{R_1} \text{ at frequency } f_r \quad (1-3)$$

Equation (1-1) shows that when Q_r is much smaller than 1, the equivalent parallel inductive reactance of the motional arm is much larger than X_1 and can, for a suitable value of Q_r , resonate with X_{C_0} . Equation (1-2) shows that the equivalent resistance of the crystal at resonance differs from R_1 by the factor $(1 + Q_r^2)$. However, since Q_r is much smaller than 1, the difference is small and R_r is usually only slightly greater than R_1 .

As the frequency is further increased, the crystal impedance increases rapidly until at frequency f_a , X_e again falls to zero and R_e has the value R_a . At this frequency the equivalent motional arm inductance X_1 again resonates with C_0 , and Equations (1-1) and (1-2) can be restated as:

$$X_p = X_1 \left(1 + \frac{1}{Q_a^2}\right) = X_{C_0} \quad (1-4)$$

$$R_a = R_1 (1 + Q_a^2) \quad (1-5)$$

where

$$Q_a = \frac{X_1}{R_1} \text{ at frequency } f_a \quad (1-6)$$

At f_a , however, $Q_a \gg 1$ (see behavior of X_1 characteristic) and, therefore,

$$X_p \approx X_1 \quad (1-7)$$

$$R_a \approx \frac{X_1^2}{R_1} \quad (1-8)$$

Other frequencies of less interest are f_m and f_n , the frequencies at which the crystal exhibits its minimum and maximum impedances, respectively, and f_p , the frequency at which the motional arm reactance is equal to that of C_0 . It should be noted that f_p does not quite coincide with the antiresonance frequency f_a because of the presence of R_1 in the motional arm. The difference is, however, at the most only a few parts in a million.

An indication of the bandwidth in which these effects occur may be obtained by noting that, for most crystals, the capacitance ratio r lies between 200 and 500. Substituting a typical value of $r = 300$ into the equation given in Table 1-2 for f_p , the ratio of f_p to f_s obtained is:

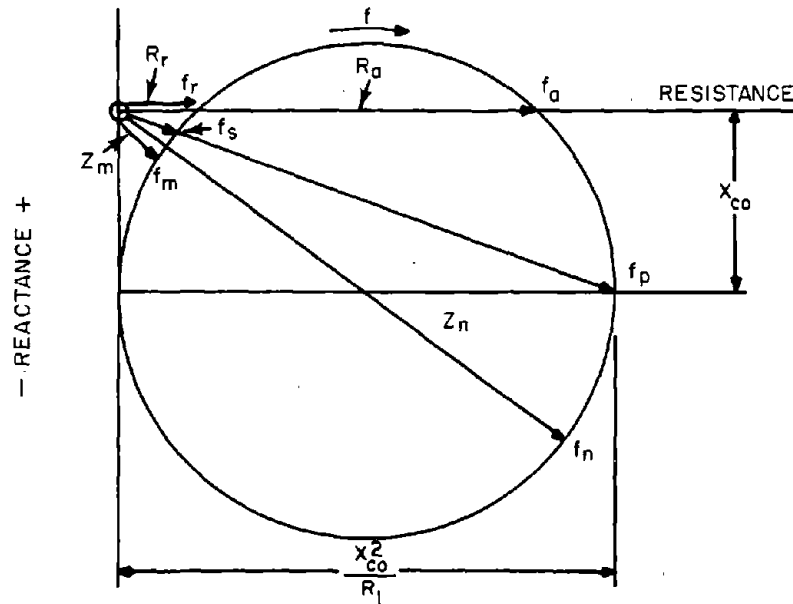
$$\frac{f_p}{f_s} = \left(1 + \frac{1}{r}\right)^{1/2} \approx 1 + \frac{1}{2r} = 1.0017 \quad (1-9)$$

For example, if $f_s = 1$ MC, then the bandwidth within which the crystal resonance effects occur will be typically less than 2 KC.

The spacing between f_s and f_r is very small; frequency differences of 1 or 2 parts per million are typical. The frequency difference between f_s and f_m is equal to that between f_s and f_r .

The electrical impedance of a crystal unit can also be presented as an impedance plane loci as shown in Figure 1-3, provided that:

$$\frac{1}{2\pi (f_n - f_m) C_0} \gg R_1 \quad (1-10)$$



TP1072-3

Figure 1-3. Impedance Diagram of a Crystal

This presentation is useful in that it gives a qualitative indication of the behavior of the phase angle of the crystal unit and notably of the high rate of change of phase angle exhibited in the frequency band between f_m and f_n . In this presentation the scaling is again misleading. In practice, the center of the circular loci would be located much closer to the resistance axis, greatly increasing the ratio of R_a to R_r .

Virtually all crystal oscillators are designed to employ a crystal unit operating in the region between f_s and f_a , and the foregoing is a useful quantitative interpretation of the behavior of a crystal resonator in this frequency

range. However, a more detailed analysis is required to more clearly define the desirable operating conditions and to determine the limits within which operation should be maintained. This is the purpose of the following analysis which determines the detailed behavior of a crystal unit:

- (a) Alone
- (b) In association with a parallel capacitance
- (c) In conjunction with a series capacitance

1-2. CRYSTAL BEHAVIOR IN FREQUENCY RANGE BETWEEN f_s AND f_p

Figure 1-4 shows the circuit to be analyzed. The analysis is greatly simplified if the motional arm elements C_1 and L_1 are first replaced by their effective total reactance valid in the frequency range between f_s and f_p , the frequencies of crystal series and parallel resonance, respectively. As previously pointed out, this frequency increment ($f_p - f_s$) is of the order of 0.2 percent of f_s ; that is:

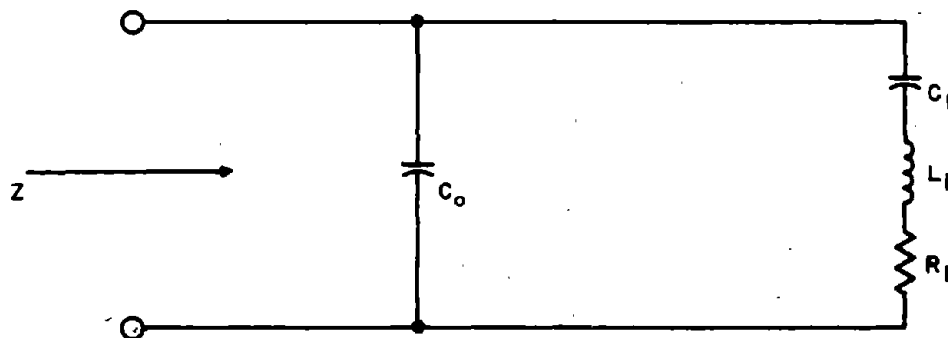
$$\frac{f_p - f_s}{f_s} \approx 0.002 \quad (1-11)$$

The reactance of C_1 is:

$$X_{C_1} = \frac{1}{\omega C_1} \quad (1-12)$$

Therefore:

$$\frac{d(X_{C_1})}{d\omega} = - \frac{1}{\omega^2 C_1} \quad (1-13)$$



TP1072-11

Figure 1-4. Crystal Equivalent Electrical Circuit

Since the frequency band of interest is between f_s and f_p , ω can be replaced in Equation (1-13) by:

$$\omega = \omega_s + \Delta\omega \quad (1-14)$$

where:

$$\begin{aligned} \Delta\omega &\leq \omega_p - \omega_s \\ &\ll \omega_s \end{aligned} \quad (1-15)$$

Therefore, Equation (1-13) becomes:

$$\frac{d(X_{C_1})}{d\omega} = \frac{1}{(\omega_s + \Delta\omega)^2 C_1} \quad (1-16)$$

The typical maximum value of $\frac{\Delta\omega}{\omega_s}$ is given by Equation (1-11) as 0.002.

Since this is small relative to 1, a valid approximation, neglecting second order differences, is:

$$\frac{d(X_{C_1})}{d\omega} \approx - \frac{1}{\omega_s^2 C_1} \left(1 - \frac{2 \Delta\omega}{\omega_s} \right) \quad (1-17)$$

The term $\frac{2 \Delta\omega}{\omega_s}$ is still small in comparison to 1 and therefore:

$$\frac{d(X_{C_1})}{d\omega} \approx - \frac{1}{\omega_s^2 C_1} \quad (1-18)$$

At the frequency f_s , L_1 and C_1 are in series resonance and therefore:

$$\omega_s^2 = \frac{1}{L_1 C_1} \quad (1-19)$$

Substituting Equation (1-19) into Equation (1-18) gives:

$$\frac{d(X_{C_1})}{d\omega} = - L_1 \quad (1-20)$$

The reactance of L_1 is:

$$X_{L_1} = \omega L_1 \quad (1-21)$$

Therefore:

$$\frac{d(X_{L_1})}{d\omega} = L_1 \quad (1-22)$$

The two reactances X_{L_1} and X_{C_1} , therefore, have the same differential with respect to frequency but are of opposite sign. The differential of the series combination of the two is, therefore:

$$\frac{d(X_{L_1} - X_{C_1})}{d\omega} = 2 L_1 \quad (1-23)$$

and the incremental change of reactance is:

$$d(X_s) = 2 L_1 d\omega = 4\pi L_1 df \quad (1-24)$$

where:

$$X_s = X_{L_1} - X_{C_1} \quad (1-25)$$

The value of X_s at frequency f_s is zero and, consequently, for frequencies between f_s and f_p :

$$X_s = 4\pi L_1 \Delta f \quad (1-26)$$

where Δf is the incremental frequency change from f_s .

As derived, Equation (1-26) is only valid for frequencies between f_s and f_p , but is equally valid over a similar range of frequencies immediately below f_s .

Using the value of X_s obtained from Equation (1-26), the equation for the crystal impedance is:

$$Z = \frac{-j X_{C_0} (R_1 + j 4\pi L_1 \Delta f)}{R_1 + j (4\pi L_1 \Delta f - X_{C_0})} \quad (1-27)$$

Defining Q_s as:

$$Q_s = \frac{4\pi L_1 \Delta f}{R_1} \quad (1-28)$$

Equation (1-27) can be restated as:

$$Z = \frac{-j X_{C_o} (1 + j Q_s)}{1 + j \left(Q_s - \frac{X_{C_o}}{R_1} \right)} \quad (1-29)$$

Separating this equation into real and imaginary parts gives:

$$Z = \frac{X_{C_o}^2}{R_1} \cdot \frac{1}{\left[1 + \left(\frac{X_{C_o}}{R_1} - Q_s \right)^2 \right]} + j \left\{ \frac{X_{C_o}^2}{R_1} \cdot \frac{\left(\frac{X_{C_o}}{R_1} - Q_s \right)}{\left[1 + \left(\frac{X_{C_o}}{R_1} - Q_s \right)^2 \right]} - X_{C_o} \right\} \quad (1-30)$$

Equating the imaginary term to zero gives the value of Q_s required to make the crystal impedance resistive:

$$Q_s = \frac{X_{C_o}}{2 R_1} \pm \left[\left(\frac{X_{C_o}}{2 R_1} \right)^2 - 1 \right]^{1/2} \quad (1-31)$$

$$(I_m = 0)$$

Equation (1-31) has two real values, provided that:

$$\frac{X_{C_o}}{2 R_1} > 1 \quad (1-32)$$

The smaller value corresponds to the value of Q_s required for crystal resonance and the other to crystal anti-resonance. Equation (1-31) also shows that if:

$$\frac{X_{C_o}}{2 R_1} = 1 \quad (1-33)$$

only one value of Q_s satisfies the requirements that make Z resistive. For values of

$$\frac{X_{C_0}}{2 R_1} < 1,$$

the crystal always has a reactive component and resonance does not occur.

Equation (1-32) establishes a limiting condition of operation for the crystal alone if it is to exhibit a resonance characteristic. (In the literature the ratio X_{C_0}/R_1 is frequently referred to as the Figure of Merit M . A crystal unit with $M = 2$, is therefore only just capable of achieving resonance.)

This is not, however, the only requirement that has to be satisfied. The main concern is with the rate of change of phase angle with frequency capability of the crystal, and this further limits the permissible minimum value of X_{C_0}/R_1 . This can be determined in the following way:

The phase angle of the crystal is:

$$\phi = \tan^{-1} \left\{ \frac{X_{C_0}}{R_1} - Q_s - \frac{R_1}{X_{C_0}} \left[1 + \left(\frac{X_{C_0}}{R_1} - Q_s \right)^2 \right] \right\} \quad (1-34)$$

Expanding and simplifying Equation (1-34) gives:

$$\tan \phi = Q_s - \frac{R_1}{X_{C_0}} \left(1 + Q_s^2 \right) \quad (1-35)$$

Differentiating Equation (1-35) with respect to Q_s gives:

$$\frac{d(\tan \phi)}{d Q_s} = 1 - \frac{2 R_1}{X_{C_0}} \cdot Q_s \quad (1-36)$$

Q_s is directly proportional to incremental frequency and therefore the rate of change of ϕ with respect to Q_s is a direct measure of the rate of change of ϕ with respect to frequency. That is:

$$\frac{d\phi}{df} = \frac{d\phi}{dQ_s} \cdot \frac{dQ_s}{\Delta f} = \frac{4\pi L_1}{R_1} \cdot \frac{d\phi}{dQ_s} \quad (1-37)$$

$\frac{d\phi}{dQ_s}$ is related to $\frac{d(\tan \phi)}{dQ_s}$ by the equation:

$$\frac{d\phi}{dQ_S} = \frac{d(\tan \phi)}{dQ_S} \bigg/ \frac{d(\tan \phi)}{d\phi} = \frac{d(\tan \phi)}{dQ_S} \cdot \cos^2 \phi \quad (1-38)$$

Substituting from Equation (1-36) into Equation (1-38) gives:

$$\frac{d\phi}{dQ_S} = \left(1 - \frac{2 R_1}{X_{C_0}} \cdot Q_S \right) \cos^2 \phi \quad (1-39)$$

The behavior of $d\phi/dQ_S$ can be determined for various X_{C_0}/R_1 ratios by substituting values of Q_S into Equations (1-34) and (1-39). These calculations result in the curves of Figure 1-5 which shows:

- (a) The characteristics of $d\phi/dQ_S$ are symmetrical about that value of Q_S giving $d\phi/dQ_S$ equal to zero.
- (b) The maximum values of $d\phi/dQ_S$ approach limiting values of ± 1 as X_{C_0}/R_1 increases.
- (c) The maximum values of $d\phi/dQ_S$ commence to decrease rapidly for X_{C_0}/R_1 values less than 3.
- (d) The maximum value of $d\phi/dQ_S$ always occurs when the crystal unit appears capacitive.
- (e) The crystal unit phase angle at which $d\phi/dQ_S$ is a maximum also increases rapidly with decreasing X_{C_0}/R_1 , becoming increasingly capacitive for X_{C_0}/R_1 values less than 3.
- (f) $d\phi/dQ_S$ at zero phase angle is always smaller than the maximum value of $d\phi/dQ_S$. As shown by the loci of $d\phi/dQ_S$ ($\phi = 0$), the difference is negligible for X_{C_0}/R_1 ratios greater than 4, but is substantial for lower values of X_{C_0}/R_1 .

In the light of this behavior, it can be concluded that for X_{C_0}/R_1 values of 4 or greater, the maximum value of $d\phi/dQ_S$ occurs in the immediate vicinity of zero phase angle; that is, near to crystal resonance frequency f_r or anti-resonance frequency f_a . For X_{C_0}/R_1 values less than 3 or 4, the $d\phi/dQ_S$ at f_r and f_a decreases significantly below the maximum attainable, which can then only be obtained by operating at a frequency below f_r or above f_a which gives the required phase angle. However, standardization of crystal measuring methods and crystal unit frequency specification plus the difficulty of introducing a stable complementary phase angle in the oscillator feedback loop tend to rule against

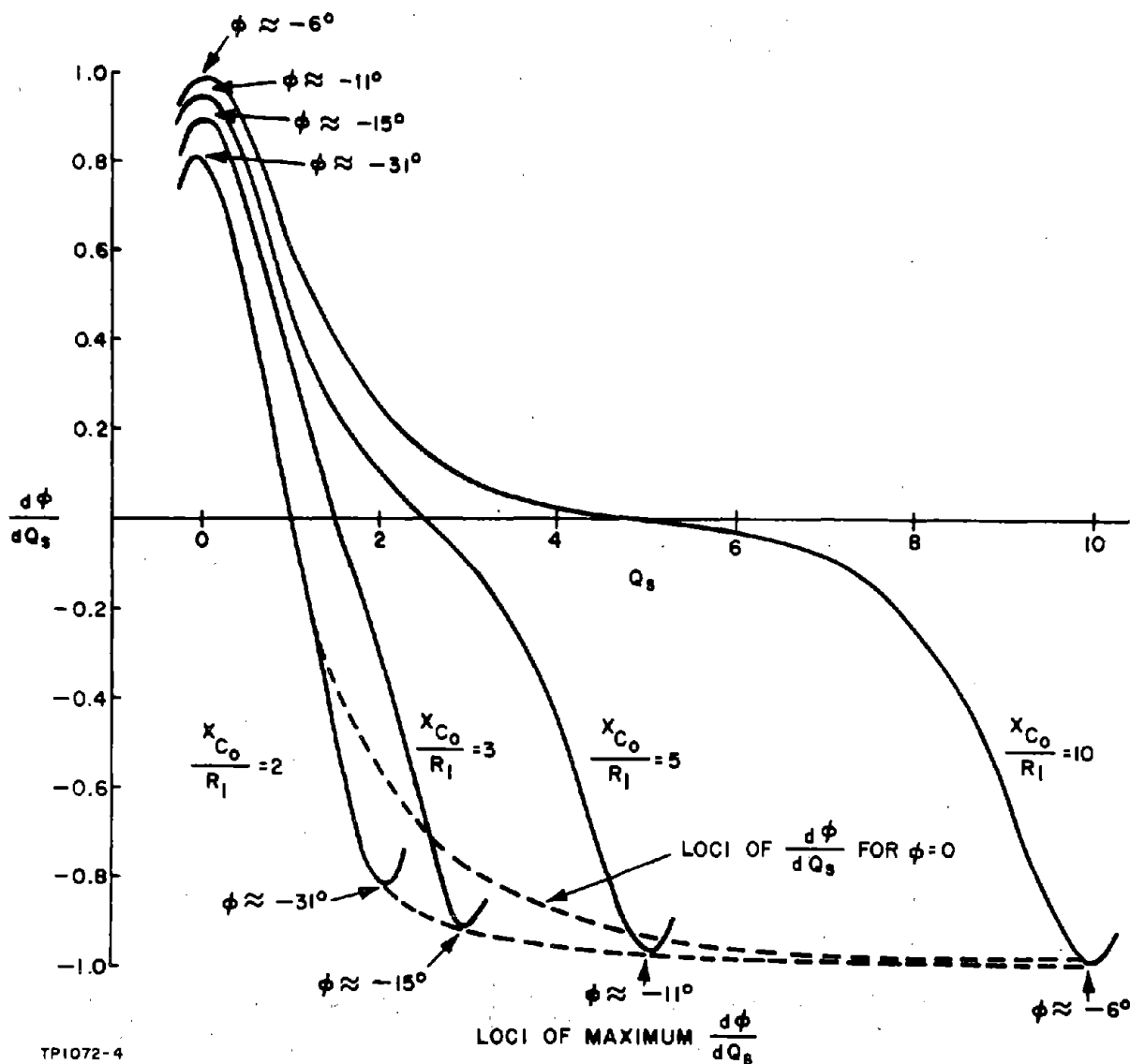
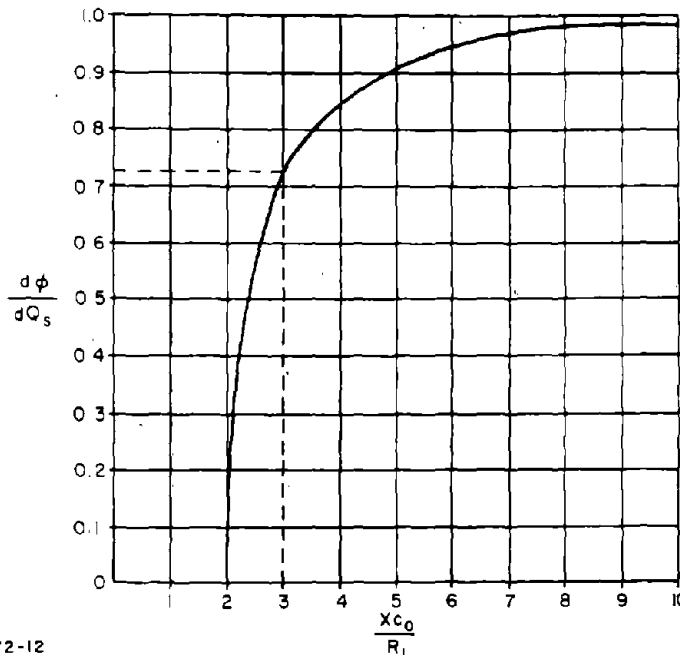


Figure 1-5. Behavior of $\frac{d\phi}{dQ_s}$ as a Function of Q_s and $\frac{X_{C_0}}{R_1}$.

this type of operation, and operation with X_{C_0}/R_1 values of less than 3 is not normally used. When this condition occurs naturally, as it may in crystals designed for operation at frequencies above 100 MC, it is normal practice to place an inductor across the crystal unit to resonate with C_0 , thereby effectively increasing the apparent value of X_{C_0}/R_1 . At all frequencies below 100 MC, X_{C_0}/R_1 has a value greater than 3, and operation at zero phase angle has negligible adverse effects on the crystal unit phase-changing capabilities. Figure

1-6 shows the behavior of $d\phi/dQ_s$ for zero phase angle operation as a function of X_{C_0}/R_1 and illustrates the rapid deterioration of $d\phi/dQ_s$ for values of X_{C_0}/R_1 less than 4.



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Figure 1-6. $d\phi/dQ_s$ at $\phi = 0$ As a Function of X_{C_0}/R_1

The graph of Figure 1-7 is derived from Equations (1-35) and (1-36) and shows the variation of ϕ as a function of Q_s using X_{C_0}/R_1 as a parameter. Since Q_s is proportional to the incremental frequency Δf , these curves are indicative of the phase angle of the crystal between f_r and f_a . No particular significance is attached to these curves except that they crudely show the increasing rate of change of ϕ at $\phi = 0$ with increasing values of X_{C_0}/R_1 and the general behavior of the crystal unit phase angle between f_r and f_p .

1-3. RELATIONSHIP OF R_1 TO R_r

The crystal parameters that are readily measured are R_r , the resonance resistance, and C_0 . Before the preceding formulae can be applied to a doubtful case, it is therefore necessary to determine R_1 from R_r . Referring to Figure 1-8 (a), at resonance the crystal unit can be considered as X_{C_0} , R_r , and X_{L_p} in parallel, where:

$$X_{L_p} = X_{C_0} \quad (1-40)$$

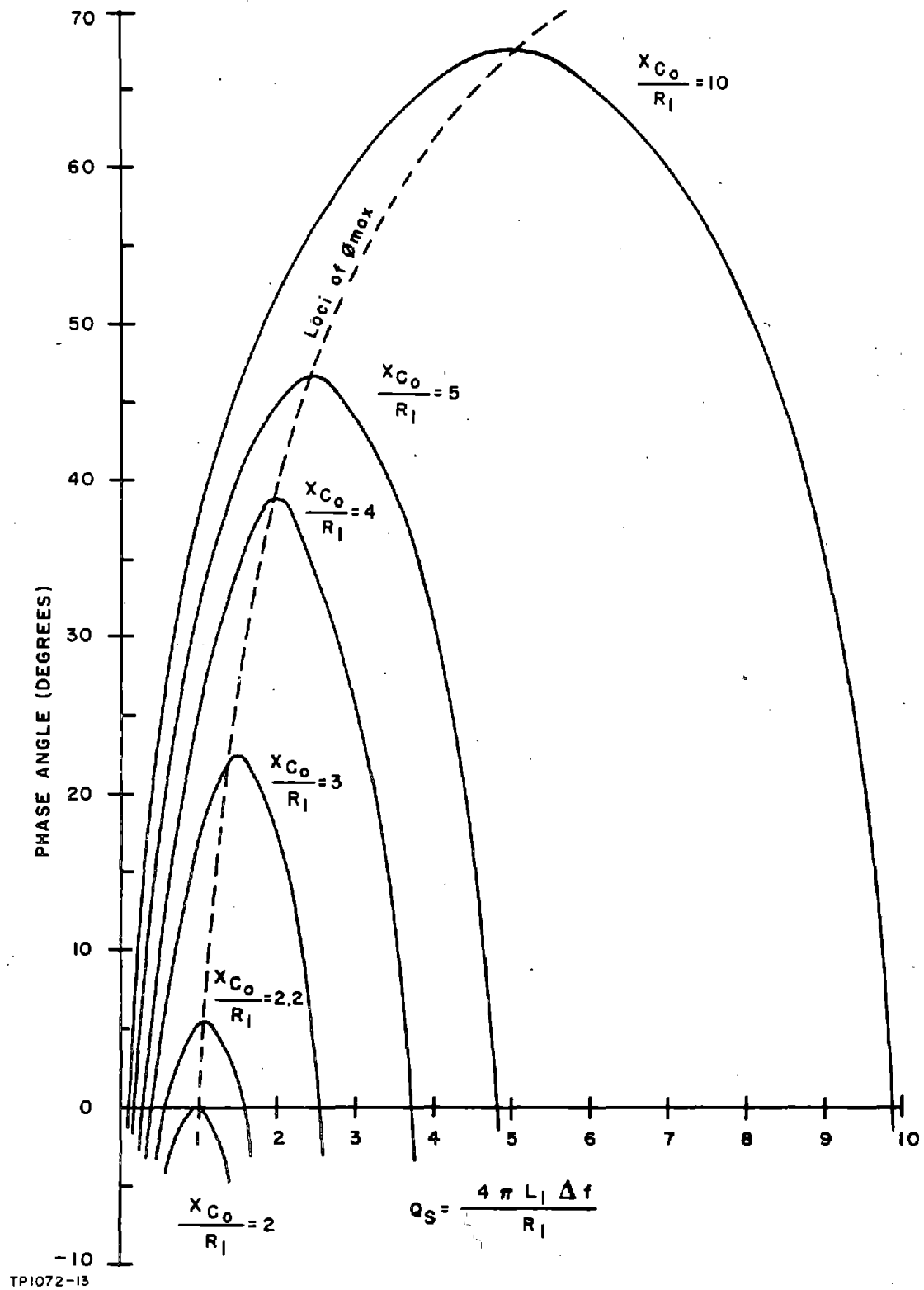


Figure 1-7. Crystal Phase Angle as a Function of Q_s for Various X_{Co}/R_1 Values

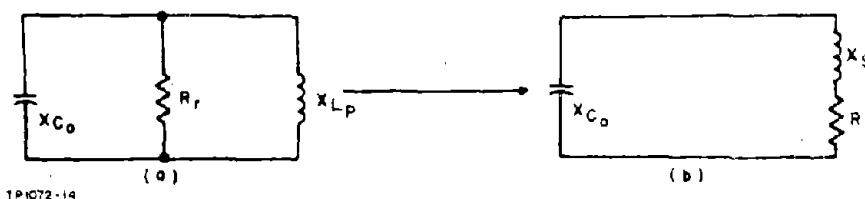


Figure 1-8. Relationship Between R_p and R_1

Referring to Figure 1-8 (b), since R_p is the effective parallel resistance of the network at f_r due to R_1 , the Q of R_r and X_{L_p} in parallel is the same as that of X_S and R_1 in series. Therefore:

$$Q_s = \frac{R_r}{X_{L_p}} = \frac{R_r}{X_{C_0}} \quad (1-41)$$

Reference to the table of parallel-to-series transformations (Table 1-1) then gives:

$$R_1 = R_r \left[\frac{1}{1 + \left(\frac{R_r}{X_{C_0}} \right)^2} \right] \quad (1-42)$$

and

$$X_S = X_{C_0} \left[\frac{1}{1 + \left(\frac{X_{C_0}}{R_r} \right)^2} \right] \quad (1-43)$$

Figure 1-9 (a) shows a normalized graph of Equation (1-42) as a function of Q_s and shows the rapid increase in R_r relative to R_1 as X_{C_0} and R_r approach equality.

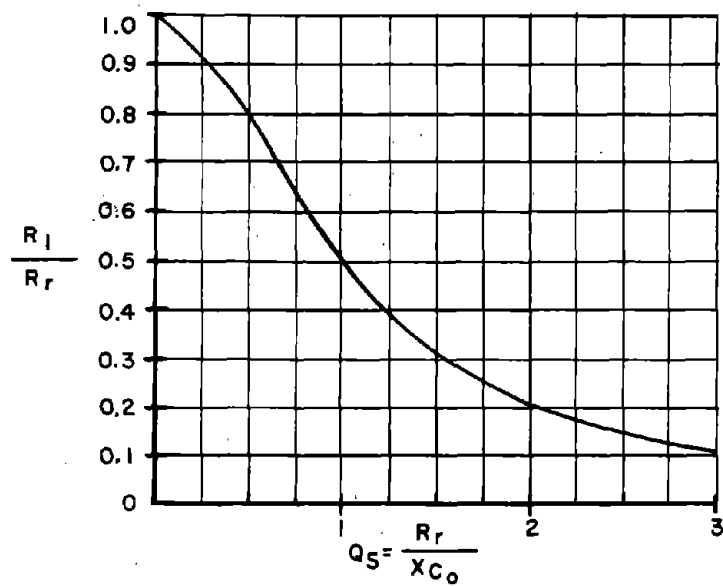
The relationship between the measured quantities R_r and X_{C_0} and X_{C_0}/R_1 is:

$$\frac{X_{C_0}}{R_1} = \frac{X_{C_0}}{R_r} \cdot \frac{R_r}{R_1} \quad (1-44)$$

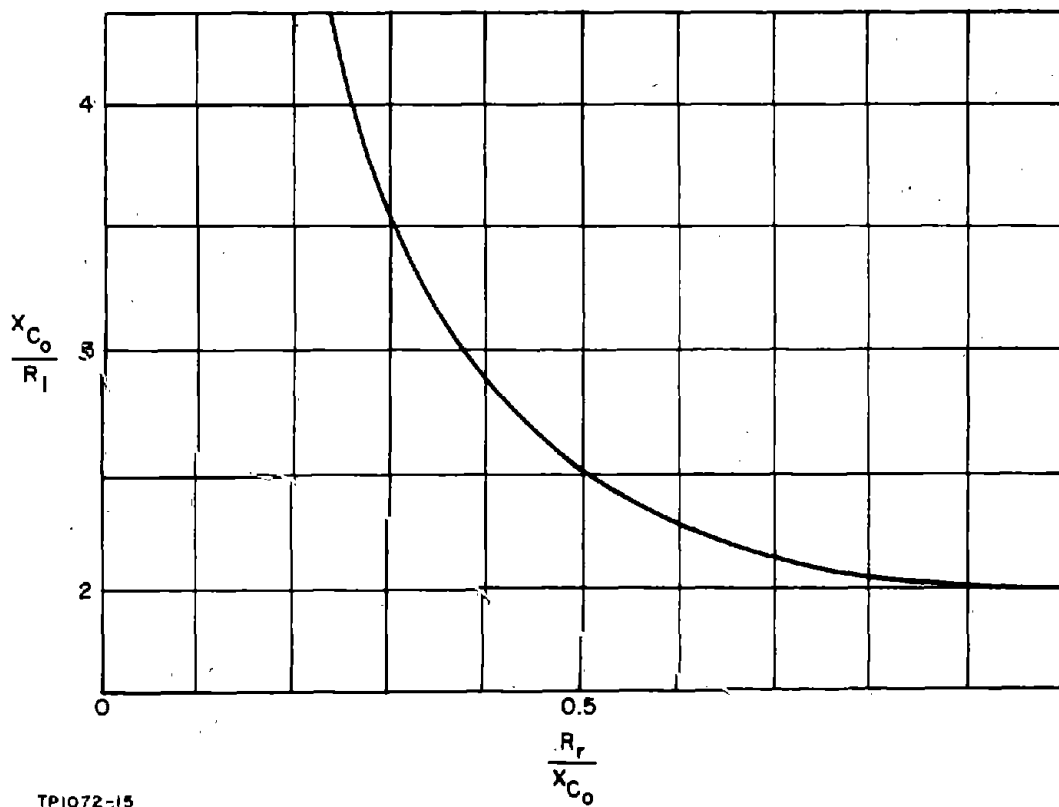
Inserting values of R_r/X_{C_0} into Equation (1-42) gives the resulting plot of Figure 1-9 (b). Comparing this graph with that of Figure 1-6 shows that

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(a)



(b)



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Figure 1-9. Relationship Between $\frac{R_r}{X_{C_0}}$, $\frac{R_1}{R_r}$, and $\frac{X_{C_0}}{R_1}$

operation below R_T/X_{C_0} ratios of at least 0.35 and preferably 0.25 is desirable if the phase shifting capability of the crystal unit is to be fully utilized. In all military type crystal units, except those designed for operation above 100 MC, R_T/X_{C_0} 's of 0.35 or less are guaranteed by their specification. The danger lies in external oscillator capacitance causing the crystal circuit to operate in this undesired region.

1-4. CRYSTAL UNIT OPERATION WITH A PARALLEL CAPACITANCE

The preceding discussion shows that the crystal unit exhibits a high rate of change of phase angle in the neighborhood of its resonance and anti-resonance frequencies. Operation of a crystal unit at resonance in an oscillator circuit is readily achieved over the entire frequency range of 1 KC to 200 MC.

Operation at anti-resonance is not, however, very practical. In the first place the crystal unit impedance is very high at the anti-resonance frequency, and difficulty would be experienced in obtaining suitable matching into the oscillator circuit. Also, in the majority of crystal unit types, C_0 has values in the range of 5 to 10 PF, and oscillator circuit stray capacitance across the crystal unit terminals could easily introduce an appreciable effective increase in C_0 . And since the anti-resonance frequency is directly related to C_0 , a decrease in effective anti-resonance frequency would result, causing the oscillation to occur at a frequency lower than f_a . Stray circuit capacitance can vary markedly between circuits of the same type and can also vary due to aging or environmental stress. Furthermore, the effect of a given amount of circuit strays on the oscillator frequency would vary markedly between crystal units of the same type, due to differences of their parameters.

All of these factors would lead to oscillator frequency tolerances much greater than those of the crystal unit alone, and, since the object is to make the oscillator frequency solely dependent on the crystal unit, this is therefore undesirable. A method of reducing these undesirable effects is to manufacture the crystal unit so that the equivalent of anti-resonance operation occurs at a specified frequency with a specified value of external crystal "loading" capacitance. In the oscillator circuit the major part of the loading capacitance is then formed by a variable capacitor, and the circuit stray capacitance constitutes the remaining part. The variable capacitor is adjusted until oscillation occurs at the crystal unit frequency.

Placing a loading capacitance C_L in parallel with the crystal unit is equivalent to increasing C_0 . Therefore, if C_0 and X_{C_0} are replaced by $C_0 + C_L$ and $X(C_0 + C_L)$, respectively, in the preceding analysis, Equations (1-27) to (1-44) describe the behavior of this circuit. If the value of C_L is sufficiently large to make the effect of circuit stray capacitance changes negligible and

sufficiently small so that $\frac{X(C_o + C_L)}{R_1}$ does not approach the limiting value of 2, the parallel combination of the crystal unit and C_L can be used as an anti-resonant circuit at the frequency f'_a , where f'_a is the new frequency of anti-resonance with C_L in circuit. This is a possible method of usage in certain frequency ranges where the conditions placed on C_L can be met. Crystal units are made specifically for operation in this or a very similar manner to be discussed in the next subsection.

1-5. CRYSTAL UNIT OPERATION WITH A SERIES LOADING CAPACITOR

Another method of operation uses a loading capacitor in series with the crystal unit. This method also has certain limiting conditions, and the following analysis develops design criteria for this type of crystal circuit.

Figure 1-10 shows the circuit to be analyzed. The impedance seen at the input terminals is:

$$Z = - \left[\frac{j X_{C_o} (1 + j Q_s)}{1 + j \left(Q_s - \frac{X_{C_o}}{R_1} \right)} + j X_{C_L} \right] \quad (1-45)$$

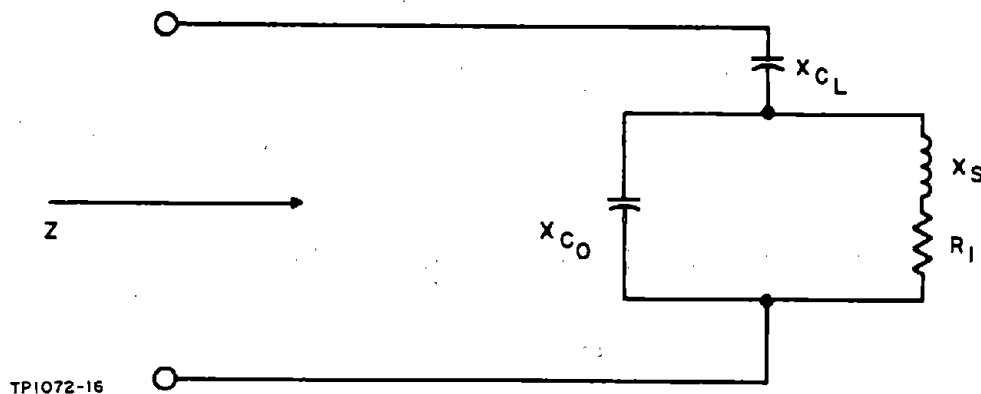


Figure 1-10. Crystal With Series Loading Capacitor

After some manipulation, Equation (1-45) can be written in the form:

$$Z = \frac{X_{C_o}^2}{R_1} \cdot \frac{1}{1 + \left(\frac{X_{C_o}}{R_1} - Q_s \right)^2} \left[1 + j \left\{ \frac{X_{C_o}}{R_1} - Q_s - \frac{R_1}{X_{C_o}^2} (X_{C_L} + X_{C_o}) \left[1 + \left(\frac{X_{C_o}}{R_1} - Q_s \right)^2 \right] \right\} \right] \quad (1-46)$$

The network is resistive when the imaginary term of Equation (1-46) is zero. Equating the imaginary term to zero and solving for Q_s gives:

$$Q_s = \frac{X_{C_0}}{2R_1} \left[\frac{1 + 2\left(\frac{X_{C_L}}{X_{C_0}}\right)}{1 + \left(\frac{X_{C_L}}{X_{C_0}}\right)} \right]^{\pm} \left\{ \left[\frac{X_{C_0}}{2R_1 \left(1 + \frac{X_{C_L}}{X_{C_0}}\right)} \right]^2 - 1 \right\}^{1/2} \quad (1-47)$$

(Im = 0)

The condition for Equation (1-47) to have two real roots is that:

$$\frac{X_{C_0}}{2R_1 \left(1 + \frac{X_{C_L}}{X_{C_0}}\right)} > 1 \quad (1-48)$$

When two real roots occur the smaller value of Q_s obtained from Equation (1-47) is the value of Q_s at which the circuit exhibits resonance characteristics, and the larger value of Q_s corresponds to that required in order that the circuit appears anti-resonant.

Equation (1-48) establishes the minimum conditions necessary for the network to exhibit resonance characteristics. This is not, however, the only requirement of the network. The network should not only exhibit resonance and anti-resonance characteristics, but should also have a large rate of change of phase angle with frequency. This requirement adds further limitations to the values of $\frac{X_{C_0}}{R_1}$ and $\frac{X_{C_L}}{X_{C_0}}$ that can be effectively employed.

The phase angle of the network is:

$$\phi = \tan^{-1} \left\{ \frac{X_{C_0}}{R_1} - Q_s - \frac{R_1 X_{C_L}}{X_{C_0}^2} \left[1 + \left(\frac{X_{C_0}}{R_1} - Q_s \right)^2 \right] - \frac{R_1}{X_{C_0}} \left[1 + \left(\frac{X_{C_0}}{R_1} - Q_s \right)^2 \right] \right\} \quad (1-49)$$

This equation can be rearranged in the form:

$$\tan \phi = -Q_s^2 \cdot \frac{R_1}{X_{C_0}} \left(1 + \frac{X_{C_L}}{X_{C_0}} \right) + Q_s \left(1 + 2 \frac{X_{C_L}}{X_{C_0}} \right) - \left[\frac{R_1}{X_{C_0}} \left(1 + \frac{X_{C_L}}{X_{C_0}} \right) + \frac{X_{C_L}}{R_1} \right] \quad (1-50)$$

The rate of change of $\tan \phi$ as a function of Q_s is:

$$\frac{d(\tan \phi)}{dQ_s} = 1 + 2 \frac{X_{CL}}{X_{C_0}} - 2 Q_s \cdot \frac{R_1}{X_{C_0}} \left(1 + \frac{X_{CL}}{X_{C_0}} \right) \quad (1-51)$$

Equation (1-51) is zero when:

$$Q_s = \frac{X_{C_0}}{2R_1} \cdot \frac{\left(1 + 2 \frac{X_{CL}}{X_{C_0}} \right)}{\left(1 + \frac{X_{CL}}{X_{C_0}} \right)} \quad (1-52)$$

As in the previous analysis, when the phase angle ϕ is less than 10 degrees:

$$\frac{d\phi}{dQ_s} \approx \frac{d(\tan \phi)}{dQ_s} \quad (1-53)$$

$\frac{d\phi}{dQ_s}$ can now be calculated using Equations (1-47) and (1-51) for various values of $\frac{X_{C_0}}{R_1}$ and $\frac{X_{CL}}{X_{C_0}}$. The curves of Figure 1-11 are obtained from such calculations and show $\frac{d\phi}{dQ_s}$ as a function of $\frac{X_{C_0}}{R_1}$, using $\frac{X_{CL}}{X_{C_0}}$ as a parameter. The

curve drawn for $\frac{X_{CL}}{X_{C_0}} = 0$ corresponds to that of Figure 1-6 which was derived for a crystal unit alone without C_L . It, therefore, serves as a reference to which the values of $\frac{d\phi}{dQ_s}$ obtained for various values of $\frac{X_{CL}}{X_{C_0}}$ can be compared. Using this comparison, it is evident that for low values of $\frac{X_{C_0}}{R_1}$ the degradation can be more severe in this case than when the crystal is used without a loading capacitor.

The reduction in $\frac{d\phi}{dQ_s}$ is not, however, as severe in marginal cases when C_L is used in series with the crystal as would be the case if the same value of C_L was connected in parallel with the crystal. It is therefore possible to operate a crystal with a given series loading capacitor for lower values of $\frac{X_{C_0}}{R_1}$ without suffering a severe reduction in $\frac{d\phi}{df}$ than would be the case using the same

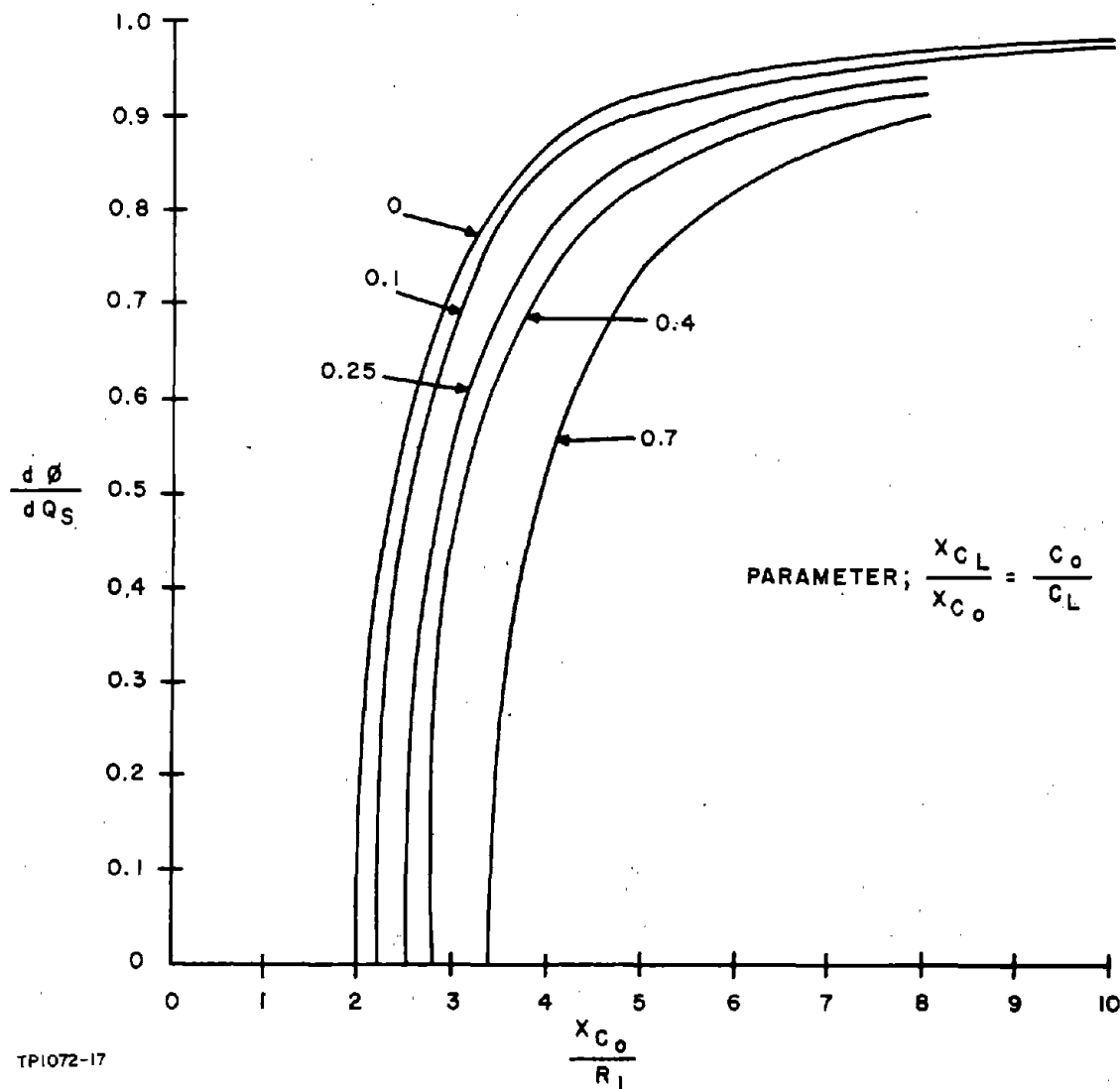


Figure 1-11. $d\phi/dQ_s$ as a Function of X_{C_0}/R_1 and X_{C_L}/X_{C_0}

loading capacitor in parallel with the crystal. To illustrate this, Figure 1-11 shows that $\frac{d\phi}{dQ_s}$ is zero when $\frac{X_{C_0}}{R_1} = 2.8$ and $\frac{X_{C_L}}{X_{C_0}} = 0.4$. If the same value of X_{C_L} is in parallel with the crystal, the total parallel capacitance is increased to:

$$C_t = C_0 + C_L = 3.5 C_0 \quad (1-54)$$

For parallel capacitive loading, $d\phi/dQ_s = 0$ when:

$$\frac{X_{C_L}}{R_1} = 2 \quad (1-55)$$

Substituting for X_{C_L} in terms of X_{C_0} in Equation (1-55) gives:

$$\frac{X_{C_0}}{R_1} = 7 \quad (1-56)$$

showing that for parallel capacitive loading, the ratio X_{C_0}/R_1 will need to be greater than 7 for resonance to occur; while for series capacitive loading, the requirement is that X_{C_0}/R_1 be greater than 2.8. The conclusion to be drawn from this comparison is that when the ratio X_{C_0}/R_1 is small, parallel capacitive loading is more likely to degrade the phase-shifting capability of the network than would equal series-capacitive loading.

1-6. CRYSTAL UNIT TYPES

The preceding analyses show three ways in which the quartz crystal unit can exhibit a high rate of change of phase angle as a function of frequency. These are:

- (a) Operation at the resonance frequency f_r (f_s at frequencies above, say, 100 MC) where the crystal acts as a series resonant element.
- (b) Operation in association with a parallel capacitance at f'_a , the anti-resonant frequency of the combination, where the crystal unit appears inductive.
- (c) Operation in association with a series capacitance at the frequency where the combination acts as a series resonant circuit. This frequency is almost equal to, and for all practical purposes, can be regarded as f'_a .

A fourth method using the crystal unit as a capacitive element in conjunction with an inductor is possible. However, it is not used because operation is difficult due to the possibility of oscillations at other undesired frequencies, since the crystal unit appears capacitive both at frequencies below f_r and above f_a . Furthermore, the circuit will often oscillate at a non-controlled frequency via C_0 when the crystal unit is defective.

Military crystal units are specified for the frequency range of 16 KC to 125 MC at the present time by MIL-C-3098C/1 to 61 and cater for the three types of operation detailed in (a), (b), and (c) in the applicable frequency ranges. Operation at series resonance is possible at all frequencies, while operation with a series or parallel capacitor is confined to the 16 KC to 20 MC and 100 KC to 20 MC ranges, respectively, due to the limitations imposed by the X_{C_0}/R_1 values. The frequency spacing between series resonance and anti-resonance with a loading capacitor is generally of the order of several hundred parts per million for fundamental crystal units. The oscillator frequency tolerance desired is usually much less than this and, therefore, two types of crystal units are manufactured. These are designated as series resonance and anti-resonance crystal units, the latter type sometimes being referred to as a parallel crystal unit. Series crystal units are designed for operation at f_r and anti-resonant crystal units for operation with either a series- or parallel-loading capacitor of a specified value at the frequency at which the combination appears resonant or anti-resonant. The nominal frequency at which this occurs is stamped on the crystal holder together with the crystal unit type in order to provide positive identification.

There are more than 50 individual crystal specifications, each one detailing the characteristics and limits of performance of a particular type of crystal unit in a given frequency range. In some frequency ranges crystal units are manufactured having various performance characteristics and physical configurations, and consequently several crystal unit types may be applicable in a certain frequency range. The individual specification sheets contain the following data:

- (a) Type of operation
- (b) Crystal holder type
- (c) Whether fundamental or overtone mode of operation
- (d) Applicable frequency range
- (e) Overall frequency tolerance
- (f) Load capacitance value where applicable
- (g) Rated or nominal crystal unit dissipation rating
- (h) Maximum value of C_0
- (i) Maximum value of equivalent resistance

- (j) Maximum frequency change under specified conditions of shock and vibration
- (k) Maximum equivalent resistance change under specified conditions of shock and vibration
- (l) Maximum change of frequency due to aging under specified conditions
- (m) Test conditions for crystal unit measurements in the appropriate standard crystal unit test set

The overall frequency tolerance, defining the frequency limits within which f_r or f'_a may vary over a given temperature range about the nominal frequency of the crystal unit, consists of two parts:

- (a) That due to the variation of the crystal resonant or anti-resonant frequency with temperature
- (b) The tolerance incurred in the manufacture of the crystal unit

In certain frequency ranges crystal units of the same construction are available with a variety of overall frequency tolerances. In these cases the reduction in tolerance is achieved by closer control of the manufacturing process in order to minimize both (a) and (b).

Crystal unit types, designed for operation in an oven under temperature-controlled conditions, have three frequency tolerances. These are:

- (a) The tolerance when operated within a specified narrow temperature range. This is known as the operating temperature range frequency tolerance and is the crystal unit manufacturing tolerance plus the tolerance allowed for the variation of crystal unit frequency over the small temperature range.
- (b) The tolerance placed on the allowable frequency variation over the narrow temperature range around the nominal operating temperature. This is known as the stability within the overall frequency tolerance.
- (c) The tolerance placed on the allowable frequency variation over the much wider operable temperature range which is usually comparable with that of the non-temperature controlled crystal units of similar design.

In both cases, the shock, vibration, and aging frequency tolerances are additional to the preceding tolerances.

The specified value of maximum equivalent resistance applies throughout the crystal operating temperature range. A typical crystal will usually have an equivalent resistance considerably smaller than the maximum value, generally one-third to one-half of the maximum. However, the total range of equivalent resistance found in a large batch of crystal units of the same type and frequency may be as great as 9 to 1. Therefore, when oscillators are being produced in large quantities, this range of equivalent resistance values is likely to be encountered, and the oscillator circuit must be designed to accept this wide variation and still perform satisfactorily. Field replacement considerations indicate that this is also advisable when only a few oscillators are involved.

The crystal unit power dissipation rating should not be exceeded under any conditions of operation. Although crystals can be operated at higher dissipation levels than those specified without catastrophic failure, several undesired effects occur. The coupling into undesired oscillation modes tends to increase with crystal unit drive level, possibly causing sudden increases in R_e , particularly as a function of temperature which may in severe cases cause oscillation to cease.

High crystal unit dissipation is also frequently synonymous with high loop gain, particularly in vacuum tube circuits, and this can lead to oscillation at the crystal unit spurious modes normally occurring at frequencies slightly higher than f_r or f'_a . Frequently the crystal unit equivalent resistance at these spurious mode frequencies is less than twice that at the desired mode, and the possibility of shock excitation into one of these spurious modes is significant under high loop gain conditions. f_r or f'_a are also functions of drive level and can vary at a rate of from 0.5 to 5 PPM per MW of crystal unit power dissipation. For crystal units having the latter characteristic, it can readily be seen that a significant increase in f_r or f'_a and hence in oscillator overall frequency tolerance can be caused by only a few milliwatts of overdrive.

The crystal unit power dissipation in an oscillator circuit depends to a great extent on the loop power gain, which is in turn dependent on the crystal equivalent resistance. Since the latter has a wide range of variation, the crystal unit dissipation also varies between individual crystal units in a given oscillator circuit. It is good design practice to ensure that, for the worst conditions, the crystal unit dissipation does not exceed the specified maximum.

A listing of all military standard crystal units is presented in Tables 1-4 through 1-6. Figure 1-12 shows the outline dimensions for crystal units utilizing different holders.

TABLE 1-4. PREFERRED CRYSTAL UNITS

Crystal-Unit Type	Frequency Range	Mode	Frequency Tolerance Percent (\pm)	Operating Temperature Range ($^{\circ}$ C)	Holder (See Figure 1-12)	Maximum R_T or R_o	Load Capacitance, (PF) ①	Rated Drive Level (MW)	Maximum Shunt Capacitance (PF)
CR-18A/U	0.8 to 20 MC	Fundamental	0.005	-55 to +105	HC-6/U	625 to 20 Ω	32.0 \pm 0.5	② 10.0 \pm 2.0 ③ 5.0 \pm 1.0	7.0
CR-19A/U	0.8 to 20 MC	Fundamental	0.005	-55 to +105	HC-6/U	520 to 15 Ω	"	② 10.0 \pm 2.0 ③ 5.0 \pm 1.0	7.0
CR-25A/U	200 to 500 KC	Fundamental	0.01	-40 to +85	HC-6/U	2.5 to 7.5 K	"	2.0 \pm 0.4	---
CR-26A/U	200 to 500 KC	Fundamental	0.002	70 to 80	HC-6/U	2.5 to 7.5 K	"	2.0 \pm 0.4	---
CR-27A/U	0.8 to 20 MC	Fundamental	④ 0.002	70 to 80	HC-6/U	625 to 20 Ω	32.0 \pm 0.5	② 5.0 \pm 1.0 ③ 2.5 \pm 0.5	7.0
CR-28A/U	0.8 to 20 MC	Fundamental	④ 0.002	70 to 80	HC-6/U	520 to 15 Ω	"	② 5.0 \pm 1.0 ③ 2.5 \pm 0.5	7.0
CR-32A/U	10 to 75 MC	Third Overtone	0.002 0.005	70 to 80	HC-6/U	40 to 60 Ω	"	⑥ 2.0 \pm 0.4 ⑦ 1.0 \pm 0.2	7.0
CR-35A/U	0.8 to 20 MC	Fundamental	⑤ 0.002	80 to 90	HC-6/U	520 to 15 Ω	"	② 5.0 \pm 1.0 ③ 2.5 \pm 0.5	7.0
CR-36A/U	0.8 to 20 MC	Fundamental	⑤ 0.002	80 to 90	HC-6/U	625 to 20 Ω	32.0 \pm 0.5	② 5.0 \pm 1.0 ③ 2.5 \pm 0.5	7.0
CR-37A/U	90 to 250 KC	Fundamental	0.02	-40 to +70	HC-13/U	5 to 5.5 K	20.0 \pm 0.5	2.0 \pm 0.4	⑧
CR-38A/U	16 to 100 KC	Fundamental	0.012	-40 to +70	HC-13/U	110 to 90 K	20.0 \pm 0.5	0.1	⑨
CR-42A/U	90 to 250 KC	Fundamental	0.003	70 to 80	HC-13/U	4.5 to 5 K	32.0 \pm 0.5	2.0 \pm 0.4	⑧
CR-45/U	455 KC	Fundamental	0.02	-40 to +70	HC-6/U	3.3 K	"	2.0 \pm 0.4	5.0 \pm 2.5
CR-47A/U	200 to 500 KC	Fundamental	0.002	70 to 80	HC-6/U	5.3 to 8.5 K	20.0 \pm 0.5	2.0 \pm 0.4	---
CR-50A/U	16 to 100 KC	Fundamental	0.012	-40 to +70	HC-13/U	100 to 60 K	"	0.1	⑨
CR-52A/U	10 to 61 MC	Third Overtone	0.005	-55 to +105	HC-6/U	40 Ω	"	⑥ 4.0 \pm 0.8 ⑦ 2.0 \pm 0.4	7.0
CR-54A/U	50 to 125 MC	Fifth Overtone	0.005	-55 to +105	HC-6/U	50 to 60 Ω	"	2.0 \pm 0.4	7.0
CR-55/U	17 to 61 MC	Third Overtone	0.005	-55 to +105	HC-18/U	40 Ω	"	2.0 \pm 0.4	7.0
CR-56A/U	50 to 125 MC	Fifth Overtone	0.005	-55 to +105	HC-18/U	50 to 60 Ω	"	2.0 \pm 0.4	7.0
CR-59A/U	50 to 125 MC	Fifth Overtone	⑤ 0.002	80 to 90	HC-18/U	50 to 60 Ω	"	1.0 \pm 0.2	7.0
CR-60A/U	5 to 20 MC	Fundamental	0.005	-55 to +105	HC-18/U	50 to 20 Ω	"	5.0 \pm 1.0	7.0
CR-61/U	17 to 61 MC	Third Overtone	⑤ 0.002	80 to 90	HC-18/U	40 Ω	"	⑥ 2.0 \pm 0.4 ⑦ 1.0 \pm 0.2	7.0

See footnotes at end of Table 1-4.

TABLE 1-4. PREFERRED CRYSTAL UNITS (Cont.)

Crystal-Unit Type	Frequency Range	Mode	Frequency Tolerance Percent (\pm)	Operating Temperature Range ($^{\circ}$ C)	Holder (See Figure 1-12)	Maximum R_T or R_B	Load Capacitance, (PF) ①	Rated Drive Level (MW)	Maximum Shunt Capacitance (PF)
CR-63A/U	200 to 500 KC	Fundamental	⑩ 0.01	-40 to +70	HC-6/U	5.3 to 8.5 K	20.0 \pm 0.5	2.0 \pm 0.4	---
CR-64/U	4 to 20 MC	Fundamental	0.005	-55 to +105	HC-18/U	120 to 25 Ω	30.0 \pm 0.5	5.0 \pm 1.0	7.0
CR-65/U	10 to 61 MC	Third Overtone	④ 0.001	70 to 80	HC-6/U	40 Ω	"	⑥ 2.0 \pm 0.4 ⑦ 1.0 \pm 0.2	7.0
CR-66/U	3 to 20 MC	Fundamental	0.0025	-55 to +105	HC-6/U	60 to 25 Ω	30.0 \pm 0.5	② 10.0 \pm 2.0 ③ 5.0 \pm 1.0	7.0
CR-67/U	17 to 61 MC	Third Overtone	0.0025	-55 to +105	HC-18/U	40 Ω	"	2.0 \pm 0.4	7.0
CR-68/U	3 to 20 MC	Fundamental	④ 0.002	70 to 80	HC-6/U	15 to 40 Ω	32.0 \pm 0.5	5.0 \pm 1.0	7.0
CR-69/U	2.9 to 20 MC	Fundamental	0.0025	-55 to +105	HC-18/U	175 to 25 Ω	30.0 \pm 0.5	5.0 \pm 1.0	7.0
CR-71/U	4.5 to 5.5 MC	Fifth Overtone	0.00008	+0.5 ¹¹	HC-30/U	175 Ω Max 100 Ω Min	32.0 \pm 0.5	70 UA \pm 20%	4.0 \pm 10%
CR-72/U	17 to 61 MC	Third Overtone	0.005	-55 to +105	HC-18/U	40 Ω	"	2 MW	7.0
CR-75/U	50 to 125 MC	Fifth Overtone	④ 0.001	70 to 80	HC-6/U	40 Ω	"	1.0 \pm 0.2	7.0
CR-76/U	17 to 61 MC	Third Overtone	0.0025	-55 to +105	HC-18/U	40 Ω	"	2.0 \pm 0.4	3.5
CR-77/U	17 to 62 MC	Third Overtone	0.0025	-55 to +105	HC-25/U	40 Ω	"	2.0 \pm 0.4	7.0
CR-78/U	2.9 to 20 MC	Fundamental	0.005	-55 to +105	HC-25/U	175 to 25 Ω	30.0 \pm 0.5	5.0 \pm 1.0	7.0
CR-79/U	2.9 to 20 MC	Fundamental	0.005	-55 to +105	HC-25/U		"	5.0 \pm 1.0	7.0
CR-80/U	50 to 125 MC	Fifth Overtone	0.0025	-55 to +105	HC-18/U	50 to 60 Ω	"	2.0 \pm 0.4	7.0
CR-81/U	17 to 61 MC	Third Overtone	0.005	-55 to +105	HC-25/U	40 Ω	"	2.0 \pm 0.4	7.0
CR-82/U	50 to 125 MC	Fifth Overtone	0.005	-55 to +105	HC-25/U	50 to 60 Ω	"	2.0 \pm 0.4	7.0
CR-83/U	50 to 125 MC	Fifth Overtone	0.0025	-55 to +105	HC-25/U	50 to 60 Ω	"	2.0 \pm 0.4	7.0
CR-84/U	17 to 61 MC	Third Overtone	0.002	80 to 90	HC-25/U	40 Ω	"	⑥ 2.0 \pm 0.4 ⑦ 1.0 \pm 0.2	7.0
CR-85/U	0.8 to 20 MC	Fundamental	0.0025	-55 to +105	HC-6/U	520 to 15 Ω	"	② 10.0 \pm 2.0 ③ 5.0 \pm 1.0	7.0

See footnote at end of Table 1-4.

TABLE 1-4. PREFERRED CRYSTAL UNITS (Cont)

FOOTNOTES:

- ① When a load capacitance is given, the crystal unit is designed to operate at anti-resonance (parallel resonance). Crystal units which have infinite load capacitance are designed to operate at series resonance.
- ② For frequencies of 10 MC and lower.
- ③ For frequencies above 10 MC.
- ④ Frequency tolerance at room temperature: ± 0.007 percent.
- ⑤ Frequency tolerance at room temperature: ± 0.008 percent.
- ⑥ For frequencies of 25 MC and lower.
- ⑦ For frequencies above 25 MC.
- ⑧ Maximum shunt capacitance shall be computed using the following formula:

Frequency (KC)	Capacitance (PF)
90 to 170	$\frac{450}{f} + 1.2, \pm 15$ percent
170+ to 250	$\frac{322}{f} + 1.2, \pm 15$ percent

Where f = the specified frequency in KC.

- ⑨ Maximum shunt capacitance shall be computed using the following formula:

16 to 34	$\frac{24}{\sqrt{f}} + 1.6, \pm 15$ percent
34+ to 54	$\frac{33}{\sqrt{f}} + 1.6, \pm 15$ percent
54+ to 100	$\frac{24}{\sqrt{f}} + 1.6, \pm 15$ percent

Where f = the specified frequency in KC.

- ⑩ Frequency tolerance over secondary operating temperature range (-55° to -40° and 70° to 90° C): ± 0.015 percent.
- ⑪ At point of zero temperature coefficient; must be a specific temperature between 65° and 77° C.

TABLE 1-5. SPECIAL-APPLICATION CRYSTAL UNITS^①

Crystal-Unit Type	Frequency Range	Mode	Frequency Tolerance Percent (±)	Operating Temperature Range (°C)	Holder	Electrodes	Load Capacitance (PF) ^②	Rated Drive Level (MW)	Maximum Shunt Capacitance (PF)
CR-15B/U	80 to 200 KC	Fundamental	0.01	-40 to +70	HC-21/U ^③	Plated	32.0 ±0.5	2.0 ±0.4	---
CR-16B/U	80 to 200 KC	Fundamental	0.01	-40 to +70	HC-21/U ^③	Plated	∞	2.0 ±0.4	---
CR-24/U	15 to 50 MC	15 to 25 MC Third Overtone 25+ to 50 MC Fifth Overtone	0.005	-55 to +105	HC-10/U ^③	Pressure	∞	2.0 ±0.4	7.0
CR-29A/U	80 to 200 KC	Fundamental	0.002	70 to 80	HC-21/U ^③	Plated	32.0 ±0.5	2.0 ±0.4	---
CR-30A/U	80 to 200 KC	Fundamental	0.002	70 to 80	HC-21/U ^③	Plated	∞	2.0 ±0.4	---
CR-33A/U	10 to 25 MC	Third Overtone	0.005	-55 to +105	HC-6/U ^④	Plated	32.0 ±0.5	2.5 ±0.5	12.0
CR-43/U	80,860 KC	Fundamental	0.01	-30 to +75	HC-16/U ^③	Plated	45.0 ±1.0	2.0 ±0.4	45.0
CR-46A/U	200 to 500 KC	Fundamental	0.01	-40 to +85	HC-6/U ^④	Plated	20.0 ±0.5	2.0 ±0.4	---
CR-51A/U	10 to 61 MC	Third Overtone	0.005	-55 to +105	HC-6/U ^④	Pressure	∞	20.0 ±4.0	7.0
CR-53A/U	50 to 87 MC	Fifth Overtone	0.005	-55 to +105	HC-6/U ^④	Pressure	∞	20.0 ±4.0	7.0
CR-57/U	500 KC	Fundamental	^⑤ 0.001	80 to 90	HC-6/U ^④	Plated	32.0 ±0.5	0.5	7.0
CR-62/U	0.8 to 20 MC	Fundamental	0.001	70 to 80	HC-6/U ^④	Plated	32.0 ±0.2	^⑥ 5.0 ±1.0 ^⑦ 2.5 ±0.5	7.0

① These units are suitable for special applications but not for general use. Specific approval of the Government is required prior to each intended use. A written justification of necessity is required before their use in new equipment design, and shall be submitted as soon as possible after the circuit design has firmed to the point at which the need for one of these crystal-unit type is evident.

② When a load capacitance is given, the crystal unit is designed to operate at anti-resonance (parallel resonance). Crystal units which have infinite load capacitance are designed to operate at series resonance.

③ See Specification MIL-H-10056 for dimensions of this crystal holder.

④ See Figure 1-12 for dimensions of crystal units utilizing this holder.

⑤ Frequency tolerance over secondary operating temperature range (20° to 80°C): ±0.005 percent.

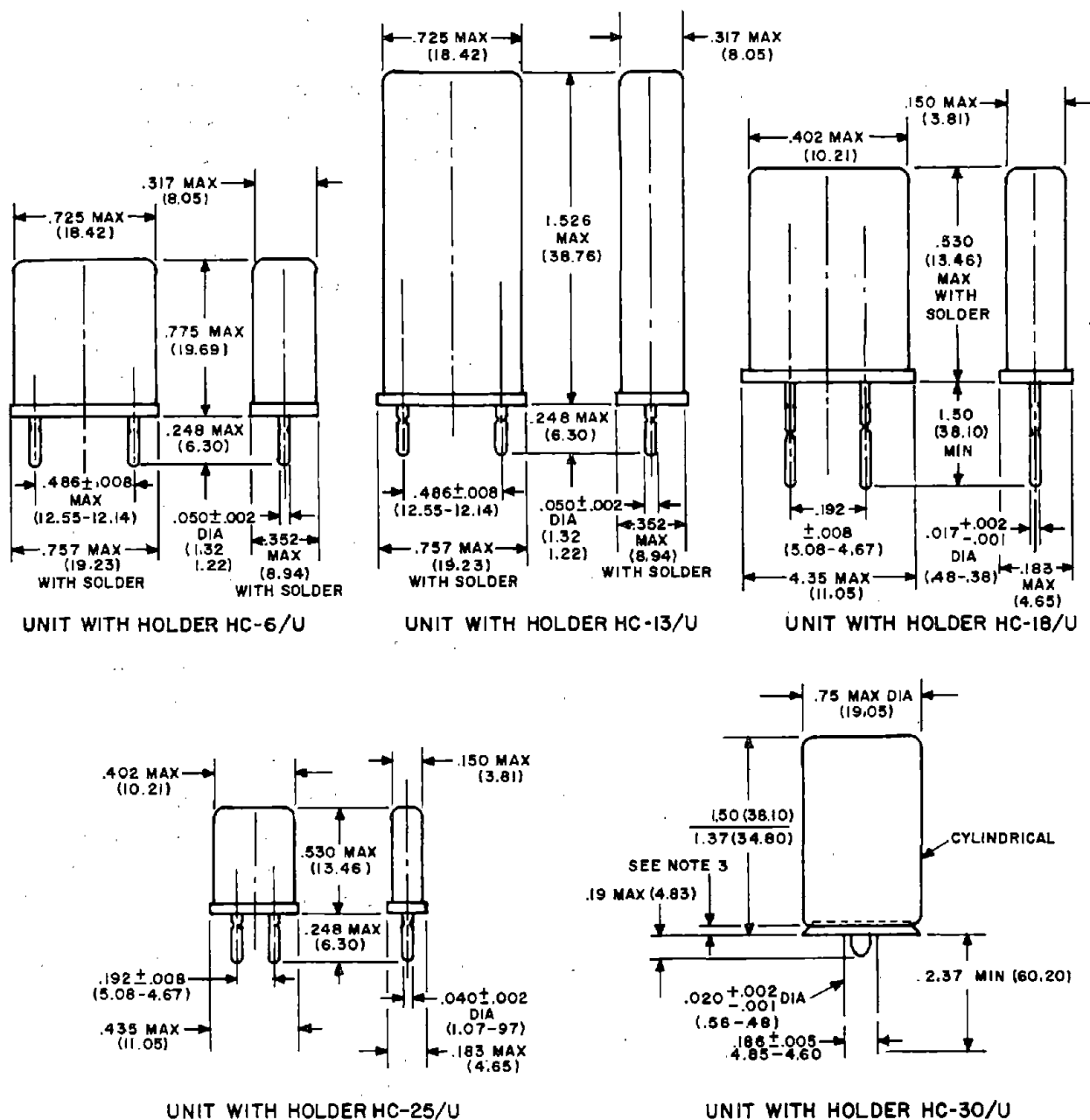
⑥ For frequencies above 10 MC and lower.

⑦ For frequencies above 10 MC.

TABLE 1-6. CRYSTAL-UNIT TYPES CROSS-REFERENCED BY FREQUENCIES

Frequency Range (KC)	Crystal-Unit Type	Preferred or Special Application
16 to 100	CR-38A/U CR-50A/U	Preferred
80 to 200	CR-15B/U CR-16B/U CR-29A/U CR-30A/U	Special Application
80.860	CR-43/U	Special Application
90 to 250	CR-37A/U CR-42A/U	Preferred Preferred
200 to 500	CR-25A/U CR-26A/U CR-46A/U CR-47A/U CR-63A/U	Preferred Preferred Special Application Preferred Preferred
455	CR-45/U	Preferred
500	CR-57/U	Special Application

Frequency Range (MC)	Crystal-Unit Type	Preferred or Special Application
0.8 to 20	CR-18A/U CR-19A/U CR-27A/U CR-28A/U CR-35A/U CR-36A/U CR-62/U CR-65/U	Preferred Preferred Preferred Preferred Preferred Preferred Special Application Preferred
2.9 to 20.0	CR-69/U CR-78/U	Preferred Preferred
3.0 to 20.0	CR-66/U CR-68/U	Preferred Preferred
4 to 20	CR-64/U	Preferred
4.5 to 5.5	CR-71/U	Preferred
5 to 20	CR-60A/U	Preferred
10 to 25	CR-33 A/U	Special Application
10 to 61	CR-51A/U CR-52A/U CR-65/U	Special Application Preferred Preferred
15 to 50	CR-24/U	Special Application
17 to 61	CR-55/U CR-61/U CR-67/U CR-76/U CR-81/U CR-84/U	Preferred Preferred Preferred Preferred Preferred Preferred
17 to 62	CR-77/U	Preferred
50 to 87	CR-53A/U	Special Application
50 to 91	CR-59A/U	Preferred
50 to 125	CR-54A/U CR-58A/U CR-75/U CR-80/U CR-82/U CR-83/U	Preferred Preferred Preferred Preferred Preferred Preferred



NOTES:

1. ALL DIMENSIONS IN INCHES.
2. METRIC DIMENSIONS IN PARENTHESES ARE SHOWN FOR GENERAL INFORMATION ONLY AND ARE BASED UPON 1 INCH=25.4 MM.
3. NO LIMITING DIMENSIONS FOR SEAL AREA.

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Figure 1-12. Outline Dimensions for Complete Crystal Units

1-7. CRYSTAL PARAMETER MEASUREMENTS

Military crystal units are specified in such a way that only three characteristics are of primary importance to the oscillator designer. These are:

- (a) The crystal unit frequency. For series resonance crystal units this is the resonance frequency f_r , and for anti-resonance crystal units the anti-resonance frequency f'_a when loaded with a specified value of capacitance C_L .
- (b) The crystal unit equivalent resistance. For series resonance crystal units this is the series resonance resistance R_r , and for anti-resonance crystal units the equivalent resistance R_e of the crystal unit and the specified loading capacitor C_L in series at the anti-resonance frequency.
- (c) The crystal dissipation rating.

The standard equipment for the testing of crystal units is the Crystal Impedance or CI Meter. The purpose of this equipment is to provide a standard method of testing crystal units, thereby ensuring a fair measure of agreement of crystal unit parameter measurements.

The basic principle used in the CI Meter to test a series resonance crystal unit is one of comparing the crystal unit being tested to a known resistor in an oscillator circuit. The comparison is made in the feedback network of an oscillator; and when the frequency and amplitude of oscillation coincide in response to oscillator tuning, loop gain adjustments, and variation of the substitution resistor, the crystal unit resonance resistance is equal to that of the substitution resistor, and the frequency of oscillation is the same as the crystal unit resonance frequency. When testing anti-resonance crystal units, the method is slightly modified. In this case, the specified value of loading capacitance is inserted in series with the crystal unit, and this combination is then compared with the substitution resistor in the same manner used for series resonance crystal units to determine the crystal unit equivalent resistance and anti-resonance frequency. To ensure good repeatability, these measurements must be made at the rated crystal unit dissipation levels given in the crystal unit specifications. It is also possible to measure the value of C_0 and to derive values of the motional arm equivalent impedance elements R_1 , L_1 , and C_1 using the CI Meter.

Because of the wide frequency range of crystal units, there are four CI Meters designated as follows:

<u>Model Number</u>	<u>Frequency Range</u>
TS-710/TSM	10 KC to 1100 KC
TS-330/TSM	0.8 MC to 15 MC
TS-683/TSM	10 MC to 100 MC
AN/TSM-15	75 MC to 200 MC

The crystal unit specification details which CI Meter will be used for testing. The CI Meters are completely self-contained, and the only additional test equipment required is a frequency counter. Measurement repeatability and accuracy is of the order of 2 PPM on crystal frequency and 5 percent on crystal equivalent resistance.

CI Meters are not always available to the oscillator designer, and there are several alternative methods of crystal unit measurement of lower accuracy that can be employed. Two of these methods are as follows:

- (a) The oscillator being designed can be used as a CI Meter. When the oscillator uses a series resonance crystal unit, this entails repetitively substituting carbon resistors for the crystal unit in the oscillator circuit and adjusting the oscillator tuning until the oscillator frequency and output voltage amplitudes coincide.

To ensure reasonable accuracy using this method, the oscillator loop gain should only be just sufficient to maintain oscillation, thereby reducing the effects of amplifier non-linearity to a minimum. This is particularly necessary if a transistor amplifier is used in the oscillator. If the signal voltage appearing between emitter and base is large compared to the "linear" operating range of the emitter-base junction, the feedback network output is effectively open-circuited over a substantial portion of the oscillation period. Since the crystal unit has energy storage properties, the substitution resistor and the crystal unit will react in different ways to this non-linear operation and the comparison is no longer valid.

When the oscillator uses an anti-resonance crystal unit, the same method of measurement can be used if an inductor equal to that of the crystal unit at the anti-resonance frequency is connected in series with the substitution resistor. That is, the reactance of the inductor should equal that of the specified loading capacitor at the measuring frequency. A 1-percent error in the inductive reactance can cause a frequency error of as much as 5 PPM, and the

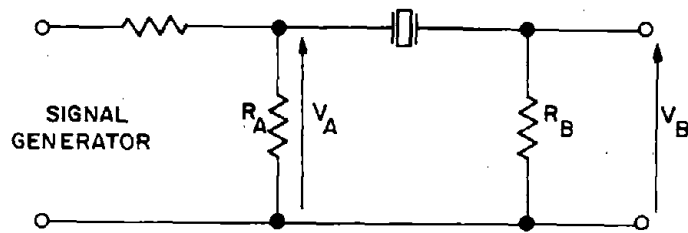
inductor must therefore be accurately adjusted in order to achieve good measuring accuracy. Similar considerations regarding minimization of oscillator loop gain also apply when measuring anti-resonance crystal units, although the effect of non-linear amplification should not be as great in this case.

Using this method of crystal unit measurement, the correlation with measurements made using a CI Meter can be expected to be within 2 PPM for frequency and 10-percent for resonance resistance for series resonance crystal units, and 5 PPM and 10-percent for anti-resonance crystal units, provided the precautions noted are taken.

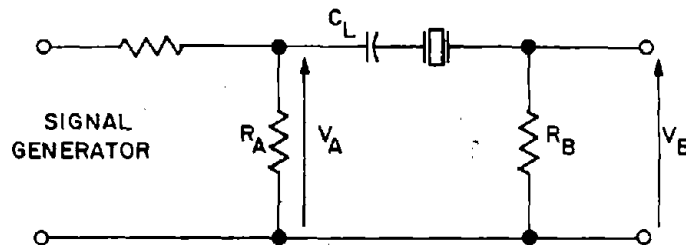
- (b) The crystal unit can also be measured with reasonable accuracy using a stable signal generator in the circuits shown in Figure 1-13. In these circuits R_A is small compared to the crystal unit equivalent resistance and R_B is comparable to the equivalent resistance. The crystal frequency is determined by adjusting the signal generator frequency until maximum output voltage is measured across R_B , and the crystal unit equivalent resistance is obtained by measuring V_A and V_B and calculating for the known value of R_B . Because of the narrow bandwidth within which resonance occurs, the signal source has to be highly stable in order to obtain meaningful results, and the signal generator will usually have to be operating for several hours before the random frequency drift is sufficiently low to permit measurements.

If an oscillator is being designed and two or more crystal units of the same nominal frequency are available, the oscillator (using one of the crystal units) can be used as a stable frequency driving source to measure the other crystal unit; the oscillator frequency being adjusted to coincide with that of the crystal under test by varying the oscillator tuning.

The frequency measured using this method is the frequency of maximum transmission f_m which coincides with the frequency of minimum crystal unit impedance. This frequency is several PPM below f_r , and there is therefore an inherent frequency measurement error. The correlation with measurements made using a CI Meter can be expected to be within 7 PPM for frequency and 10-percent for resistance.



(a) Series Resonance Crystal Unit Test Circuit



(b) Anti-resonance Crystal Unit Test Circuit

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Figure 1-13. Approximate Methods of Measuring Crystal Unit Frequency and Equivalent Resistance

1-8. OPERATION OF CRYSTAL UNIT AT RESONANCE WITH INDUCTIVE AND/OR RESISTIVE TERMINATION

The effect of a capacitance in series and/or in parallel with the crystal unit on the rate of change of phase angle with frequency was covered in Sections 1-2 to 1-5, and the desirable operating conditions were determined. The terminating load presented to the crystal unit by the remainder of the oscillator circuit can also appreciably degrade the phase changing properties of the crystal unit and requires investigation. The effect is different in series-resonance and anti-resonance oscillator circuits, and the former is treated first. The example used is that of a transistor oscillator, since this circuit presents a complex impedance to the crystal and therefore requires a more generalized analysis than does the equivalent vacuum tube circuit, the input impedance of which is essentially resistive.

A condition of operation that occurs in series type transistor oscillators entails the crystal unit operating at resonance into the emitter input impedance of the transistor as shown in Figure 1-14 (a). At frequencies above a few megacycles the input impedance of a tuned transistor amplifier is inductive, and the equivalent electrical crystal circuit is as shown in Figure 1-14 (b), where X and R are the amplifier series input impedance components. The effect of this type of operation on the $d\phi/df$ characteristic of the crystal can be determined approximately in the following manner.

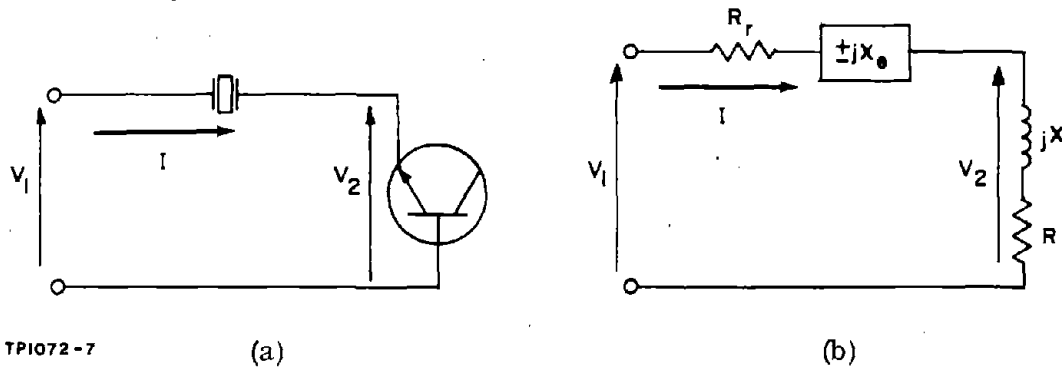


Figure 1-14. Crystal Unit Operating at Resonance into the Emitter Input Impedance of a Transistor

Provided that X_{C_0}/R_1 is larger than 5, the curves of Figure 1-5 show that the variation of $d\phi/dQ_s$ due to changes of ϕ of ± 10 degrees about the zero phase shift point will be less than ± 10 percent. Therefore, in this limited region of operation, $d\phi/dQ_s$ can be regarded as a constant. This is also shown qualitatively in Figure 1-7 where the phase angle curves are seen to be virtually linear in the region of zero phase angle. Therefore:

$$\frac{d\phi}{dQ_s} \approx K_1 \quad (1-57)$$

and

$$\phi \approx K_1 Q_s - \phi_k \quad (1-58)$$

where K_1 is the value of $d\phi/dQ_s$ at series resonance, which, for the condition stipulated, has a value in the range of 0.85 to 1 and ϕ_k is a constant phase angle given by:

$$\phi_k = \frac{4\pi L_1}{R_1} (f_s - f_r) K_1 \quad (1-59)$$

The impedance of the crystal unit can then be written as:

$$Z_C = R_r (1 + j \tan \phi) \quad (1-60)$$

and for phase angles less than 10 degrees, this can be approximated as:

$$Z_C \approx R_r \left[1 + j (K_1 Q_s - \phi_k) \right] \quad (1-61)$$

The loop equation for the network of Figure 1-14 is then:

$$V_1 = I \left\{ R_r \left[1 + j (K_1 Q_s - \phi_k) \right] + R + j X \right\} \quad (1-62)$$

Over the small frequency range of interest, the inductive component of the load is essentially constant. Therefore, the phase angle change of the voltage V_2 relative to V_1 is solely a function of the change in the phase angle of I relative to V_1 . The phase angle of V_1 relative to I is:

$$\phi_1 = \frac{R_r (K_1 Q_s - \phi_k) + X}{R_r + R} \quad (1-63)$$

The rate of change of phase angle of ϕ_1 with respect to Q_s is then:

$$\frac{d\phi_1}{dQ_s} = \frac{R_r}{R_r + R} \cdot K_1 \quad (1-64)$$

Dividing Equation (1-64) by Equation (1-57) gives:

$$\frac{d\phi_1 / d\phi}{dQ_s / dQ_s} = \frac{R_r}{R_r + R} \quad (1-65)$$

Equation (1-65) shows that the reduction in $d\phi/dQ_s$ incurred is solely due to the resistive component of the load and that the inductive component has no effect on the circuit rate of change of phase angle.

Since the stability of the oscillator is dependent on the phase shifting ability of the crystal unit when inserted in the feedback loop, it is desirable that the ratio given in Equation (1-65) should approach unity. That is, R should be much less than R_r . However, R does not constitute the total resistance in series with the crystal unit. The driving source will also have a series resistive component r which will have a similar effect to R in reducing the phase angle shifting capability of the crystal unit. Introducing r into Equation (1-65) gives:

$$\frac{d\phi_1 / d\phi}{dQ_s / dQ_s} = \frac{R_r}{R_r + R + r} \quad (1-66)$$

Equation (1-66) gives the total degradation of the circuit $d\phi/dQ_s$ relative to that of the crystal unit alone. One of the objects in oscillator design is to make $(R + r)$ as small as possible relative to R_r , subject to maintaining an adequate loop gain.

1-9. SERIES RESONANCE CRYSTAL UNIT POWER DISSIPATION

It is desirable that the crystal unit power dissipation should not exceed the rated value under all conditions of operation. Since the resonance resistance of a crystal unit is permitted such a wide range of variation, the limitations placed on the crystal terminating voltage levels are not evident and the purpose of the succeeding analysis is to determine the limits. The circuit to be analyzed is shown in Figure 1-15, where R_i represents the circuit at the amplifier input side of the crystal unit and V represents the voltage applied to the crystal unit by the feedback circuit connected to the amplifier output. This implies that the oscillator output represents a constant voltage source, a reasonable approximation because of the limiting that occurs. From Figure 1-15 the crystal unit dissipation P_c is:

$$P_c = \frac{V^2 R_r}{(R_i + R_r)^2} \quad (1-67)$$

This is the well-known power transfer equation which shows that P_c will be a maximum when R_i and R_r are matched. That is:

$$R_i = R_r \quad (1-68)$$

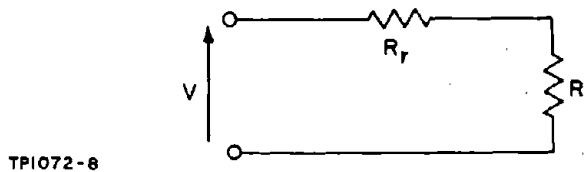


Figure 1-15. Effective Crystal Circuit in Series Resonant Oscillator

It has been previously shown that R_i contributes to the loading of the crystal unit and that it should be small relative to R_r if a large reduction in $d\phi/df$ is to be avoided. It is therefore undesirable that R_i should exceed R_r max, and it is preferable that it should be considerably smaller. Assuming R_i is not greater than R_r max, the maximum crystal unit dissipation will then be:

$$P_{c \text{ MAX}} = \frac{V^2}{4 R_i} \quad (1-69)$$

Substituting the crystal unit dissipation rating $P_{c \text{ MAX}}$ into Equation (1-69) and transposing gives:

$$V_{\max} = 2\sqrt{P_{c \text{ MAX}} \cdot R_i} \quad (1-70)$$

where V_{\max} is the maximum allowable crystal unit driving source voltage.

Equation (1-70) is applicable when R_i has a value intermediate between the minimum and maximum values of R_r . For the assumed 9-to-1 variation of R_r , R_i must have a value in the range:

$$\frac{1}{9} R_{r \text{ max}} \leq R_i \leq R_{r \text{ max}} \quad (1-71)$$

If R_i is less than $\frac{1}{9} R_{r \text{ max}}$, the maximum allowable driving source voltage is:

$$V_{\max} = \frac{9 R_i + R_{r \text{ max}}}{3 R_{r \text{ max}}} \sqrt{P_{c \text{ MAX}} \cdot R_{r \text{ max}}} \quad (1-72)$$

A compromise value of R_i that does not introduce excessive crystal unit loading but yet gives a reasonable voltage attenuation is obtained when R_i equals $\frac{1}{3} R_{r \text{ max}}$. The reduction in the circuit $d\phi/df$ below that of the crystal unit alone due to R_i will then be 25 percent for a worst-case crystal unit. Assuming this condition and a constant driving source voltage, the relative crystal unit dissipation is:

$$P_c = \frac{V^2 R_r}{\left(\frac{1}{3} R_{r \text{ max}} + R_r\right)^2} \quad (1-73)$$

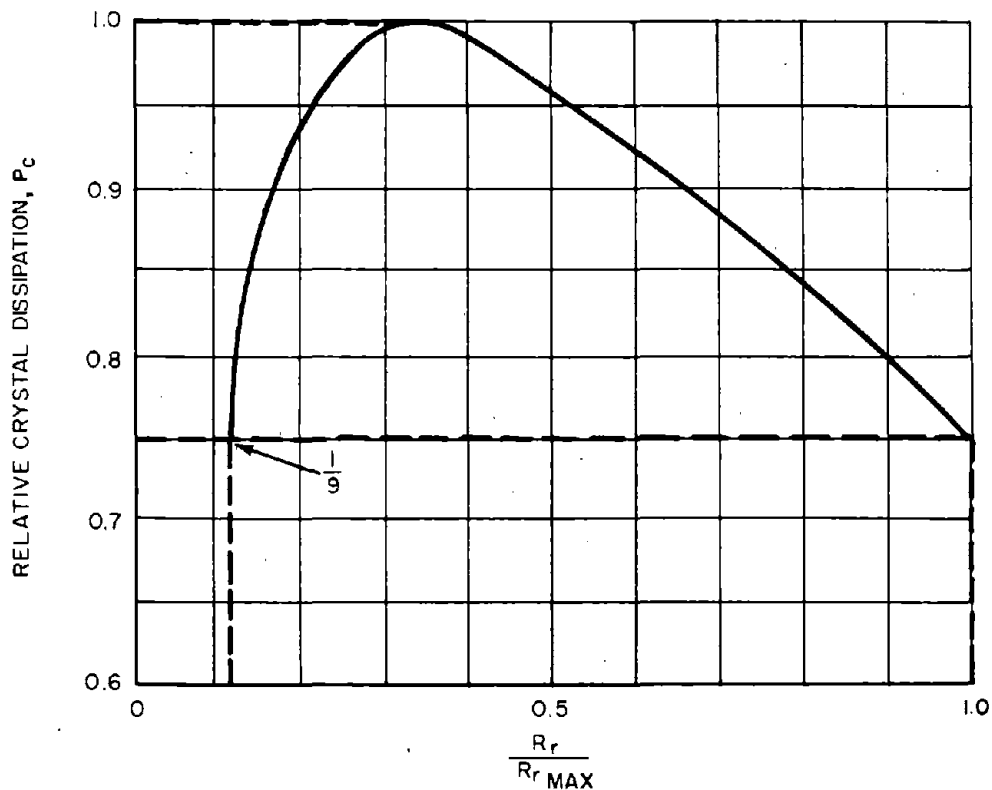
The maximum crystal unit dissipation is then obtained when $R_r = \frac{1}{3} R_{r \text{ max}}$. That is:

$$P_{c \text{ max}} = \frac{3}{4} \frac{V^2}{R_{r \text{ max}}} \quad (1-74)$$

The relative dissipation at other values of R_r is obtained by normalizing P_c with respect to $P_{c \text{ max}}$. Dividing Equation (1-73) by Equation (1-74) gives:

$$\frac{P_c}{P_{c \text{ max}}} = \frac{4}{3} \frac{R_{r \text{ max}} \cdot R_r}{\left(\frac{1}{3} R_{r \text{ max}} + R_r\right)^2} \quad (1-75)$$

Substituting various relative values of R_r into Equation (1-75) gives the plot of Figure 1-16 which shows that a 25 percent variation in P_c will occur over the assumed 9-to-1 range of R_r under the specified conditions.



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Figure 1-16. Crystal Dissipation Curve when $R_i = \frac{1}{3} R_r \text{ max}$

In practice, as crystal units are interchanged in an oscillator circuit, the loop gain will increase for decreasing values of R_r . This will cause an increase in oscillator output voltage and crystal unit driving source voltage with decreasing R_r , since the crystal unit driving source voltage will be directly proportional to the oscillator output voltage. The values of V_{max} given by Equations (1-70) and (1-72) apply when R_r is less than its maximum value and, consequently, when the loop gain is high. Therefore, when determining amplifier bias levels for a worst-case design, the crystal unit drive source voltage used in the calculations must be less than the values given by Equations (1-70) and (1-72). Reducing V_{max} 20 percent below the calculated value will usually prove sufficient.

Power supply voltage variations will also influence the oscillator output voltage and should also be taken into account. As a general rule, the oscillator output voltage will increase by the same percentage as the B+ voltage increase.

This analysis assumes that the amplifier input resistance remains constant as the loop gain increases. This is normally a justifiable assumption when the oscillator uses a vacuum tube amplifier, since the grid-base of the tube is normally large compared to the signal levels appearing there. However, when

a transistor amplifier is used, the signal level may easily exceed the linear signal handling capability of the emitter-base junction and the assumption of a constant amplifier input resistance is not justifiable. The input resistance of an overdriven transistor amplifier is difficult to estimate except in the most general terms, since it depends on the transistor current and voltage bias levels and the amplifier output signal voltage. The effect of overdrive is to increase the average amplifier input resistance, since the emitter-base diode is effectively reverse-biased over a portion of the signal period. Because of the highly non-linear characteristics of the junction, the increase is quite marked; average input resistance of 10 or more times the small signal input resistance occurring for loop voltage gains of 3. Insofar as crystal unit power dissipation is concerned, the increase in amplifier input resistance means that the maximum crystal unit dissipation will occur at a larger value of R_T , permitting the crystal drive source voltage to be larger than the values given by Equations (1-70) and (1-72). This, in turn, allows an increase in amplifier output voltage and oscillator output power. This effect is further discussed in Section VI where an attempt is made to estimate the allowable crystal unit drive voltage under these conditions.

1-10. CRYSTAL π NETWORK

In certain frequency ranges, a simple oscillator configuration results when the amplifier uses a grounded cathode tube or a grounded emitter transistor and an anti-resonance crystal unit in a phase inverting feedback network. The feedback network consists of a π network of the type shown in Figure 1-17; and when the value of C_T , C_L , and C_S are appropriately selected, the loading of the crystal unit by the driving source and the output load can be reduced to negligible proportions.

The purpose of the following analysis is to investigate these loading effects and to develop suitable design equations for the crystal π network.

1-11. Crystal π Network Analysis

The generalized form of the π network is shown in Figure 1-17 (a). This circuit shows the driving source and its output resistance R and the π network terminating load Z_1 . R can be regarded as the amplifier total output resistance (reactive component tuned out) including the oscillator load resistance R_L , Z_1 is the amplifier input impedance, and C_L is included in series with the crystal to provide a method of adjusting the impedance level of the network.

If it is assumed that Z_1 , the load across crystal π network, is negligibly large compared to X_{C_S} , the simplified network is as shown in Figure 1-17 (b) when the crystal is replaced by its series equivalent circuit. This assumption

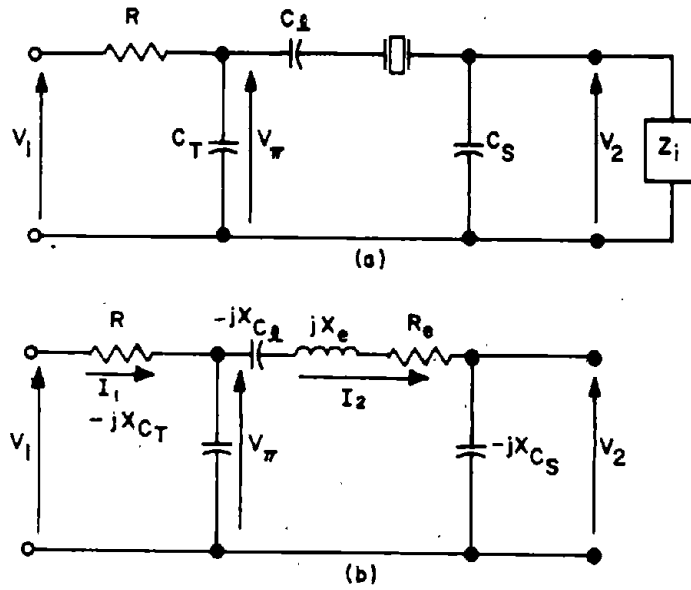


Figure 1-17. Equivalent Circuits of a Crystal Network and its Driving Source

concerning Z_i simplifies the analysis and does not invalidate the results, provided that the crystal loading and the network phase angle modifying effects of Z_i are otherwise introduced into the analysis. The assumption is also made that the effective inductance of the crystal is a linear function of frequency and that its effective resistance is constant over the small frequency range of interest.

The equations for the network of Figure 1-17 are:

$$V_1 = I_1 (R - jX_{C_T}) + I_2 \cdot jX_{C_T} \quad (1-76)$$

$$0 = I_1 \cdot jX_{C_T} + I_2 \left[R_e + j(X_e - X_{C_1} - X_{C_T} - X_{C_S}) \right] \quad (1-77)$$

$$V_2 = -I_2 \cdot jX_{C_S} \quad (1-78)$$

Solving for V_2 gives:

$$A_V = \frac{V_2}{V_1} = - \frac{X_{C_T} \cdot X_{C_S}}{R_e \cdot R + X_{C_T} (X_e - X_{C_S} - X_{C_1}) + j \left[R(X_e - X_{C_T} - X_{C_S} - X_{C_1}) - R_e \cdot X_{C_T} \right]} \quad (1-79)$$

When the phase angle approaches 180 degrees, Equation (1-79) can be approximated as:

$$A_V \approx - \frac{X_{C_T} \cdot X_{C_S}}{R_e \cdot R + X_{C_T} (X_e - X_{C_S} - X_{C_\ell})} \quad (1-80)$$

The term $(X_e - X_{C_S} - X_{C_\ell})$ is the effective inductance X_{Leff} of the circuit to the right of C_T in Figure 1-17 (b). That is:

$$X_{Leff} = X_e - X_{C_S} - X_{C_\ell} \quad (1-81)$$

The condition required for the imaginary component in the denominator to cancel is:

$$R (X_{Leff} - X_{C_T}) = R_e \cdot X_{C_T} \quad (1-82)$$

Equation (1-82) can be rearranged in the form:

$$\frac{R}{R_e} = \frac{X_{Leff}}{R_e} \cdot \frac{R}{X_{C_T}} - 1 \quad (1-83)$$

Substituting Equation (1-81) into Equation (1-82) and rearranging gives:

$$A_V = - \frac{X_{C_S}}{X_{Leff}} \cdot \frac{1}{\left[1 + \frac{R}{X_{C_T}} \cdot \frac{R_e}{X_{Leff}} \right]} \quad (1-84)$$

The phase angle of V_2 relative to V_1 , over and above the 180-degree phase inversion, is obtained from Equation (1-79) as:

$$\tan \phi = \frac{R (X_e - X_{C_S} - X_{C_\ell} - X_{C_T}) - R_e \cdot X_{C_T}}{R \cdot R_e + X_{C_T} (X_e - X_{C_S} - X_{C_\ell})} \quad (1-85)$$

Over the small frequency range of operation, the reactances X_{C_T} , X_{C_S} , and X_{C_ℓ} can be considered as constants. Consequently, X_e can be regarded as the only frequency dependent term, and differentiating with respect to X_e is equivalent to differentiating with respect to frequency.

That is:

$$\frac{d\phi}{df} = \frac{d\phi}{dX_e} \cdot \frac{dX_e}{df} = K \frac{d\phi}{dX_e} \quad (1-86)$$

where K is a constant in the small frequency range under discussion.

From Equation (1-85):

$$\begin{aligned} \frac{d(\tan \phi)}{dX_e} &= \frac{1}{R_e} \left[\frac{1}{1 + \frac{X_{C_T}}{R} \cdot \frac{X_{Leff}}{R_e}} \right] \\ &\propto \left\{ 1 - \frac{X_{C_T}}{R} \left[\frac{R(X_e - X_{C_T} - X_{C_S} - X_{C_L}) - R_e \cdot X_{C_T}}{R_e \cdot R + X_{C_T} (X_e - X_{C_S} - X_{C_L})} \right] \right\} \quad (1-87) \end{aligned}$$

But:

$$\frac{d(\tan \phi)}{dX_e} = \frac{d\phi}{dX_e} \frac{d(\tan \phi)}{d\phi} = \frac{d\phi}{dX_e} \cdot \sec^2 \phi \quad (1-88)$$

Therefore:

$$\begin{aligned} \frac{d\phi}{dX_e} &= \frac{\cos^2 \phi}{R_e} \left[\frac{1}{1 + \frac{X_{C_T}}{R} \cdot \frac{X_{Leff}}{R_e}} \right] \\ &\propto \left\{ 1 - \frac{X_{C_T}}{R} \left[\frac{R(X_e - X_{C_T} - X_{C_S} - X_{C_L}) - R_e \cdot X_{C_T}}{R_e \cdot R + X_{C_T} \cdot X_{Leff}} \right] \right\} \quad (1-89) \end{aligned}$$

The factors of Equation (1-89) are denoted as (1), (2), and (3) for the purposes the succeeding discussion.

1-12. Crystal Loading Due to R

To find the loading effect of R, it is first necessary to find the minimum value of $d\phi/dX_e$ that can be obtained in the circuit.

The maximum value of $d\phi/dX_e$ is obtained when R becomes very large (no crystal loading due to the driving source). Then:

$$\frac{d\phi}{dX_e} (\max) = \frac{1}{R_e} \cos^2 \phi \quad (1-90)$$

The crystal loading due to R is therefore minimized as factors (2) and (3) approach 1 and as ϕ approaches 0 degree.

A suitable value must be found for the reduction in the network $d\phi/dX_e$ below that of the crystal unit alone. Further degradation will be incurred due to Z_i as will be shown later, and a circuit $d\phi/dX_e$ degradation (due to R) to 75 percent of that of the crystal unit alone when R_e has its maximum value $R_{e \max}$ is considered suitable.

Another factor must also be considered. Factor (1) shows that a large deviation of the input-output voltage phase angle from 180 degrees will cause a large degradation of circuit $d\phi/dX_e$, in addition to those due to R and Z_i . For example, a phase deviation of 10 degrees causes a 3 percent reduction, 20 degrees in 11 percent reduction, and 30 degrees a 25 percent decrease. Clearly a phase angle of less than 20 degrees is desirable because of this effect. Assuming a maximum value of ϕ of ± 10 degrees and noting that the bracketed term of factor (3) is $\tan \phi$ (Equation 1-85) gives the following equation for the normalized degradation:

$$\begin{aligned} \frac{\frac{d\phi}{dX_e}}{\frac{d\phi}{dX_e} (\max)} &= 0.75 \\ &= \frac{1 - 0.176 \frac{X_{CT}}{R}}{1 + \frac{X_{CT}}{R} \cdot \frac{X_{Leff}}{R_{e \max}}} \end{aligned} \quad (1-91)$$

Values of $X_{Leff}/R_{e \max}$, X_{CT}/R , and $R/X_{CT} \cdot R_{e \max}/X_{Leff}$ which simultaneously satisfy the equality of Equation (1-91) are given in Table 1-7 for values of $X_{Leff}/R_{e \max}$ from 0.5 to 30. Reference to Table 1-7 and Equation (1-84) shows that the voltage attenuation then lies between the limits:

$$\frac{X_{CS}}{5.5 X_{Leff}} < |A_V| < \frac{X_{CS}}{4 X_{Leff}} \quad (1-92)$$

in order to satisfy the given loading conditions.

TABLE 1-7. NETWORK COMPONENT RATIOS RESULTING IN A 25-PER-CENT $\frac{d\phi}{dX_e}$ REDUCTION

$\frac{X_{Leff}}{R_{e \max}}$	$\frac{X_{CT}}{R}$	$\frac{R}{X_{CT}} \cdot \frac{R_{e \max}}{X_{Leff}}$
0.5	0.45	4.45
1	0.27	3.7
2	0.15	3.32
4	0.08	3.16
8	0.041	3.05
12	0.028	3.03
20	0.016	3.02
30	0.011	3.02

1-13. Effect of Output Load Z_i

As shown subsequently, the input impedance of a phase inverting amplifier can be considered as a parallel combination of resistance $R_{in(p)}$ and capacitance $C_{in(p)}$ which for the purpose of this analysis become R_i and C_i . Introducing Z_i into the crystal π network requires certain conditions to be met if the preceding analysis is to remain valid.

1-14. Effect of C_i

The presence of C_i established a minimum limit to the value of C_S . Since the voltage attenuation of the π network is proportional to X_{CS} , C_i may therefore influence the minimum realizable value of A_V in the absence of more stringent limitation by R_i . The latter condition normally applies for transistor amplifiers.

1-15. Effect of R_i

The presence of R_i in parallel with C_S results in both additional crystal loading and an additional phase shift of V_2 relative to V_1 . The impedance across which the output voltage V_2 appears is now:

$$Z = \frac{R_i}{1 + j \frac{R_i}{X_{CS}}} = \frac{-jX_{CS}}{1 - j \frac{X_{CS}}{R_i}} \quad (1-93)$$

The output voltage is then:

$$V_2 = I_2 Z = \frac{-jX_{CS}}{1 - j \frac{X_{CS}}{R_i}} \cdot I_2 \quad (1-94)$$

Comparison of Equation (1-94) with Equation (1-78) shows that the presence of R_i has reduced the phase of angle V_2 relative to I_2 , from -90 degrees to a value:

$$\phi_{V_O} = - (90^\circ - \tan^{-1} \frac{X_{CS}}{R_i}) \quad (1-95)$$

This reduction of ϕ_{V_O} is equivalent to an additional phase lead of the π network and will be beneficial when the amplifier has a phase lag. It should not, however, be allowed to become too large, since any phase lead greater than that of the amplifier phase lag will require a compensating phase lag of I_2 . And if this becomes excessive, a reduction in $d\phi/dX_e$ will occur as shown by the $\cos^2\phi$ term of Equation (1-89). A maximum value of 10 degrees therefore appears to be a reasonable compromise for $\tan^{-1} X_{CS}/R_i$ when the phase angle is the controlling factor. This gives:

$$X_{CS} \leq \frac{R_i}{6} \quad (1-96)$$

However, this does not take into account the crystal loading due to R_i . The parallel-to-series transform of R_i and X_{CS} results in a resistance r_i in series with the crystal unit equal to:

$$r_i = \frac{R_i}{1 + \left(\frac{R_i}{X_{CS}}\right)^2} \quad (1-97)$$

Equation (1-96) shows that R_i/X_{CS} will be greater than 6 when the maximum phase angle condition is satisfied and, therefore, r_i can be approximated as:

$$r_i = \frac{(X_{CS})^2}{R_i} \quad (1-98)$$

In the π network, r_i is in series with R_e and effectively increases the value of R_e to be used in Equation (1-89). This will result in a further reduction in

$d\phi/dX_e$, and a limit must be placed on this effect. Bearing in mind the 25-percent reduction due to R when R_e equals $R_{e \text{ max}}$ and possibly as much as 5 percent due to input phase angle deviations, a suitable limit to place on loading due to r_i would be 10 percent. That is:

$$r_i \leq 0.1 R_{e \text{ max}} \quad (1-99)$$

Substituting this value of r_i into Equation (1-98) and transposing gives:

$$X_{C_S} \leq \sqrt{0.1 R_{e \text{ max}} \cdot R_i} \quad (1-100)$$

The value of X_{C_S} must therefore have the smaller value given by Equation (1-96) or (1-100). Equating these shows that the transition occurs when:

$$R_i = 3.6 R_{e \text{ max}} \quad (1-101)$$

1-16. Crystal Unit Power Dissipation

This circuit is employed in two ways, and it is desirable to know the power dissipation in relationship to both V_1 and V_π .

(a) Relative to V_1

Neglecting r_i as small compared to R_e the crystal unit power dissipation P_C can be obtained by substituting in terms of I_2 for V_2 in Equation (1-84). When V_1 and I_2 approach 90 degrees:

$$|I_2| = \frac{V_1}{X_{\text{Leff}} \left[1 + \frac{R}{X_{C_T}} \cdot \frac{R_e}{X_{\text{Leff}}} \right]} \quad (1-102)$$

Then:

$$P_C = |I_2|^2 R_e = \frac{V_1^2 R_e}{(X_{\text{Leff}})^2 \left[1 + \frac{R}{X_{C_T}} \cdot \frac{R_e}{X_{\text{Leff}}} \right]^2} \quad (1-103)$$

Differentiating P_C with respect to R_e shows that the maximum crystal dissipation occurs when:

$$\frac{R}{X_{C_T}} \cdot \frac{R_e}{X_{\text{Leff}}} = 1 \quad (1-104)$$

Bearing in mind the possible 9-to-1 range of values of R_e , the condition given by Equation (1-104) will occur if:

$$\frac{R}{X_{CT}} \cdot \frac{R_{e \max}}{X_{Leff}} \leq 9 \quad (1-105)$$

Table 1-7 shows that this condition is satisfied for all $X_{Leff}/R_{e \max}$ values exceeding 0.5. Therefore, the maximum crystal dissipation will be:

$$P_{C \max} = \frac{V_1^2}{4} \cdot \frac{R_e}{(X_{Leff})^2} \quad (1-106)$$

The value of R_e that satisfies Equation (1-104) can be obtained from Table 1-7, Column 3, in terms of $R_{e \max}$. This shows that for all values of $X_{Leff}/R_{e \max}$ greater than 0.5, the range of values of R_e that results in the equality given by Equation (1-104) is:

$$\frac{R_{e \max}}{4.45} \leq R_e \leq \frac{R_{e \max}}{3} \quad (1-107)$$

Equation (1-107) shows that the value of R_e at which maximum crystal unit dissipation occurs does not vary greatly, and using a value of R_e equal to 0.274 $R_{e \max}$ in Equation (1-106) will result in an error of less than 20 percent in $P_{C \max}$ for all values of $X_{Leff}/R_{e \max}$ greater than 0.5. The maximum value of V_1 that does not overdrive the crystal can now be obtained from Equation (1-106) by substituting for R_e and for the crystal unit dissipation rating $P_{C \max}$ as:

$$\begin{aligned} V_{1 \max} &= 2 \sqrt{P_{C \max} \cdot \frac{(X_{Leff})^2}{0.27 R_{e \max}}} \\ &= 3.8 \cdot \frac{X_{Leff}}{R_{e \max}} \sqrt{P_{C \max} \cdot R_{e \max}} \end{aligned} \quad (1-108)$$

Equation (1-108) shows that the maximum allowable input voltage is directly proportional to the value of $X_{Leff}/R_{e \max}$ used, all other terms in the expression being constant for a given crystal type and frequency.

(b) Relative to V_π

In one method of operation, R will be the combined resistance of the oscillator external load R_L and the amplifier output resistance $R_{o(p)}$ in parallel. The value of R (R_L in this case) is determined by

the crystal loading, which therefore indirectly determines the minimum value of R_L and the possible oscillator power output as shown in the following analysis.

In an oscillator circuit, it is desirable that the output power be independent of changes in crystal characteristics. Therefore, one design object is to develop a certain amplifier output voltage, which in this case is also the voltage across C_T , which is compatible with the crystal dissipation rating for all possible values of R_e , and to maintain this voltage level constant independent of variations in R_e . The resistive component R_π , reflected across the terminals of C_T by the crystal equivalent resistance R_e , is given by a series-to-parallel transformation as:

$$R_\pi = R_e \left[1 + \left(\frac{X_{Leff}}{R_e} \right)^2 \right] \quad (1-109)$$

Because of the 9-to-1 variation of R_e between crystal units, the value of R_π is a variable and will have a minimum value when R_e is at maximum and vice-versa. The minimum value of R_π is obtained by substituting R_e equals $R_{e \max}$ into Equation (1-109) giving:

$$R_{\pi \min} = R_{e \max} \left[1 + \left(\frac{X_{Leff}}{R_{e \max}} \right)^2 \right] \quad (1-110)$$

Similarly, the maximum value of R_π is:

$$R_{\pi \max} = \frac{R_{e \max}}{9} \left[1 + \left(\frac{9 X_{Leff}}{R_{e \max}} \right)^2 \right] \quad (1-111)$$

The crystal unit power dissipation is equal to:

$$P_C = \frac{V_\pi^2}{R_\pi} \quad (1-112)$$

where V_π is the voltage across C_T . Therefore, for a given V_π , the crystal dissipation will be greatest when R_π has its smallest value. The maximum allowable value of V_π when R_e equals $R_{e \max}$ is then:

$$\begin{aligned} V_{\pi A} &= \sqrt{P_{C \max} \cdot R_{\pi \min}} \\ &= \sqrt{P_{C \max} \cdot R_{e \max} \left[1 + \left(\frac{X_{Leff}}{R_{e \max}} \right)^2 \right]} \end{aligned} \quad (1-113)$$

or, transposing:

$$P_{C \text{ MAX}} = \frac{V_{\pi A}^2}{R_{e \text{ max}} \left[1 + \left(\frac{X_{L \text{ eff}}}{R_{e \text{ max}}} \right)^2 \right]} \quad (1-114)$$

But $V_{\pi A}$ is the voltage across R_L , and therefore the output power is:

$$P_L = \frac{V_{\pi A}^2}{R_L} \quad (1-115)$$

If it is assumed that $R_{o(p)}$ is much greater than R_L , R_L then replaces R in the crystal loading equations previously derived. Substituting for R and $R_{e \text{ max}}$ in Equation (1-83) gives:

$$\frac{R_L}{R_{e \text{ max}}} = \frac{X_{L \text{ eff}}}{R_{e \text{ max}}} \cdot \frac{R_L}{X_{C_T}} - 1 \quad (1-116)$$

Substituting for R_L in Equation (1-115) from Equation (1-116) and dividing Equation (1-115) by Equation (1-114) gives:

$$\frac{P_L}{P_{C \text{ MAX}}} = \frac{1 + \left(\frac{X_{L \text{ eff}}}{R_{e \text{ max}}} \right)^2}{\frac{X_{L \text{ eff}}}{R_{e \text{ max}}} \cdot \frac{R_L}{X_{C_T}} - 1} \quad (1-117)$$

Figure 1-18 is a plot of Equation (1-117) for values of $X_{L \text{ eff}}$, $R_{e \text{ max}}$, R_L , and X_{C_T} compatible with the previously derived crystal loading conditions. It shows that the allowable load power can be considerably greater than the crystal dissipation rating for $X_{L \text{ eff}}/R_{e \text{ max}}$ values less than 1; and that for values greater than 2, the allowable load power is only slightly more than one-third of the crystal dissipation rating. It will subsequently be shown that operation with $X_{L \text{ eff}}/R_{e \text{ max}}$ values less than 1 results in poor oscillator power conversion efficiency and that this type of oscillator is most suitable when output powers of less than $P_{C \text{ max}}$ are desired.

This relationship was derived, assuming that the amplifier output resistance was much greater than the load resistance. This condition results in the maximum power output; and when the amplifier output resistance cannot be ignored, the allowable oscillator output power will be correspondingly reduced.

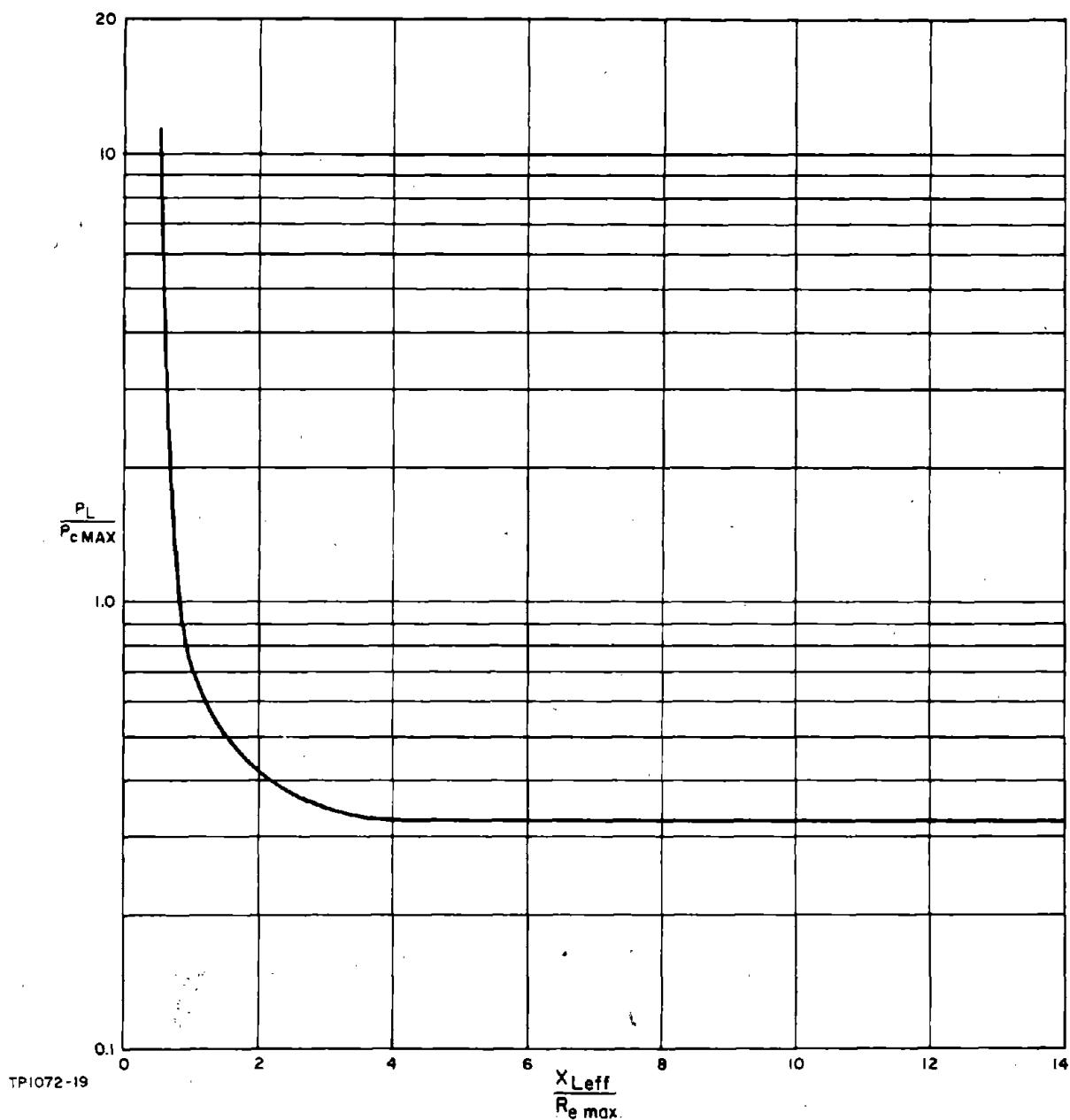


Figure 1-18. Ratio of Oscillator Output Power Relative to Crystal Dissipation Rating as a Function of $X_{L\text{ eff}}/R_{e\text{ max}}$

SECTION 2

APPLICATION OF QUARTZ CRYSTALS TO OSCILLATOR DESIGN

2-1. GENERAL

In the preceding section it was demonstrated that, provided certain conditions of usage are observed, the quartz crystal has the high rate of change of phase angle, and the insensitivity to external disturbances, desirable in the frequency controlling element of an oscillator. Because of these conditions, the introduction of the crystal unit into the oscillator circuit requires careful consideration, and this is the purpose of the following discussion.

2-2. GENERALIZED OSCILLATOR BLOCK DIAGRAM

From the discussion in the Introduction, it can be seen that the essential circuits of an oscillator are a power amplifying device and a feedback network which extracts a portion of the amplifier output power and returns it to the amplifier input. Consideration of this circuit and the operating characteristics of the crystal unit leads to certain conclusions regarding the placement of the crystal unit in the circuit and the nature of the network that will be required to terminate the crystal unit. These are:

- (a) In Sections 1-8 and 1-11 it was shown that to avoid reducing the crystal $\frac{d\phi}{df}$ characteristics unduly, the power transfer between the input and output of the crystal unit, or the network in which it is incorporated, should be inefficient. That is, the power available at the output side of the crystal or crystal network should be small compared to the power dissipation in the crystal unit. In view of the limited power dissipation capabilities of the crystal and the desirability of minimizing the dissipation, it follows that the crystal should be inserted into the oscillator circuit at the minimum power level point. Simple reasoning shows that this occurs at the input of the amplifier which is, therefore, the logical position for the crystal or the crystal network.
- (b) It was also shown in Sections 1-8 and 1-11 that the crystal terminating impedance levels should be compatible with those of the crystal unit if its high rate of change of phase angle with frequency characteristic is to be maintained. In general, neither the input or output impedance levels of the power amplifier will meet this requirement, and passive networks having impedance transforming properties may need to be interposed between the crystal unit and both the amplifier input and output. The purpose of these networks is to reflect the

amplifier input and output impedances at compatible levels into the crystal or crystal network.

- (c) That portion of the amplifier output power to be fed back to the amplifier input, P_{FB} , is conveniently derived in parallel with that fed to the external load, P_L . The same signal voltage is then across both feedback network and load, and the power division between them is therefore dependent on the relative values of the parallel equivalent resistances of the feedback network and the oscillator load. In most cases, it is desirable that the power division should favor the external load (provided that the loop gain condition is still satisfied), and it may then be necessary to introduce an impedance transforming network at the input of the feedback network to obtain the requisite power division. Generally, this function can be combined with that of the impedance transforming network giving compatible matching between crystal and amplifier output.

2-3. OSCILLATOR GAIN RELATIONSHIPS

From the preceding discussion it is possible to construct the more detailed oscillator block diagram shown with the loop broken in Figure 2-1 and to determine the power and voltage relationships. In this circuit the loop gain is assumed to be 1 and the power transfer efficiencies E , the voltage attenuations $A_v \angle \phi$, the power gain G_p , and the voltage gain $G_v \angle \phi$ of the various blocks are those applying when each block is terminated in the succeeding block as shown. The reactive components of the feedback network and the oscillator load are also assumed to be tuned out. The total amplifier output power is then:

$$P_T = E_1 \cdot E_2 \cdot E_3 \cdot G_p \cdot P_{FB} = G'_p \cdot P_{FB} \quad (2-1)$$

where

$$G'_p = E_1 \cdot E_2 \cdot E_3 \cdot G_p \quad (2-2)$$

and

$$P_T = P_L + P_{FB} \quad (2-3)$$

Substituting for P_T from Equation (2-3) into Equation (2-1) and transposing gives:

$$\frac{P_L}{P_{FB}} = G'_p - 1 \quad (2-4)$$

Since the power dissipations P_L and P_{FB} occur in parallel resistive loads R_L and R_{FB} , respectively:

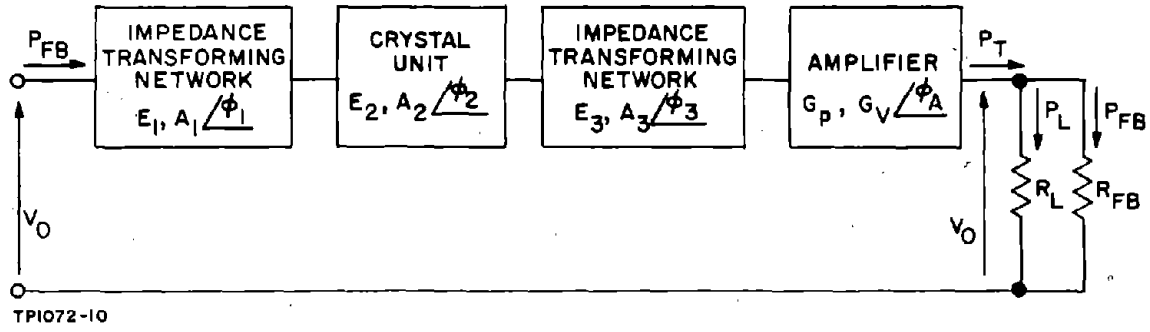


Figure 2-1. Generalized Oscillator Block Diagram

$$\frac{P_L}{P_{FB}} = \frac{V_O^2}{R_L} \bigg/ \frac{V_O^2}{R_{FB}} = \frac{R_{FB}}{R_L} \quad (2-5)$$

Therefore,

$$\frac{R_{FB}}{R_L} = G'_p - 1 \quad (2-6)$$

Similarly, from Equation (2-1):

$$G'_p = \frac{P_T}{P_{FB}} = \frac{V_O^2}{R_T} \bigg/ \frac{V_O^2}{R_{FB}} \quad (2-7)$$

where

$$R_T = \frac{R_{FB} \cdot R_L}{R_{FB} + R_L} \quad (2-8)$$

Therefore,

$$\frac{R_{FB}}{R_T} = G'_p \quad (2-9)$$

Dividing Equation (2-9) by Equation (2-6) gives:

$$\frac{R_L}{R_T} = \frac{G'_p}{G'_p - 1} \quad (2-10)$$

The voltage gain expression is:

$$V_O = A_1 \cdot A_2 \cdot A_3 \cdot G_v \cdot V_O \bigg/ \phi_1 + \phi_2 + \phi_3 + \phi_A \quad (2-11)$$

or

$$A_1 \cdot A_2 \cdot A_3 \cdot G_v = 1 \quad (2-12)$$

and

$$\phi_1 + \phi_2 + \phi_3 + \phi_A = 0, 2\pi \text{ rads, etc.}$$

Equation (2-4) defines the ratio between oscillator output and feedback power and shows that it is dependent on the net power gain of all the oscillator blocks. It also determines the maximum power output of the oscillator, since the maximum feedback power will be limited by the permissible crystal unit dissipation. Equation (2-6) expresses this in another way, showing the maximum value of R_{FB} that can be employed for a given net gain. Equations (2-9), (2-10), and (2-12) are also useful in oscillator design calculations.

These equations are all derived for a loop gain of 1. In a practical oscillator it is desirable that the loop gain under small signal conditions should be greater than 1 so that minor gain reductions due to any cause will not result in the cessation of oscillation. It is also advantageous up to a point in stabilizing the oscillator output power; a topic that will be discussed later. A loop power gain of 2 or 3 seems to be generally suitable, and this can be introduced into the preceding equations by assigning to G_p or G'_p a value of $1/2$ to $1/3$ of its actual value; or, if the voltage relationships are to be used, by decreasing G_v to $\frac{G_v}{\sqrt{2}}$ or $\frac{G_v}{\sqrt{3}}$.

The use of these equations can be demonstrated by an idealized design example of a series resonance oscillator. The following circuit conditions are assumed: The amplifier power gain is 200 when $R_T = 1K$ and has zero phase shift between input and output. The amplifier input impedance is resistive and has a value of 20 ohms. The crystal resonance resistance R_r is 80 ohms.

The amplifier input resistance is sufficiently low that an impedance transforming network will not be required between the crystal unit and the amplifier input, and the crystal unit can be directly connected to the amplifier input. The power transfer efficiency between the crystal unit input and output will be:

$$E_c = \frac{R_{in}}{R_{in} + R_r} = 0.2 \quad (2-13)$$

The net gain from the crystal unit input to the amplifier output, calculating on the basis of a loop gain requirement of 2, is:

$$E_c \cdot \frac{G_p}{2} = 20 \quad (2-14)$$

The input resistance as viewed at the input terminal of the crystal unit is 100 ohms. This is considerably smaller than R_T , and an impedance transforming network

will be required between the amplifier output and the crystal unit input terminal. Specifying the efficiency E_1 of this network as 0.75 gives a net loop gain of:

$$G'_p = E_1 \cdot E_c \cdot \frac{G_p}{2} = 15 \quad (2-15)$$

then:

$$R_L = \frac{G'_p}{G'_p - 1} \cdot R_T = 1.07 \text{ K} \quad (2-16)$$

$$R_{FB} = G'_p \cdot R_T = 15 \text{ K} \quad (2-17)$$

The impedance transformation ratio T_r required between amplifier output and crystal unit input is, therefore:

$$T_r = \frac{R_{FB}}{R_{in} + R_r} = 150 \quad (2-18)$$

Since this network will be passive, its impedance transforming properties will be reciprocal, and the resistance R facing the crystal unit at its input terminal will be:

$$R = \frac{1}{T_r} \cdot \frac{R_o \cdot R_L}{R_o + R_L} \quad (2-19)$$

where R_o is the effective parallel output resistance of the amplifier. Even if R_o is assumed to be infinite, R will be 6.7 ohms due to R_L , and therefore provides adequate terminating conditions for a crystal with a resonance resistance of 80 ohms. If the dissipation rating of the crystal unit $P_C \text{ MAX}$ is 2 MW, the maximum power output allowable before crystal overdrive occurs is found as follows:

The amplifier input power is:

$$P_{in} = \frac{R_{in}}{R_r} \cdot P_C \text{ MAX} = 0.5 \text{ MW} \quad (2-20)$$

then

$$P_{FB} = \frac{(P_C \text{ MAX} + P_{in})}{E_1} = 3.33 \text{ MW} \quad (2-21)$$

and

$$P_L = P_{FB} (G'_p - 1) \approx 47 \text{ MW} \quad (2-22)$$

This example could also have been given in terms of loop voltage gain.

In the preceding , the requirement for additional networks having impedance transforming properties has been determined, and general oscillator design equations have been developed. A further outcome is the added emphasis placed on the important characteristics of amplifiers and impedance transforming networks which need to be known before oscillator design calculations can be made. These characteristics which are subjects of Section 3 and 4, respectively, are:

- (a) The power or voltage gain, the phase angle, and the input and output impedance of the amplifier.
- (b) The power transfer efficiency, impedance transforming or voltage attenuation ratio, and the phase angle of the impedance transforming network.

SECTION 3 AMPLIFIER CHARACTERISTICS

3-1. GENERAL

As stated in Section 2 the amplifier characteristics of primary importance are the power or voltage gain, the input impedance, and the phase shift between input and output. Because the amplifier normally provides the limiting action that stabilizes the amplitude of oscillation, its operation in an oscillator circuit is non-linear, with the input impedance and voltage and power gain varying cyclically with the period of oscillation. The estimation of average values of input impedance and gain under these conditions would be difficult and, as it turns out for the simple types of oscillators discussed here, unjustified in view of the satisfactory results that can be achieved by simpler methods.

The approach used is to ignore the non-linear action of the amplifier, and to assume that the small signal gain and input impedance suffice to characterize the amplifier for oscillator design purposes. This simplification is justified in practice by the results obtained and also closely approaches the actual circuit operation when the loop gain is only slightly greater than 1. Additionally, it also accurately portrays the circuit conditions during the initial buildup of oscillation prior to the oscillation amplitude stabilization by the amplifier non-linearity. Therefore, the amplifier small signal gain and input impedance are appropriate design parameters when estimating the loop gain and phase shift which will allow oscillation to build up.

The following discussion presents appropriate formulae for the calculation of amplifier input impedance, power gain, voltage gain and, in some cases, output impedance for the frequency range where the amplifier characteristics are amenable to calculation. For both transistor and vacuum tube amplifiers this range extends from zero frequency to possibly 10 to 40 MC, depending on amplifier configuration. Above this range the amplifier characteristics become increasingly complex, and simple formulae no longer give sufficient accuracy for design purposes. An experimental approach is then preferable, and experimentally derived data are presented to provide background information which will allow the effects of active device bias level changes to be estimated.

In the following discussion, design equations which are commonly available from textbooks are given without derivation.

3-2. VACUUM TUBE CHARACTERISTICS AT LOW FREQUENCIES

At low frequencies, reasonably accurate estimations of gain and input impedance can be obtained from the equivalent circuits of Figure 3-1 and the

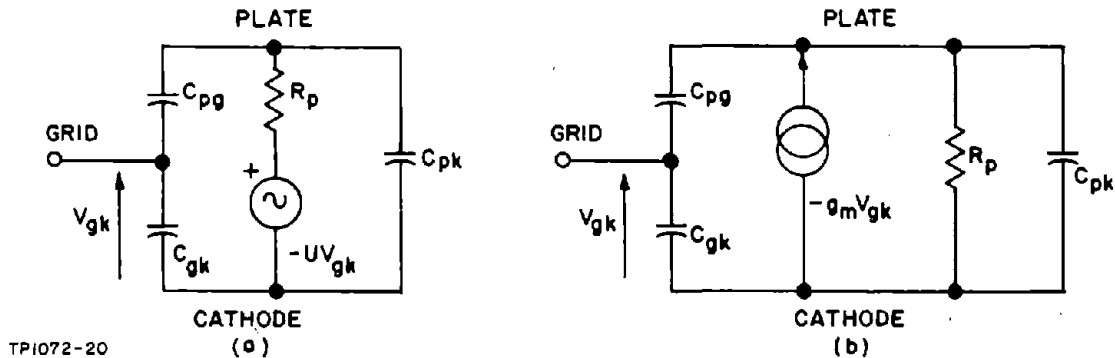


Figure 3-1. Vacuum Tube Equivalent Circuits

parameter values quoted in the manufacturer's data sheets. For the general purpose type of miniature and subminiature vacuum tube, this equivalent circuit adequately represents the performance of the device up to frequencies of 20 to 50 MC, depending on amplifier configuration. Above this frequency range parasitic reactance, notably cathode lead inductance, becomes a dominating factor in the behavior of the tube, and the equations derived from the simple circuits of Figure 3-1 no longer apply.

3-3. Design Equations for Triode Amplifiers at Low Frequencies

a. Grounded Cathode Triode Amplifier

When the plate circuit is tuned to resonance or at frequencies where the load and tube reactances are large compared to the load resistance R_T , the following equations are applicable:

The voltage gain is:

$$G_V = - \frac{U R_T}{R_T + R_p} \quad (3-1)$$

The tube input impedance is:

$$C_{in(p)} = (G_V + 1) C_{pg} + C_{gk} + C \text{ (strays)} \quad (3-2)$$

where $(G_V + 1) C_{pg}$ is the "Miller" capacitance.

This is the input impedance of the tube alone, and a grid leak resistor R_g will be necessary. The total input impedance therefore consists of $C_{in(p)}$ and R_g in parallel. For the tubes suitable for oscillator applications, the maximum value of R_g is normally specified as 1 megohm and occasionally as 2 megohms. The output impedance is R_p in parallel with C_{pg} and C_{pk} .

The power gain is:

$$G_p = G_V^2 \cdot \frac{R_g}{R_T} = \frac{U^2 \cdot R_T \cdot R_g}{(R_T + R_p)^2} \quad (3-3)$$

In the frequency range where these equations apply, the phase angle between input and output voltage is essentially 180 degrees when the plate circuit is tuned to resonance.

b. Grounded Grid Triode Amplifier

With the same plate tuning conditions as for the grounded cathode amplifier, the following equations are applicable:

The voltage gain is:

$$G_V = \frac{(U + 1) R_T}{R_T + R_p} \quad (3-4)$$

The input impedance consists of two parallel components. The resistive component is:

$$R_{in(p)} = \frac{R_T + R_p}{U + 1} \quad (3-5)$$

The capacitive component is:

$$C_{in(p)} = C_{gk} + C(\text{strays}) - C_{pk}(G_V - 1) \quad (3-6)$$

where $C_{pk}(G_V - 1)$ is due to feedback via C_{pk} .

The feedback term will normally be large relative to C_{gk} and $C(\text{strays})$ unless special screening is provided within the tube, and the parallel input reactance will then be inductive. The output impedance is R_p in parallel with C_{pg} and C_{pk} .

The power gain is:

$$G_p = G_V^2 \cdot \frac{R_{in(p)}}{R_T} = \frac{(U + 1) R_T}{R_T + R_p} \quad (3-7)$$

In the frequency range where these equations apply, the phase angle between input and output voltage is essentially 0 degree when the plate circuit is tuned to resonance.

3-4. Design Equations for Tetrode or Pentode Amplifiers at Low Frequencies

a. Grounded Cathode Pentode or Tetrode Amplifier

When the plate circuit is tuned to resonance or at frequencies where the load and tube reactances are large compared to the load resistance, and when screen and suppressor grids are effectively decoupled to the cathode, the following equations are applicable.

The voltage gain is:

$$G_V = -g_m R_T \quad (3-8)$$

where

$$g_m = \frac{U}{R_p} \quad (3-9)$$

The input impedance consists of two parallel components. The reactive component is:

$$C_{in(p)} = C_{gk} + (G_V + 1) C_{pg} + C_{(strays)} \quad (3-10)$$

The resistive component is that of the grid leak resistor R_g which is usually specified as 1 megohm maximum for the type of tubes suitable for low power oscillators. The output impedance is R_p in parallel with C_p , the capacitance between the plate and all other electrodes.

The power gain is:

$$G_p = G_V^2 \cdot \frac{R_g}{R_T} = g_m^2 \cdot R_T R_g \quad (3-11)$$

In the frequency range where these equations apply, the phase angle between input and output voltage is essentially 180 degrees when the plate circuit is tuned to resonance.

b. Grounded Grid Pentode or Tetrode Amplifier

When the plate circuit is tuned to resonance or at frequencies where the load and tube reactances are large compared to the load resistance, and when the screen and suppressor grids are effectively decoupled to the cathode, the following equations are applicable:

The voltage gain is:

$$G_V = g_m R_T \quad (3-12)$$

The input impedance consists of two parallel components. The reactive component is:

$$C_{in(p)} = C_{gk} + C_{(strays)} - (G_V - 1) C_{pk} \quad (3-13)$$

The resistive component is:

$$R_{in(p)} = \frac{1}{g_m} \quad (3-14)$$

The output impedance is R_p in parallel with C_p . The power gain is:

$$G_p \approx G_V^2 \cdot \frac{R_{in}}{R_T} = g_m^2 R_T \cdot R_{in} \quad (3-15)$$

3-5. GROUNDED GRID TRIODES AT HIGH FREQUENCIES

At frequencies above 25 MC where only series resonance crystal units are available, the grounded grid triode amplifier configuration results in a simple oscillator circuit. Measurements made on grounded grid triode tuned amplifiers indicate that the low-frequency design equations given previously are reasonably accurate up to 200 MC, provided that suitable high-frequency tubes are selected and certain allowances are made. It is found that at frequencies above, say, 50 MC, the amplifier behaves as if the plate resistance of the tube is lower than would be expected from the low-frequency values usually given by the manufacturer. If the amplification factor is regarded as remaining equal to that at low frequencies, the g_m is effectively increased. This results in the amplifier voltage gain for a given total load resistance being greater than that calculated and the amplifier input resistance being less than that calculated. An example of this is the 8058 triode at 200 MC.

For a plate voltage of 85 VDC and a plate current of 10 MA, the data sheet gives $U = 70$, $R_p \approx 6$ K, and $g_m \approx 12$ MA/V. The short circuit input resistance should therefore be approximately 85 ohms. Actual measurement of the cathode input resistance with the plate AC short-circuited on a tube of this type at 200 MC gives a value of 52 ohms which, if U remains constant, gives $R_p \approx 3.7$ K. Similarly, the calculated amplifier voltage gain for a total load resistance of 2 K is 17.5 for the quoted biasing conditions, while measurement gave a voltage gain of 30 which, if U remains constant, indicates an R_p of approximately 2.7 K. The two values of R_p derived from measurements do not correlate, and it is obvious that the behavior is more complex than that attributable to a change

in R_p . Nevertheless, this simple concept does aid in understanding the amplifier behavior at high frequencies. At lower frequencies the effect is less severe and should be negligible below 75 MC for all high-frequency triodes.

The input reactance of high-frequency grounded grid triodes with the plate load tuned to resonance appears to be negligible compared to the resistive component. The input impedance can therefore be considered as being essentially resistive.

3-6. TRANSISTOR AMPLIFIERS

NOTE: This handbook is concerned with crystal oscillators operating over the temperature range of -55°C to $+105^{\circ}\text{C}$. The latter limit automatically rules out the use of germanium transistors and, consequently, the following discussion centers upon the use of silicon transistors. However, apart from the difference in dissipation ratings and the less stable biasing characteristics of the germanium transistor, the operating characteristics of both are essentially similar and the following discussion should be applicable to either type.

At frequencies less than a few megacycles, provided that suitably chosen transistors are used, the gain and input impedance of transistor amplifiers can be estimated using a simple equivalent circuit. At frequencies above a few megacycles, however, the characteristics of a transistor amplifier become increasingly complex. Even very high frequency transistors having alpha cutoff frequencies in excess of 1 KMC have marked input impedance phase angles above 10 MC. At these higher frequencies, then, there is no alternative but to accept and make use of the transistor in its more complicated mode of operation. However, below a few megacycles it is always possible by a suitable choice of transistor type to design an amplifier having essentially resistive characteristics.

Consideration of transistor amplifier behavior shows that three distinct categories exist in the frequency range up to 200 MC. These are:

- (a) Amplifiers in the frequency range up to, say, 100 KC. In this frequency range, virtually all of the more recent low-power dissipation transistors exhibit essentially resistive characteristics.
- (b) Amplifiers in the frequency range up to 5 MC. In general, above 100 KC the general purpose type transistors exhibit

complex frequency dependent characteristics. It is therefore advisable to use high-frequency transistor types characterized by gain-bandwidth products exceeding 100 MC in the frequency range from, say, 100 KC to a few megacycles. No price penalty is paid in doing this, and the advantage of an essentially resistive amplifier circuit described by simple equations is obtained. These types of transistors are, of course, equally applicable at frequencies below 100 KC.

- (c) Amplifiers in the frequency range from 5 MC to 200 MC. In this frequency range, only the high-frequency type transistors with gain-bandwidth products in excess of 200 MC are suitable for consideration. Cost is likely to be the determining factor here in the selection of a transistor type. In general, the higher cost transistors will be less frequency dependent to a higher frequency, since cost and gain-bandwidth product tend to increase in step.

The following discussion is arranged in the three categories described in (a), (b), and (c).

3-7. Transistor Amplifiers at Frequencies Below 100 KC

Virtually all recently introduced small-signal transistors have common-emitter current-gain cutoff frequencies in excess of 100 KC and behave as essentially resistive devices below this frequency. Consequently, practically any small-signal general-purpose transistor is suitable for use in oscillator designs in this frequency range. For these types of transistor, the manufacturer's data sheets most frequently quote the "h" or hybrid transistor parameters which are defined by Figure 3-2 and the following equations:

$$V_1 = (h_i \cdot I_1) + (h_r \cdot V_2) \quad (3-16)$$

$$I_2 = h_f \cdot I_1 + h_o \cdot V_2 \quad (3-17)$$

where

- h_i = Input resistance at 1, 1' with 2, 2' short-circuited
- h_r = Reverse voltage transfer ratio from 2, 2' to 1, 1' with terminals 1, 1' open-circuited
- h_f = Forward current transfer ratio from 1, 1' to 2, 2' with 2, 2' short-circuited
- h_o = Input resistance at 2, 2' with 1, 1' open-circuited

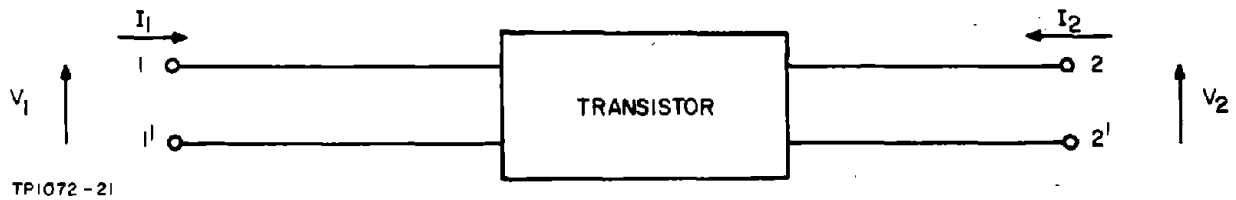


Figure 3-2. Transistor "Black Box"

Additional subscripts b, e, or c specify whether the parameters are those for the common-base, common-emitter, or common-collector configuration, respectively. For the purpose of design calculation, these parameters may be regarded as purely resistive in the frequency range under discussion. The base-emitter and base-collector capacitances have only a limited effect which can be remedied if necessary during the experimental stage of the oscillator design.

The transistor data sheets usually give typical values of these parameters in the grounded base configuration at a particular value of DC emitter or collector current, and for a particular value of DC voltage between collector-base or collector-emitter. In addition, graphs are given showing the change of the parameter values with emitter or collector current, collector-base or collector-emitter voltage, and with temperature. By using these graphs and the quoted typical parameter values, it is possible to estimate the typical parameter values over a wide range of current, voltage, and temperature.

The data sheets also usually specify the maximum and minimum values of h_{fe} , the common-emitter current gain, and frequently include this and the term $(1 + h_{fb})$ in the graphical information. For a given transistor type, the range of h_{fe} between minimum and maximum values is typically 3:1, and comparable variations of h_{ib} , h_{rb} , and h_{ob} can be expected.

3-8. Power Gain, Input and Output Resistance

The formulae for power gain, input resistance, and output resistance of a transistor in terms of the "h" parameters are:

$$G_p = \frac{h_f^2 \cdot R_T}{(1 + h_o \cdot R_T) [h_i + (h_i \cdot h_o - h_f \cdot h_r) R_T]} \quad (3-18)$$

where R_T = total load resistance

$$R_{in} = h_i - \frac{h_r \cdot h_f \cdot R_T}{1 + h_o \cdot R_T} \quad (3-19)$$

$$R_O = \frac{h_i + R_G}{h_i \cdot h_o - h_f \cdot h_r + h_o \cdot R_G} \quad (3-20)$$

where R_G = driving source resistance. The voltage gain is:

$$G_V = \frac{h_f \cdot R_T}{h_i (1 + h_o \cdot R_T) - h_f \cdot h_r \cdot R_T} \quad (3-21)$$

3-9. Common-Base to Common-Emitter 'h' Parameter Conversions

The transistor data sheets normally give the common-base parameters. To convert these to the common-emitter parameters, the following formulae are used:

$$h_{ie} = \frac{h_{ib}}{1 + \Delta b + h_{fb} - h_{rb}} \approx \frac{h_{ib}}{1 + h_{fb}} \quad (3-22)$$

$$h_{re} = \frac{\Delta b - h_{rb}}{1 + \Delta b + h_{fb} - h_{rb}} \approx \frac{\Delta b - h_{rb}}{1 + h_{fb}} \quad (3-23)$$

$$h_{fe} = \frac{(h_{fb} + \Delta b)}{1 + \Delta b + h_{fb} - h_{rb}} \approx \frac{-h_{fb}}{1 + h_{fb}} \quad (3-24)$$

$$h_{oe} = \frac{h_{ob}}{1 + \Delta b + h_{fb} - h_{rb}} \approx \frac{h_{ob}}{1 + h_{fb}} \quad (3-25)$$

where

$$\Delta b = h_{ib} \cdot h_{ob} - h_{rb} \cdot h_{fb} \quad (3-26)$$

The approximate formulae indicate the dependence of the common-emitter parameters on the term $(1 + h_{fb})$. The value of h_{fb} is within a few percent of -1. Consequently, when converting the parameters, small changes in the assumed value can radically affect the values obtained. Therefore, the power gain and impedance level calculations should only be regarded as indicative of the actual performance of the transistor, and experimental checks are desirable.

3-10. Typical Transistor Amplifier Operating Characteristics

The typical operating characteristics of small signal transistor amplifiers suitable for low-frequency oscillator service are:

a. Common-Base Amplifier

G_p = Up to 30 to 35 DB, depending on the degree of output matching

R_{in} = 30 to 150 ohms, depending on the total load resistance

R_o = 100 K to 2 MEGΩ, depending on the value of R_G

b. Common-Emitter Amplifier

G_p = Up to 45 DB, depending on the degree of output matching

R_{in} = 500 ohms to 5 K, depending on the total load resistance

R_o = 10 K to 100 K, depending on the value of R_G

3-11. Simplifications of G_p , R_{in} , and R_o Formulae

Various simplifications of these formulae can be made under certain conditions. If:

$$R_T \ll \frac{1}{h_o} \quad (3-27)$$

$$G_p \approx h_f^2 \cdot \frac{R_T}{h_i} \quad (3-28)$$

and

$$G_V \approx \frac{R_T}{h_{ib}} \quad (3-29)$$

$$R_{in} \approx h_i \quad (3-30)$$

These equations are usually applicable when $R_T \leq 60$ K for common-base operation and $R_T \leq 5$ K for common-emitter operation. Also, if:

$$R_G \gg h_i \quad (3-31)$$

then

$$R_o \approx \frac{1}{h_o} \quad (3-32)$$

Equation (3-31) is usually applicable when $R_G > 1$ K for common-base operation and $R_G > 15$ K for common-emitter operation.

3-12. Background Information on High-Frequency Transistors

The behavior of high-frequency transistor amplifiers is greatly influenced by the delay experienced by the signal in passing across the transistor junctions, and the feedback between output and input via the parasitic reactive elements associated with the semiconductor structure, the lead attachments, and the case. The criteria generally employed in judging the relative merits of high-frequency transistors are:

- (a) The gain-bandwidth product f_T . This quantity typifies the behavior of the common-emitter short-circuit current gain h_{fe} . It is found that above a certain frequency the product of h_{fe} and test frequency remains relatively constant. That is, h_{fe} decreases with an approximately 6 DB per octave slope as shown in Figure 3-3. The value of f_T quoted in the transistor data sheet therefore enables an estimate to be made of the h_{fe} at any frequency in the range above f_β , the cutoff frequency where the slope commences. Below f_β the low-frequency current gain h_{FE} applies.
- (b) Another quantity usually specified is the matched power gain at some high frequency, frequently either 200 or 500 MC, when the internal feedback within the transistor is completely cancelled (unilateralized) by equal and opposite external feedback. Above a certain frequency the unilateralized matched power gain also decreases with frequency of operation. Until recently this decrease was also considered to have a 6 DB per octave slope as shown in Figure 3-3, and often the frequency at which the unilateralized power gain equalled 1 (termed f_{osc}) was used as a figure of merit. This method of specification now appears to have fallen into disuse, presumably because of the inaccuracies involved. Matched power gains of from 8 to 20 DB at 200 MC are typical. Power gain and f_T tend to increase approximately in step.
- (c) The value of C_{ob} , the capacitance measured between collector and base with the emitter open-circuited and a reverse-bias voltage on the collector-base junction. This capacitance consists of two components: The stray capacitance associated with the leads and case, and that occurring at the semiconductor junction. The latter is an inverse function of the reverse-bias voltage applied to the collector-base junction and, consequently, the bias voltage must be specified for the stated value of C_{ob} to be meaningful.

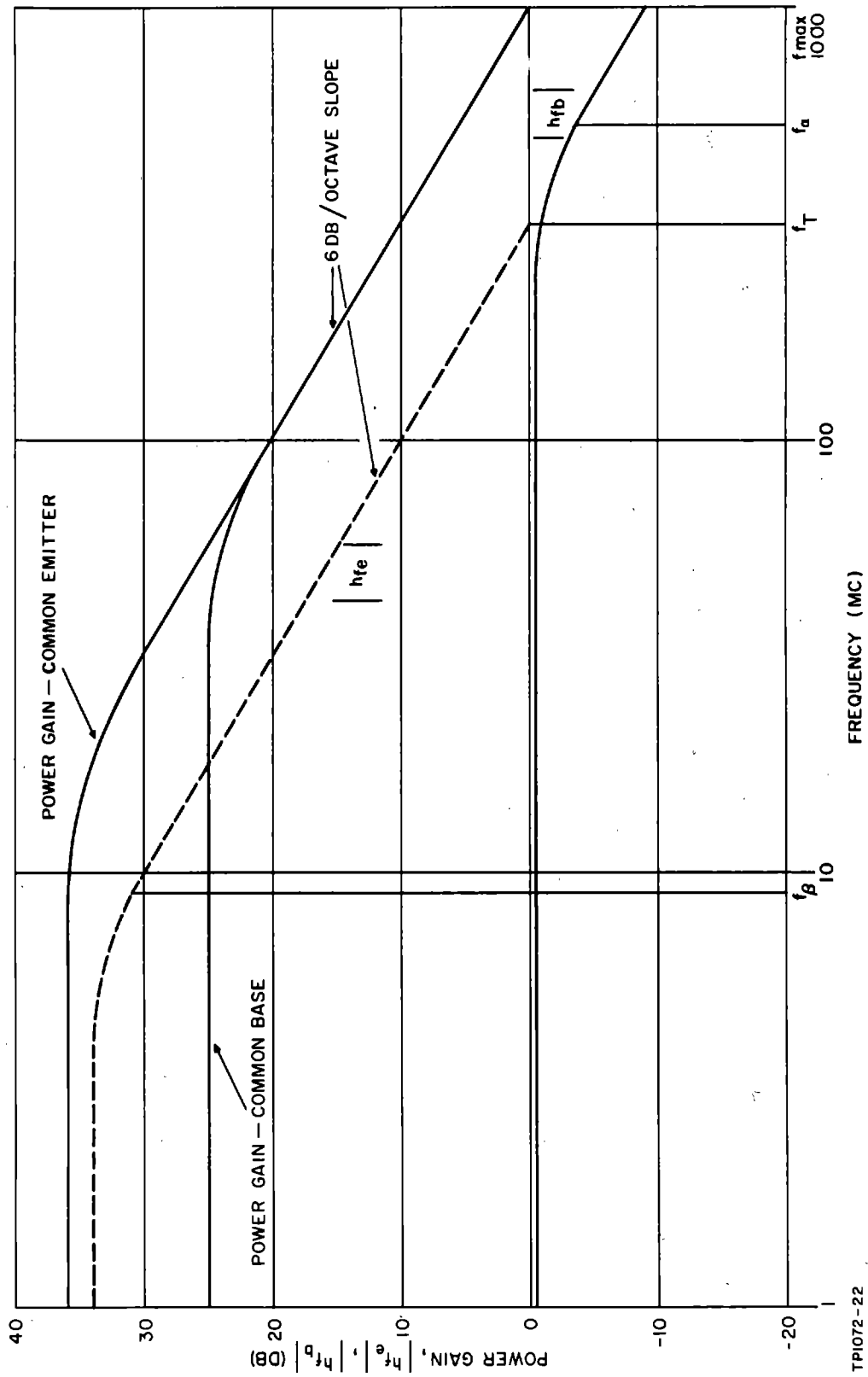


Figure 3-3. Characteristics of a Unilateralized High-Frequency Transistor

C_{ob} and f_T follow an inverse relationship; a transistor having an f_T of 100 MC is likely to have a C_{ob} , at V_{cb} equals 10 V, of from 5 to 10 PF; an "intermediate" transistor with an f_T of 300 MC generally has a C_{ob} , at V_{cb} equals 10 V, of from 3 to 6 PF; while for the same bias conditions, the C_{ob} of a transistor having an f_T of 800 MC will be from 1 to 3 PF. In this latter case the stray capacitance forms a large part of the total, and the collector is usually not connected to the case in an effort to further reduce the strays. A fourth lead is then brought out from the transistor for the purpose of grounding the case.

- (d) Another useful figure of merit, which is usually not specified, is the alpha cutoff frequency f_α . This is the frequency at which the common-base short-circuit current gain is 3 DB down relative to its low-frequency value α_0 . f_α is loosely related to f_T , having a value of from 1.3 to 1.8 f_T .

The performance characteristics shown in Figure 3-3 are representative of the amplifier characteristics to be expected from a transistor with an f_T of about 500 MC.

The power gain of a transistor amplifier not employing unilateralization can be greater than or smaller than that of a unilateralized amplifier. In certain frequency ranges the transistor internal feedback is positive, increasing the parallel resistive component of the input impedance and resulting in an enhanced amplifier power gain. At other frequencies the internal feedback is negative, causing a decrease in the parallel resistive component of the input impedance and hence a reduction in the amplifier power gain. The positive feedback effect commences in the frequency region where the power gain cutoff frequency occurs, extends for several octaves above this point, and is then superseded by the degenerative feedback effect. For common-emitter transistor amplifiers, the positive feedback effect commences in the 5 to 30 MC region, depending on transistor characteristics, and extends in frequency up to, say, 30 to 150 MC. Over the greater part of this frequency range, the transistor internal feedback is sufficient to cause oscillation when the input termination is suitable and the collector load resistance is sufficiently high.

For common-base amplifiers the positive feedback effect commences in the 20 to 100 MC region, depending on transistor characteristics, and extends in frequency up to, say, 100 MC to 1 KMC. Again, over the greater part of this frequency range, oscillation is possible when the terminating impedance levels are appropriate.

Above the quoted frequency ranges, the degenerative effects take over and the power gain falls below that of a unilateralized amplifier. In crystal

oscillator design, this inherent regeneration is a mixed blessing. To a certain extent its effects are beneficial, since it changes the amplifier characteristics in a desirable manner, from the oscillator circuit viewpoint. However, too much regeneration creates other undesirable effects, and since it appears impractical to calculate the amount of regeneration occurring, the permissible amount has to be determined experimentally, thereby complicating the design procedure.

3-13. Transistor Equivalent Circuit

It does not appear possible to construct a simple equivalent circuit which adequately describes the performance of a transistor amplifier at frequencies above a few megacycles. Above this frequency range, the voltage gain and input impedance of both common-base and common-emitter tuned amplifiers vary considerably with frequency of operation in a manner which does not appear amenable to simple analysis.

Below a frequency of 5 to 20 MC, depending on the high-frequency qualities of the transistor and the amplifier configuration, the frequency dependence is smaller, and adequate performance estimations can be made based on the equivalent circuits shown in Figure 3-4. Figure 3-4 (a) is the common-base equivalent circuit which is based on the behavior of the common-base short-circuit current gain (h_{fb} or α) at frequencies in the vicinity of the alpha cutoff frequency f_α . Apparently the common-base short-circuit current-gain-frequency characteristics of a transistor are analogous to those of a transmission line. $|\alpha|$ closely approximates the response of a network having a simple pole at f_α , while the phase angle between input and output current exceeds that of a simple pole by a large amount. For the frequency range below the alpha cutoff frequency f_α , the behavior can be adequately approximated by the equation:

$$h_{fb} = \frac{\alpha_0 \cdot e^{-jm \frac{f}{f_\alpha}}}{1 + j \frac{f}{f_\alpha}} \quad (3-33)$$

where the term $e^{-jm \frac{f}{f_\alpha}}$ accounts for the phase angle lag that occurs in the transistor in excess of that given by the simple pole $(1 + j \frac{f}{f_\alpha})^{-1}$. In present day high-frequency transistors, this excess phase angle at f_α lies in the range of 20 to 50 degrees, giving values for m of from 0.35 to 0.9.

The other components of the circuit are as follows:

- (a) C_{cb}' is the capacitance associated with the collector-base junction and is approximately equal to $(C_{ob} - 1 \text{ PF})$.

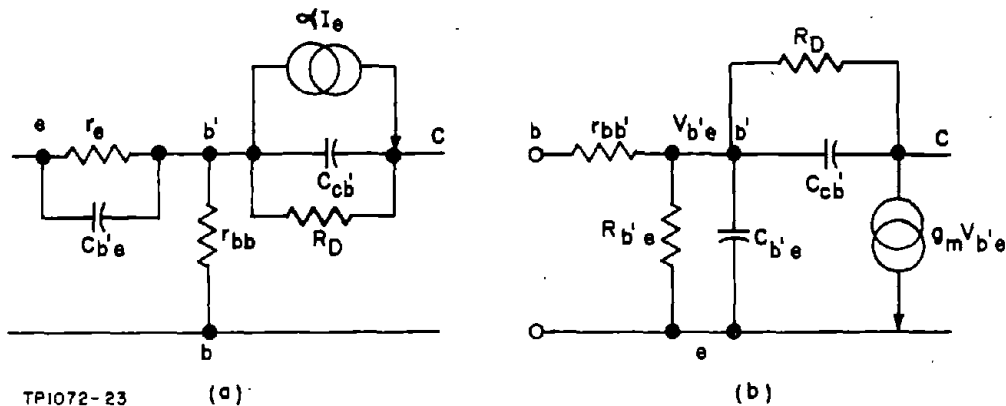


Figure 3-4. High-Frequency Transistor Equivalent Circuits

- (b) $r_{bb'}$ is the resistance of the semiconductor material between the base connection (extrinsic base b) and the active region of the base (intrinsic base b') of the transistor. Typically, the value of $r_{bb'}$ lies between 30 and 100 ohms for all high-frequency transistors, and is assumed to be constant, independent of bias levels and frequency.
- (c) r_e is the sum of the dynamic resistance associated with the forward-biased emitter-base junction and the ohmic resistance r' of the emitter semiconductor material between the emitter connection and the active region of the junction. The dynamic resistance r_e is given by the equation:

$$r_e = \frac{25}{I_E} \quad (3-34)$$

where I_E is the DC emitter current in MA.

Therefore:

$$r_e = \frac{25}{I_E} + r' \quad (3-35)$$

Judging from measurements made on several types of transistor, r' typically has a value of 1 ohm and therefore has little influence on r_e at emitter current levels of less than 3 MA, but can have a major bearing on r_e at high current levels.

- (d) $C_{b'e}$ is the capacitance associated with the emitter-base junction, and its value is an inverse function of emitter current.

Therefore, the time constant $C_{b'e} \cdot r_e$ tends to hold relatively constant as I_E is varied, particularly at low emitter current levels where the effect of the ohmic emitter resistance is small. The value of $C_{b'e}$ is determined from the current gain behavior of a common-emitter amplifier and is subsequently derived when that equivalent circuit is considered.

- (e) R_D is the dynamic resistance of the reverse-biased collector-base junction. An estimation of R_D for a particular transistor type can be obtained from the common-emitter collector current-collector voltage curves frequently given in the data sheets. These curves are obtained with the base essentially open-circuited (constant base current) and therefore the slope of the curves at any given working point is approximately equal to $R_D (1 - \alpha_o)$, which is in turn approximately equal to R_D/h_{FE} . Reference to a set of these curves shows that R_D is a function of both collector current and voltage, decreasing with increasing collector current and voltage. (Care should be taken using this interpretation in the region immediately below the collector-emitter breakdown voltage BV_{CEO} , where the slope of the curves increases drastically. h_{FE} also increases rapidly in this region, and R_D remains essentially constant.)

The common-emitter equivalent circuit shown in Figure 3-4 (b) is derived from the common-base circuit of Figure 3-4 (a). $R_{b'e}$, the resistance between the intrinsic base and emitter, is related to the r_e of the common-base circuit by the equation:

$$R_{b'e} = \frac{r_e}{1 - \alpha_o} \quad (3-36)$$

g_m is also related to r_e by the equation:

$$g_m = \frac{\alpha_o}{r_e} \quad (3-37)$$

α_o is very nearly 1 and, since r_e can be less than 2 ohms under heavy bias conditions, a g_m of several hundred MA/Volt is attainable. The value of $C_{b'e}$ is obtained in terms of r_e and f_T by equating the short-circuit current gain of the common-emitter equivalent circuit to 1. If the transmission through $C_{cb'}$ is neglected, the value of $C_{b'e}$ obtained is:

$$C_{b'e} = \frac{1}{\omega_T \cdot r_e} \quad (3-38)$$

where

$$\omega_T = 2 \pi f_T \quad (3-39)$$

$r_{bb'}$, R_D , and $C_{cb'}$ are the same elements as those in the common-base circuit.

Both of these equivalent circuits are based on, and adequately portray, the short-circuit current gain of the transistor as functions of frequency. In this condition the feedback effects governing operation are those due to the common coupling element between input and output circuits. In the common-base circuit this is the component $r_{bb'}$; in the common-emitter circuit it consists of $R_{b'e}$ and $C_{b'e}$ in parallel. In both cases, the voltage sensitive feedback is assumed to have a negligible effect and the presence of $C_{cb'}$ in the equivalent circuits is merely a token acknowledgement that voltage sensitive feedback occurs.

In attempting to apply these equivalent circuits to oscillator design, tuned amplifier voltage gain and input impedance equations were derived for the circuits of Figure 3-4 and compared with experimental results. It was found that at frequencies below, say, 2 MC, a satisfactory degree of agreement was obtained for operating conditions likely to be employed in oscillator design. Above this frequency the agreement between calculated and measured voltage gains gradually decreased, while the actual amplifier input impedance varied drastically from that calculated for all but small amplifier total load resistances.

Under short-circuited output conditions, good agreement was reached between calculated and measured input impedance. The disagreement appears to be due to the inadequate specification by the circuit of Figure 3-4 of the voltage sensitive feedback between the collector and the intrinsic base and extrinsic base of the transistor. The equations derived from Figure 3-4(b) fail to predict the onset of positive feedback within the amplifier which causes the actual parallel input resistance to increase for amplifier loads above a certain value, whereas the equation predicts a continuous decrease of the parallel input resistance as the amplifier load is increased.

The voltage gain of a tuned transistor amplifier decreases as a function of frequency above a certain frequency f_V , which is a function of both transistor biasing conditions and amplifier load resistance. The disagreement between the measured and calculated amplifier voltage gains is primarily due to the difference in slopes; the voltage gain equation predicting a 20 DB per decade gain reduction, while measurements indicate a slope of from 12 to 16 DB per decade, depending on transistor type.

It is possible that the agreement could be improved by adding additional components to the equivalent circuit of Figure 3-4. However, the equations derived from Figure 3-4 are relatively complex and entail a rather lengthy calculation which makes their usefulness doubtful. Adding more components would

increase the complexity of the equations and result in an undesirably lengthy calculation. This can be circumvented by combining low-frequency voltage gain calculations and short-circuit input impedance calculations with measured data to be subsequently introduced.

The formulae for voltage gain and short-circuit input impedance for the circuits of Figure 3-4 at frequencies below the voltage gain cutoff frequency are:

a. Common-Base Amplifier

Voltage gain:

$$G_{V_o} = \frac{\alpha_o \cdot R_T}{r_e + r_{bb'} (1 - \alpha_o) + (r_{bb'} + r_e) \frac{R_T}{R_D}} \quad (3-40)$$

Short-circuit series-input resistance:

$$R_{in(s)} = r_e + r_{bb'} (1 - \alpha_o) + r_{bb'} \cdot \frac{R_T}{R_D} \quad (3-41)$$

Short-circuit series-input inductance:

$$X_{L(s)} = r_{bb'} \cdot \frac{R_T}{X_{C_{cb}}'} \quad (3-42)$$

b. Common-Emitter Amplifier

Voltage gain:

$$G_{V_o} = \frac{-g_m \cdot R_{b'e} \cdot R_T}{R_{b'e} + r_{bb'} + (r_{bb'} + r_e) \frac{R_T}{R_D (1 - \alpha_o)}} \quad (3-43)$$

Substitution for g_m and $R_{b'e}$ shows (as it should) that $|G_{V_o}|$ is identical for common-base and common-emitter amplifiers.

Short-circuit parallel-input resistance:

$$R_{in(p)} = (r_{bb'} + R_{b'e}) \left[\frac{1 + \left(\frac{r}{X_{C(p)}} \right)^2}{1 + \frac{R_{b'e} \cdot r}{\left(X_{C(p)} \right)^2}} \right] \quad (3-44)$$

Short-circuit parallel-input capacitance:

$$C_{in(p)} = (C_{b'e} + C_{ob'}) \left(\frac{R_{b'e}}{R_{b'e} + r_{bb'}} \right)^2 \left(\frac{1}{1 + \left(\frac{r}{X_{C(p)}} \right)^2} \right) \quad (3-45)$$

where:
$$r = \frac{r_{bb'} \cdot R_{b'e}}{r_{bb'} + R_{b'e}} \quad (3-46)$$

and

$$X_{C(p)} = \frac{1}{\omega (C_{b'e} + C_{ob'})} \quad (3-47)$$

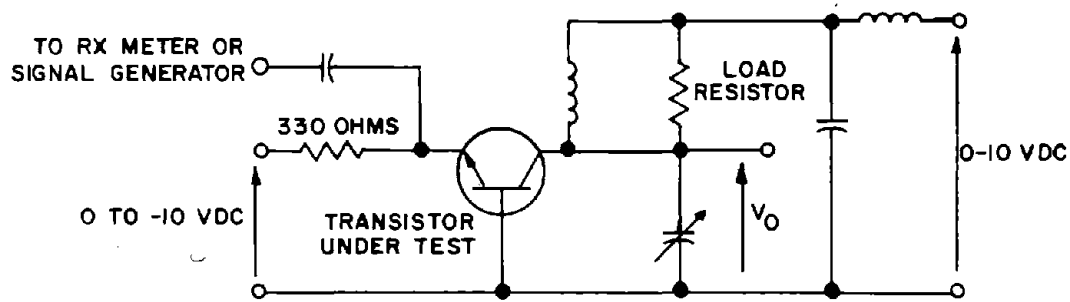
3-14. Experimentally Derived Transistor Amplifier Performance Data

The following data was obtained in the circuits shown in Figure 3-5(a) and (b) for common-base and common-emitter amplifiers, respectively. The two-voltage supply circuit of Figure 3-5(a), which allows a true grounding of the base lead, was used for the common-base amplifier tests to prevent decoupling problems in the base connection to ground. Similarly, in the common-emitter circuit the emitter lead was directly grounded to avoid emitter decoupling problems, and the base current was derived from a second voltage source through a high-value resistance to make the input impedance component due to R_b negligible.

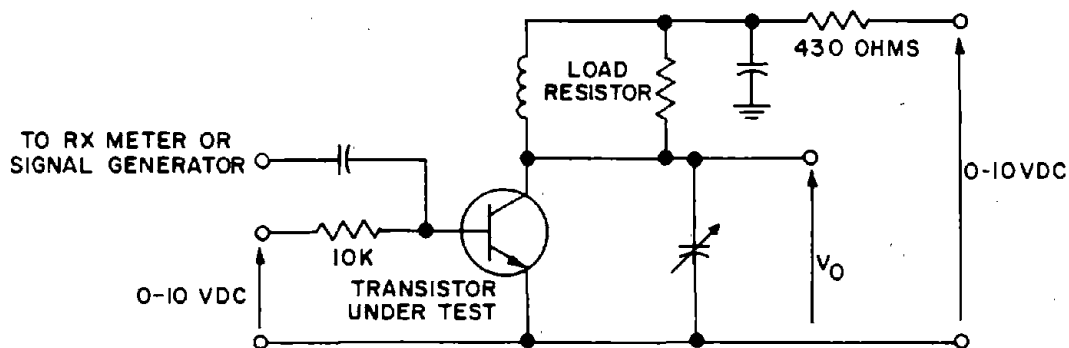
The circuits were constructed to mount directly on the RX Meter ground terminal for input impedance measurements, and the input coupling capacitors used at the various test frequencies were selected to have negligible effect on the input impedance measurements; a condition verified experimentally. In the common-base circuit, the transistor parallel input resistive component is frequently less than 15 ohms. This is the minimum measuring limit of the RX Meter, and a known impedance must be placed in series with the transistor input to bring the total impedance to a measurable level. The transistor input resistance is then obtained by calculation. In this case the coupling capacitor was chosen to cancel the inductive reactance of the low-value resistance used as the series element, thereby simplifying the calculation.

In the common-emitter circuit, the parallel-input capacitance is frequently larger than 27 PF, the largest value directly measurable by the RX Meter. Known values of inductance were then placed across the RX Meter terminals to allow measurements to be made and the parallel-input capacitance then derived by calculation. The RX Meter used for input impedance measurements was modified to reduce the output terminal voltage to 10 MV or less to ensure linear amplifier operation.

Measurements were made on groups of five types of transistors having typical gain bandwidth products of from 300 MC to 1 KMC. Although transistors



(a) Common-Base Amplifier Voltage Gain and Input Impedance Test Circuit



(b) Common-Emitter Amplifier Voltage Gain and Input Impedance Test Circuit

TP1072-24

Figure 3-5. Common-Base and Common-Emitter Amplifier Circuits

having f_T 's at the high end of this range are relatively costly at this time, their cost appears likely to decrease substantially in the near future. When, and if, this occurs, the improved performance characteristics will in many cases make their use desirable in this type of oscillator at frequencies above a few megacycles. Both voltage gain and input impedance measurements were made with the output voltage tuned to maximum.

3-15. Voltage Gain Measurements

The voltage gain of common-base and common-emitter amplifiers is essentially the same, and the following is applicable to either configuration. All the transistors measured showed the same general behavior with frequency. At low frequencies the tuned voltage gain is independent of frequency and is primarily a function of emitter current, total collector load resistance, and the value of R_D . At higher frequencies the tuned voltage gain falls at a rate of between 12 and 16 DB per decade virtually independently of total collector load resistance or emitter current. The cutoff frequency f_V at which the slope commences is a function of load resistance, emitter current, and transistor type.

Figures 3-6, 3-7, and 3-8 show the typical voltage gain as a function of frequency for the various transistor types. Each of these plots was derived from measurements taken on a number of transistors. The variation between units of a given type was in general found to be small; the gain spread at voltage gain levels of 40 DB being ± 2 DB, decreasing to less than ± 1 DB at typical voltage gains of 25 DB. Occasionally, however, transistors are found that deviate appreciably from the norm. In some cases, this appears to be due to an unusually high value of ohmic emitter resistance, affecting the low frequency gain drastically but having little effect at high frequencies. In other cases, C_{ob} appears to be abnormally high, resulting in negligible effect at low frequencies but causing a severe reduction of voltage gain at high frequency. This behavior appears to be exceptional, however, and the spread between individual units of a particular type is probably no greater than that found in vacuum tubes.

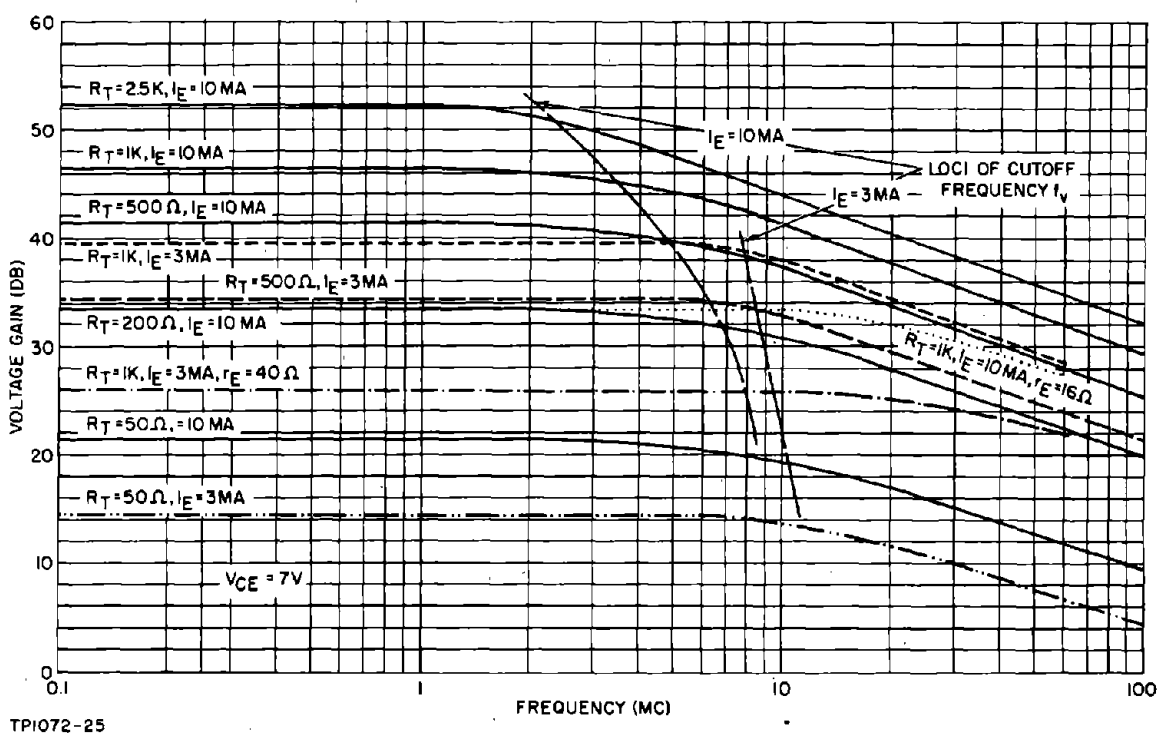
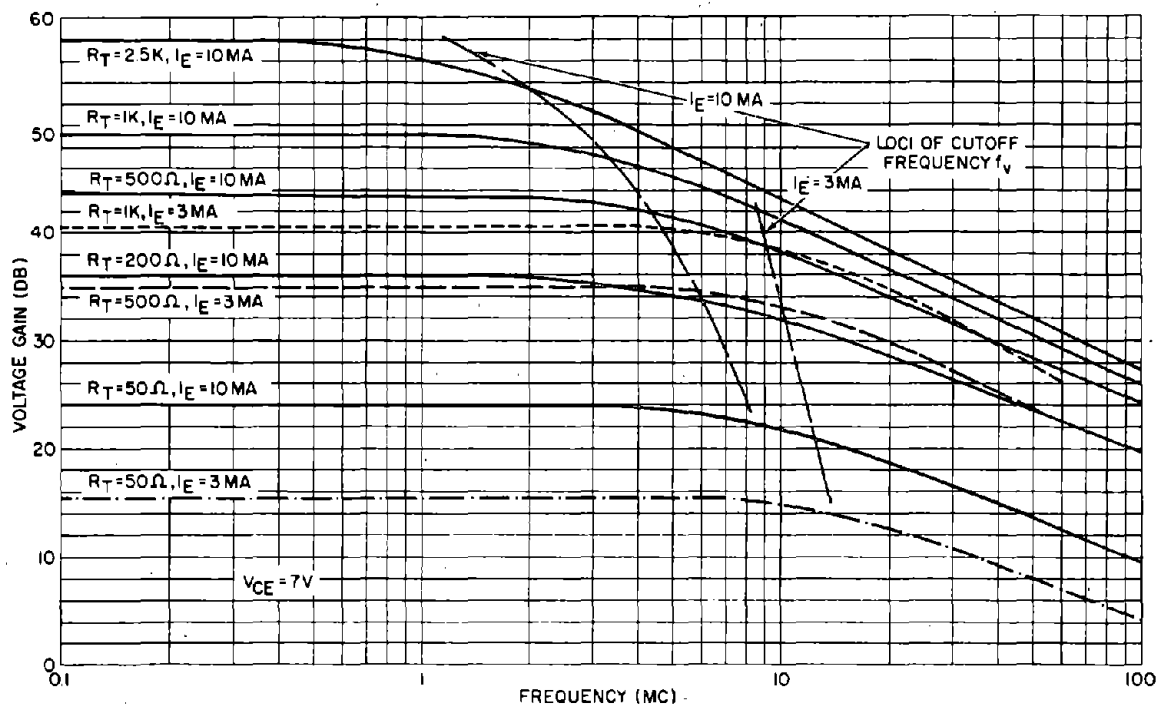


Figure 3-6. 2N706A Tuned Amplifier Voltage Gain as a Function of Frequency

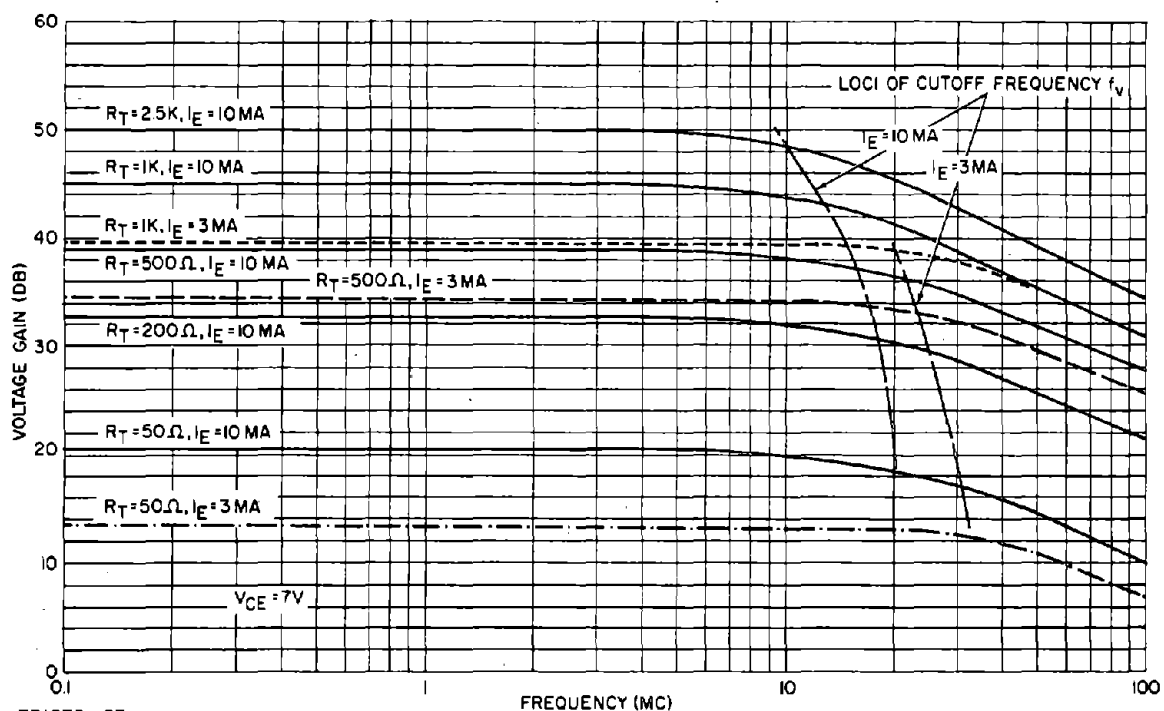
3-16. Voltage Gain Behavior at Frequencies Below f_V

At low emitter currents in this frequency region, the differences in voltage gain of all the transistors tested was small. As shown in Table 3-1, at a frequency of 100 KC and an emitter current of 3 MA, the variation in voltage gain for all types was, with two exceptions, within ± 1.5 DB ($\pm 20\%$) for collector loads of 200 ohms and 1 K. Increasing the emitter current to 10 MA causes an



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Figure 3-7. 2N2219 Tuned Amplifier Voltage Gain as a Function of Frequency



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Figure 3-8. 2N917 and 2N2708 Tuned Amplifier Voltage Gain as a Function of Frequency

TABLE 3-1. VOLTAGE GAIN AT 100 KC

Transistor Type	Transistor h_{FE} at I_E of 3MA 10MA 30MA			Voltage Gain (DB) ($V_{CE} = 7$ VDC)					
				$R_T = 200 \Omega$			$R_T = 1 K$		
				$I_E = 3MA$	$I_E = 10MA$	$I_E = 30MA$	$I_E = 3MA$	$I_E = 10MA$	$I_E = 30MA$
2N2219	-	130	150	$(V_{CE} = 7$ VDC)					
	-	170	190	28	36	43	40.5	49.5	58.5
	-	130	180	27.5	36	42.5	40.5	49	57
	-	330	380	28	36	43.5	41	49	57
2N706A	30	30		28	36.5	43.5	40.5	49	56.5
	22	24		25.5	32.5	36	39	45.5	49.5
	55	60		25	32.5	36	38.5	45	48
	42	46		26.5	34	39	40.5	47	51.5
	60	68		26	34	39	39.5	47	51
2N917	87	108		26.5	34.5	40	40	47.5	50
	80	85		26	33		39.5	45	
	105	120		26	32.5		39.5	44.5	
				20.5	24.5		34	37.5	
				26	32.5		39.5	44.5	
				26	32.5		39.5	45	
2N2708	85	81		26.5	32.5		40	45	
	55	58		25.5	31.5		40	44	
	120	130		25.5	32		39	44	
	45	48		26.5	33		40	46	
2N709	60	68		25.5	31		39	43.5	
	17	23		$(V_{CE} = 4$ VDC)					
	82	96		27	35	41	40.5	48	53.5
				26	32	36	38.5	43	43
				26	33	35.5	39	44.5	44
				24	31.5	35	35	42.5	44
				26.5	33.5	37	39.5	45.5	47
			26.5	33.5	37.5	39.5	46	48	

* Denotes exceptional units

increase in the spread to ± 5 and ± 7 DB for 200-ohm and 1-K collector loads, respectively. However, the total spread between individual units of a given type is less than ± 2.5 DB and typically less than ± 1.5 DB. A further increase of emitter current to 30 MA results in wide variations of voltage gain between the various transistor types. But here again, as in the preceding case, the typical spread within a given type is less than ± 2 DB.

The variation in voltage gain between transistors for a load of 200 ohms is primarily due to the differences in the h_{FE} 's and the emitter ohmic resistance values, since for this load R_D will have a negligible effect. It is therefore possible to estimate the values of $r_e + r_{bb'}(1 - \alpha_0)$ by comparing Equation (3-48) with the actual voltage gains given in Table 3-1. The voltage gain expression, when R_D is assumed infinite, is:

$$G_V = \frac{\alpha_0 R_T}{r_e + r_{bb'}(1 - \alpha_0)} \quad (3-48)$$

Substituting R_T equals 200 ohms, assuming a typical value for α_0 , and equating Equation (3-48) to the typical value of voltage gain given in Table 3-1, gives the values of $r_e + r_{bb'}(1 - \alpha_0)$ shown in Table 3-2. The values of r_e , the dynamic resistance of the emitter-base junction, are also included in Table 3-2 for comparison. Relating the values of the $r_e + r_{bb'}(1 - \alpha_0)$ to r_e shows that the following breakdown gives a satisfactory distribution of the excess resistance:

2N2219 : $r' \approx 0.3$ ohm, $r_{bb'}(1 - \alpha_0) \approx 0.3$ ohm, $r_{bb'} \approx 60$ ohms
 2N706A : $r' \approx 0$, $r_{bb'}(1 - \alpha_0) \approx 1.4$ ohms, $r_{bb'} \approx 60$ ohms
 2N709 } : $r' \approx 1.5$ ohms, $r_{bb'}(1 - \alpha_0) \approx 0.7$ ohm, $r_{bb'} \approx 60$ ohms
 2N917 }
 2N2708 }

TABLE 3-2. DERIVED VALUES OF $r_e + r_{bb'}(1 - \alpha_0)$

Transistor Type	$r_e + r_{bb'}(1 - \alpha_0)$ (ohms)		
	$I_e = 3\text{MA}$	$I_e = 10\text{MA}$	$I_e = 30\text{MA}$
2N2219	8.0	3.2	1.4
2N706A	10	4	2.2
2N709	10	4.5	3.2
2N917	10	4.5	-
2N2708	10	5.0	-
r_e	8.3	2.5	0.83

These experimentally derived values of r' and r_{bb}' suggest that, when considering other comparable transistor types, the emitter-base junction and base ohmic resistances can be assumed to have values of about 1 ohm and 60 ohms, respectively.

The wide variations in voltage gain between the transistor types at high current levels is probably due in part to the difference in the collector-base junction characteristics. As stated previously, the dynamic resistance R_D of the collector-base diode at any given working point is proportional to the slope of the collector curves (frequently given in the transistor data sheets) divided by h_{FE} . Typical sets of these curves are given in Figure 3-9 and show that, at collector currents of a few milliamperes, the onset of voltage breakdown is abrupt, and its effects are largely confined to a small region of voltages in the immediate vicinity of the collector-emitter breakdown voltage, BV_{CEO} . Therefore, for collector-emitter voltages well below BV_{CEO} , the value of R_D is high and virtually uninfluenced by the breakdown characteristic. At higher collector currents the onset of breakdown spreads over a wider region, and consequently its effects are felt at lower collector voltages. The slope of the collector curves at voltages well below BV_{CEO} is then increased relative to that at lower collector currents, causing a reduction in the value of R_D . For a given transistor type, the value of R_D , at a particular working point V_{CE} and I_C , is a function of h_{FE} , the relative value of V_{CE} to BV_{CEO} , and any peculiarities of the collector-base diode. In view of this complex relationship, it is therefore not surprising that large differences in voltage gain occur at high emitter current levels.

Equation (3-40) qualitatively illustrates the effect of the decreasing value of R_D with increasing emitter current. r_{bb}' is much greater than r_e for emitter currents larger than 2 MA, and consequently the term $(r_{bb}' + r_e) \frac{R_T}{R_D}$ is virtually inversely proportional to R_D for a given amplifier load, R_T . Also, $r_e + r_{bb}'(1 - \alpha_0)$, the remainder of the denominator term, decreases rapidly with increasing emitter current, approaching a terminal value of 1 to 3 ohms for emitter currents in excess of 20 MA. At high current levels, therefore, an $(r_{bb}' + r_e) \frac{R_T}{R_D}$ value of a few ohms will have an appreciable effect on the amplifier voltage gain, while at low current levels its contribution to the denominator term will be small, particularly since R_D will then have a larger value.

The effect of the emitter ohmic resistance will also be great at these current levels and can cause substantial variations. Similarly, the product $r_{bb}(1 - \alpha_0)$ also has a significant effect on the voltage gain at high currents.

For those transistor types having data sheets containing collector curves covering the contemplated operating conditions, it is possible to estimate the value of R_D and its effect on the voltage gain by measuring the slope of the curve

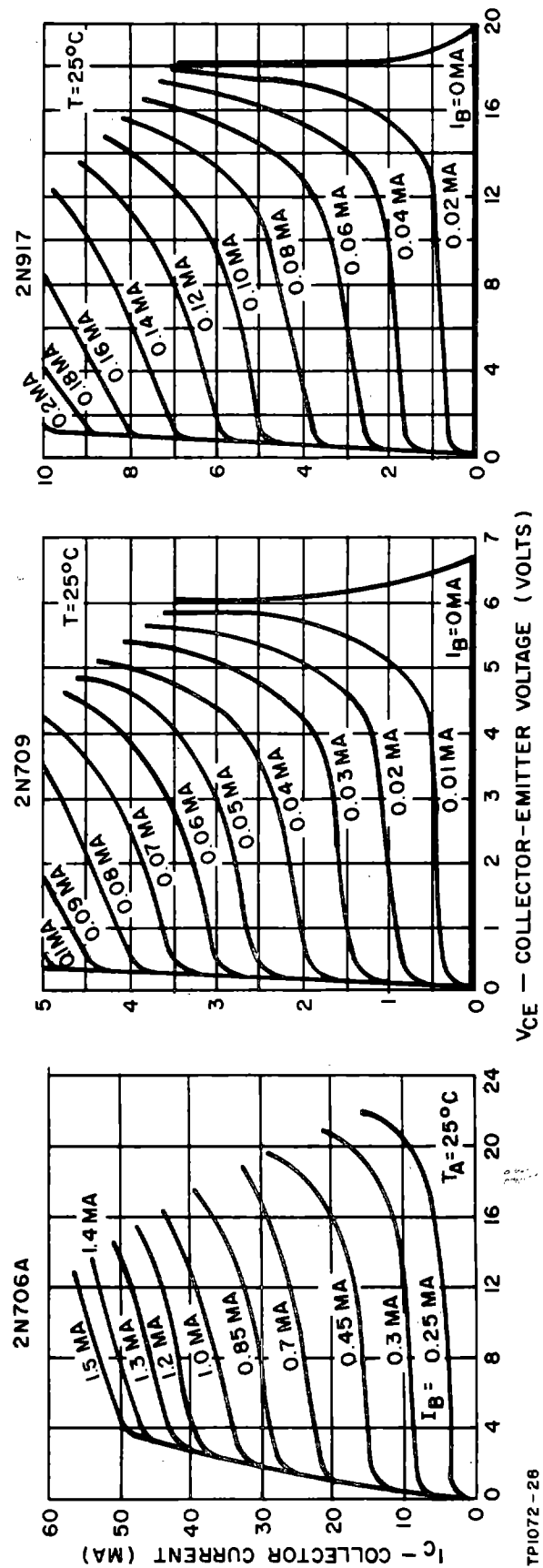


Figure 3-9. Collector Current Versus Collector-Emitter Voltage

at the operating point. Carrying out this procedure for the 2N706A and 2N917 gives the results shown in Table 3-3. Comparison of these voltage gains with the measured values in Table 3-1 and Figures 3-6 and 3-8 shows good agreement, except for the case of the 2N917 with $R_T = 2.5K$, which gives a gain 3 DB higher than that measured. This appears to be caused by the behavior of the transistor saturation resistance at collector currents larger than 10 MA. Above 10 MA the saturation resistance increases appreciably, with the knee extending out into the region of $V_{CE} = 5V$ at an I_E of 30 MA. In addition, h_{FE} falls rapidly with increasing emitter current in the region above 10 MA. This combination of effects would cause a considerable amount of 2nd harmonic distortion in the collector voltage waveform. However, the increase would be gradual and would not be readily apparent in the procedure used during the tests to check linearity. This consisted of increasing the drive signal by 3 DB and noting the increase in output. This knee behavior also occurs in the 2N2708 transistor and may be a characteristic of the very high gain-bandwidth transistor types. When considering the use of these types of transistors in the common-emitter configuration, it will be advisable to investigate this and to determine any resulting undesired effects. In the case of the 2N917 and the 2N2708, the behavior of the saturation resistance and h_{FE} will limit the desirable operating current range to below 10 MA and to oscillator applications requiring less than, say 20 or 30 MW of output power.

TABLE 3-3. LOW FREQUENCY VOLTAGE GAIN

Transistor Type	I_E (MA)	V_{CE}	Slope (K)	h_{FE} from curves	R_D (K)	R_T (K)	$(r_e + r_{bb'}) \frac{R_T}{R_D}$ (ohms)	G_V
2N706A	10	7	8	30	240	1	0.27	230 (47 DB)
	10	7	8	30	240	2.5	0.7	520 (54 DB)
	30	7	2	35	70	1	0.9	310 (50 DB)
2N917	10	7	3.5	60	210	1	0.3	205 (46 DB)
	10	7	3.5	60	210	2.5	0.75	480 (53 DB)

In the frequency range of 0.8 to 20 MC, amplifier voltage gains in excess of 100 (40 DB) are normally unnecessary in oscillators; and over the greater part of the range, a gain of 50 is more than adequate. This order of voltage gain is easily achieved, and it will often be possible to trade voltage gain for amplifier stability with transistor interchange by incorporating an unbypassed emitter

resistance, r_E , in the circuit. This is particularly desirable at emitter current levels above 3 MA where the voltage gain spread increases. At low frequencies its effect, insofar as voltage gain is concerned, is to increase the apparent value of r_e . Reference to the values of r' , $r_{bb}'(1 - \alpha_0)$ and $(r_e + r_{bb}') \frac{R_T}{R_D}$ previously derived, and the voltage gain spreads given in Table 3-1, shows that values of r_E , as small as 2 or 3 ohms will be beneficial in stabilizing the voltage gain at high current levels.

Another advantage is that the range of frequencies over which the voltage gain is independent of frequency is increased. An example of this is given in Figure 3-6 where the tuned amplifier gain with an emitter resistor of 16 ohms, an R_T of 1 K, and a voltage gain of 33 DB (≈ 50) is shown to have a cutoff frequency three times higher than that of an amplifier with the same voltage gain, an R_T of 200 ohms, and no emitter resistor.

The use of emitter degeneration is also helpful during the preliminary design stage, particularly for emitter current levels above 3 MA, when a transistor of unknown detailed characteristics is to be used. The assumption of a few ohms of emitter degeneration will then enable the amplifier gain to be accurately estimated.

3-17. Voltage Gain Cutoff Frequency f_V

Because of the desirability of being able to estimate the voltage gain cutoff frequency, a semi-empirical approach was used in developing a formula for f_V with the following results. The behavior of the loci of f_V at emitter current levels of 3 and 10 MA for various values of amplifier load is shown in Figures 3-6, 3-7, and 3-8. The same general behavior is apparent for all the tested transistor types. At low values of amplifier load, f_V is almost independent of R_T and is primarily determined by the behavior of the extrinsic transconductance of the transistor. From Figure 3-4 (b), the relationship between V_1 and $V_{b'e}$ when the collector and emitter are short-circuited is:

$$\frac{V_{b'e}}{V_1} = \frac{R_{b'e}}{(r_{bb}' + R_{b'e}) (1 + j \frac{r}{X_{C_{b'e}}})} \quad (3-49)$$

where

$$r = \frac{R_{b'e} \cdot r_{bb}'}{R_{b'e} + r_{bb}'} \quad (3-50)$$

Therefore, the extrinsic transconductance is:

$$\text{Extrinsic } g_m = \frac{g_m \cdot R_{b'e}}{(r_{bb}' + R_{b'e}) (1 + j \frac{r}{X_{C_{b'e}}})} \quad (3-51)$$

The extrinsic transconductance cutoff frequency f_V' is then:

$$f_V' = \frac{1}{2\pi C_{b'e} \cdot r} \quad (3-52)$$

Relating Equation (3-38) to Equation (3-52) gives:

$$f_V' = \frac{r_e}{r} \cdot f_T \quad (3-53)$$

Using typical values of f_T from the data sheets and the typical values of r_e , $r_{bb'}$, and h_{FE} previously tabulated gives the f_V' shown in Table 3-4. f_V' is the theoretical frequency at which the extrinsic transconductance is 3 DB down on a response curve having a 20 DB per decade attenuation characteristic at higher frequencies. The experimental results indicate that the actual attenuation characteristic is approximately half this theoretical value and that the experimental values of f_V correspond to the frequency at which the voltage gain is 1 to 1.5 DB down. The magnitude of the response of a network having a simple single pole is down by 1 DB at one-half the cutoff frequency, and this is the value which should be compared for agreement with the experimentally derived cutoff frequencies, f_V , given in Table 3-4.

TABLE 3-4. CALCULATED VALUES OF TRANSCONDUCTANCE CUTOFF FREQUENCY

Transistor Type	I_E (MA)	r_e (ohms)	Typical h_{FE}	$R_{b'e}$ (ohms)	r (ohms)	f_T (MC)	f_V' (MC)	$f_V' \sqrt{2}$ (MC)	f_V (MC)
2N706A	10	2.5	40	100	40	300	19	9.5	10-11
	3	8.3	40	330	50	200	33	16.5	13-14
2N2219	10	2.8	130	360	50	300	17	8.5	10-12
	3	8.3	100	830	56	250	37	18.5	16-18
2N917	10	4	80	320	50	700	56	28	21-24
	3	9.5	70	670	54	700	120	60	38-42

Extrapolating the loci of f_V to the 0 DB gain level gives the approximate values presented in the last column of Table 3-4. Comparison with the calculated values of $f_V' \sqrt{2}$ gives substantial agreement, with the exception of the 2N917 at an

emitter current of 3 MA where the actual cutoff frequency is 30 percent below the estimated value.

For higher values of amplifier load resistance, it was experimentally found that the tuned amplifier voltage gain cutoff frequency with a given load resistor coincided with that obtained when the circuit was rearranged as a video amplifier. The untuned voltage gain of the equivalent transistor circuit at frequencies well below f_V' is:

$$G_{VV} = \frac{\alpha_o \cdot R_T}{r_e + r_{bb'}(1 - \alpha_o) + \frac{R_T}{R_D}(r_e + r_{bb'}) + j \frac{R_T}{X_{C_{cb}}}(r_e + r_{bb'})} \quad (3-54)$$

G_{VV} exhibits the frequency response of a simple pole with a cutoff frequency given by the condition:

$$r_e + r_{bb'}(1 - \alpha_o) + \frac{R_T}{R_D}(r_e + r_{bb'}) = \frac{R_T}{X_{C_{cb}}}(r_e + r_{bb'}) \quad (3-55)$$

The left-hand side of Equation (3-55) is the denominator term of the low frequency voltage gain expression. Therefore:

$$f_V = \frac{1}{2\pi C_{cb'} \cdot G_{V_o}(r_e + r_{bb'})} \quad (3-56)$$

Using the measured values previously derived and values of $C_{cb'}$ estimated from the data sheets, assuming $C_{cb'}$ is 1 PF less than $C_{ob'}$, gives the cutoff frequency values shown in Table 3-5.

TABLE 3-5. CUTOFF FREQUENCY VALUES

$I_E = 10 \text{ MA}, V_{CE} = 7 \text{ V}$			
Type	R_T (K)	$C_{cb'}$ (PF)	f_V (MC)
2N706A	2.5	2.5	1.8
	1	2.5	4.3
	0.5	2.5	8.3
2N2219	2.5	3.5	0.9
	1	3.5	2.3
	0.5	3.5	4.6
2N917	2.5	1	5.2
	1	1	12

The cutoff frequency values derived from Equation (3-56) indicate the frequency at which the response is 3 DB down. In this case, however, reasonable agreement is obtained for R_T values of 1 K or larger when a direct comparison is made with the measured values of f_V . The exception is the 2N917 with a 2.5 K load where the calculated and measured values show substantial disagreement. This may also be attributable to the previously noted behavior of saturation resistance characteristic of this transistor. At lower values of R_T the cutoff frequency given by Equation (3-56) approaches the transconductance cutoff frequency and is therefore no longer valid. The theoretical cutoff frequency f_{VC} , when both effects are combined, can be derived from the transistor equivalent circuit as:

$$f_{VC} = \frac{1}{2\pi \cdot G_{VO} \left[\frac{r_{bb'}}{\omega_T \cdot R_T} + (r_e + r_{bb'}) C_{cb'} \right]} \quad (3-57)$$

The addition of an unbypassed emitter resistor, r_E , effectively increases the values of r_e . For an amplifier using a 2N706A transistor with $R_T = 1K$, $I_E = 10MA$, and $r_E = 16$ ohms, the value of f_V given by Equation (3-56) is 20 MC. Comparison with the measured voltage gain characteristic for these conditions given in Figure 3-6 shows an error of 25 percent. The calculated transconductance cutoff frequency, $\frac{f'_V}{2}$, is 45 MC.

3-18. Voltage Gain at Frequencies Above f_V

In this frequency region the tuned voltage gain decreases at a rate of from 10 to 16 DB per decade, depending on transistor type, emitter current, and amplifier load resistance. The effect of the last two factors, however, appears to be small judging from the limited experimental data. In the worst cases, the increase in slope between loads of 50 ohms and 2.5 K was approximately 4 DB per decade.

The voltage gain available in this frequency range is therefore primarily dependent on the cutoff frequency, f_V , and since this decreases rapidly with increasing values of load resistance, the voltage gain as a function of R_T is non-linear. The most marked example of this is the 2N2219 where a 2.5 times increase in R_T from 1 K to 2.5 K results in a voltage gain increase of only 1.5 to 2 DB (15 to 25 percent) at frequencies above 10 MC, whereas a similar increase at frequencies below f_V gives an increase of voltage gain of 8 DB (2.5 times). A similar, but less severe, reduction occurs for the other transistor types.

In this frequency region the voltage gain formula given by the transistor equivalent circuit of Figure 3-4 is not accurate. This formula gives a 20 DB per decade slope above f_V , which is considerably greater than that actually measured.

It will therefore be necessary to make voltage gain measurements when designing in this frequency range using other transistor types, although preliminary estimations can be made from the plots of Figure 3-6, based on the relative values of f_T and h_{FE} . This is no great inconvenience if the test circuit is constructed in the form to be used for the prototype oscillator.

In this sub-section the following has been determined:

- (a) The voltage gain at frequencies below f_V can be estimated with adequate accuracy from Equation (3-40), assuming $r' = 1$ ohm, $r_{bb}' = 60$ ohms, and using a value for R_D derived from the data sheet.
- (b) The value of the cutoff frequency f_V can be adequately estimated from Equations (3-53) and (3-56) and the known general behavior of f_V .
- (c) In the frequency region above f_V , an estimation of voltage gain adequate for the preliminary design stage can be obtained either by first determining the approximate cutoff frequency loci shape from f_V calculations at $R_T = 0$ and, say, $R_T = 1$ K, or by extrapolation or interpolation from the plots of Figures 3-6 through 3-8.

The temperature dependency of the voltage gain of a transistor amplifier was found to be quite small when adequate biasing arrangements are used. Voltage gain changes of less than ± 20 percent were obtained over the temperature range of -55 to $+105$ degrees C using silicon transistors.

3-19. Common Emitter Amplifier Input Impedance

For the Pierce type oscillator which is only used up to 20 MC, it is desirable to know the amplifier input impedance in terms of the parallel resistive and reactive components. Measurements were made on tuned amplifiers for various amplifier loads and transistor types at frequencies of 5 and 20 MC, and the results obtained are shown in Figures 3-10, 3-11, and 3-12.

3-20. Parallel Input Resistance

Referring to the parallel input resistive components shown in Figures 3-10 and 3-11, it is apparent that the general behavior of this component is similar for all the transistors tested. In each case, as the amplifier load resistance is increased from the zero value, the input resistance decreases at first, levels out in the region of R_T equal to 100 to 600 ohms, and then increases. In some instances it reaches values several times that measured with the amplifier output short-circuited. The amount of decrease is dependent on the frequency and the transistor type. At 20 MC all the transistors tested show a maximum decrease

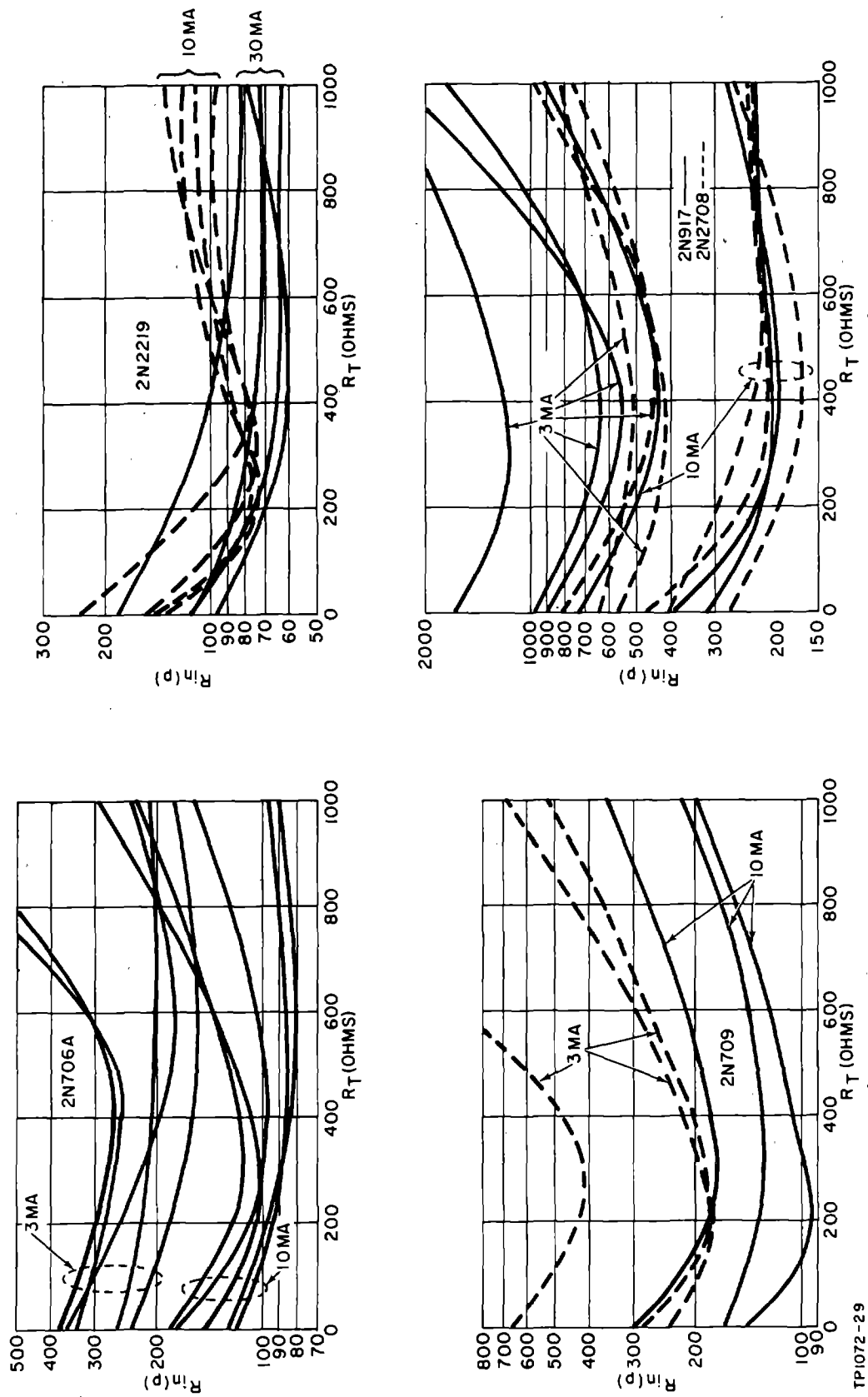


Figure 3-10. Amplifier Parallel Input Resistance Measurements, 20-MC Frequency

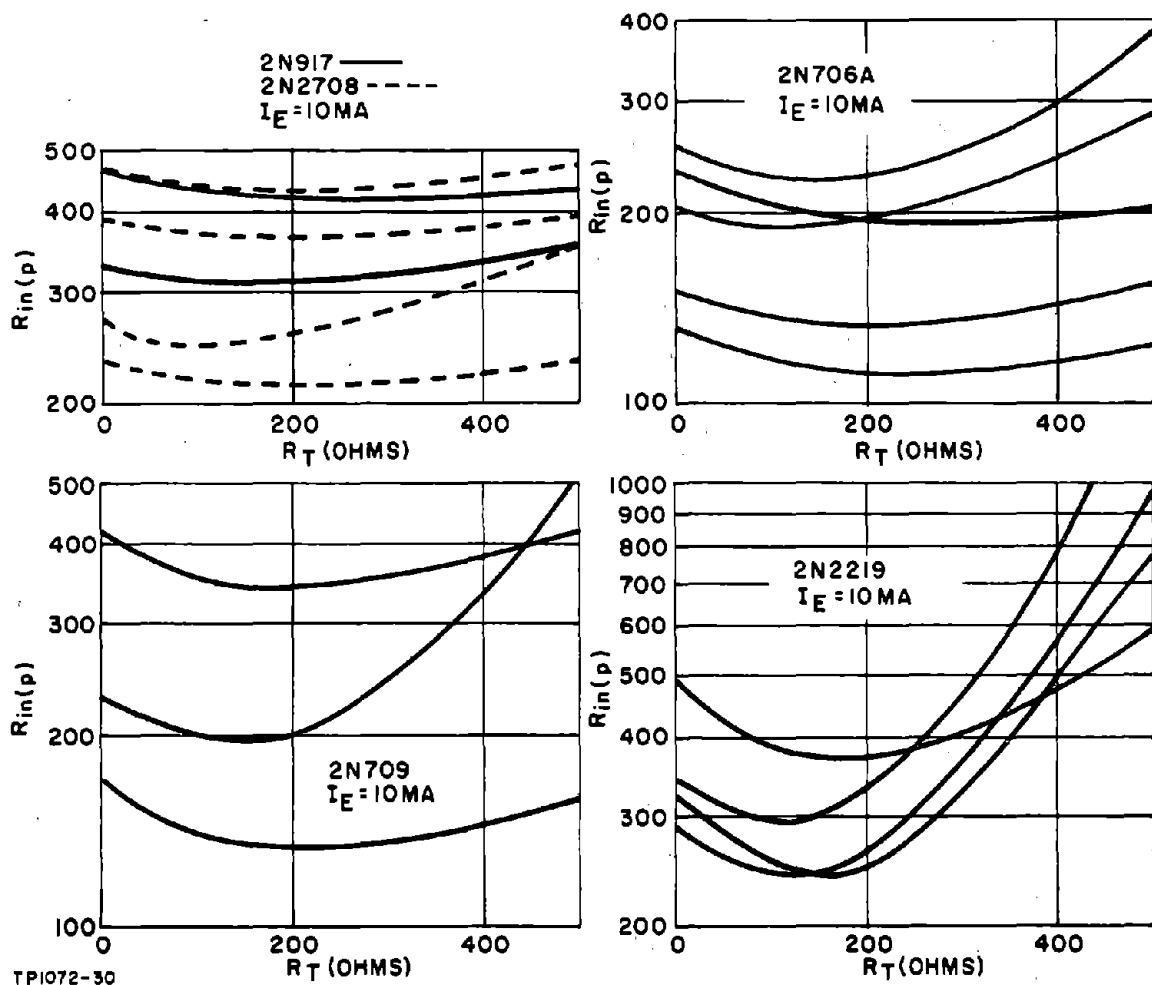
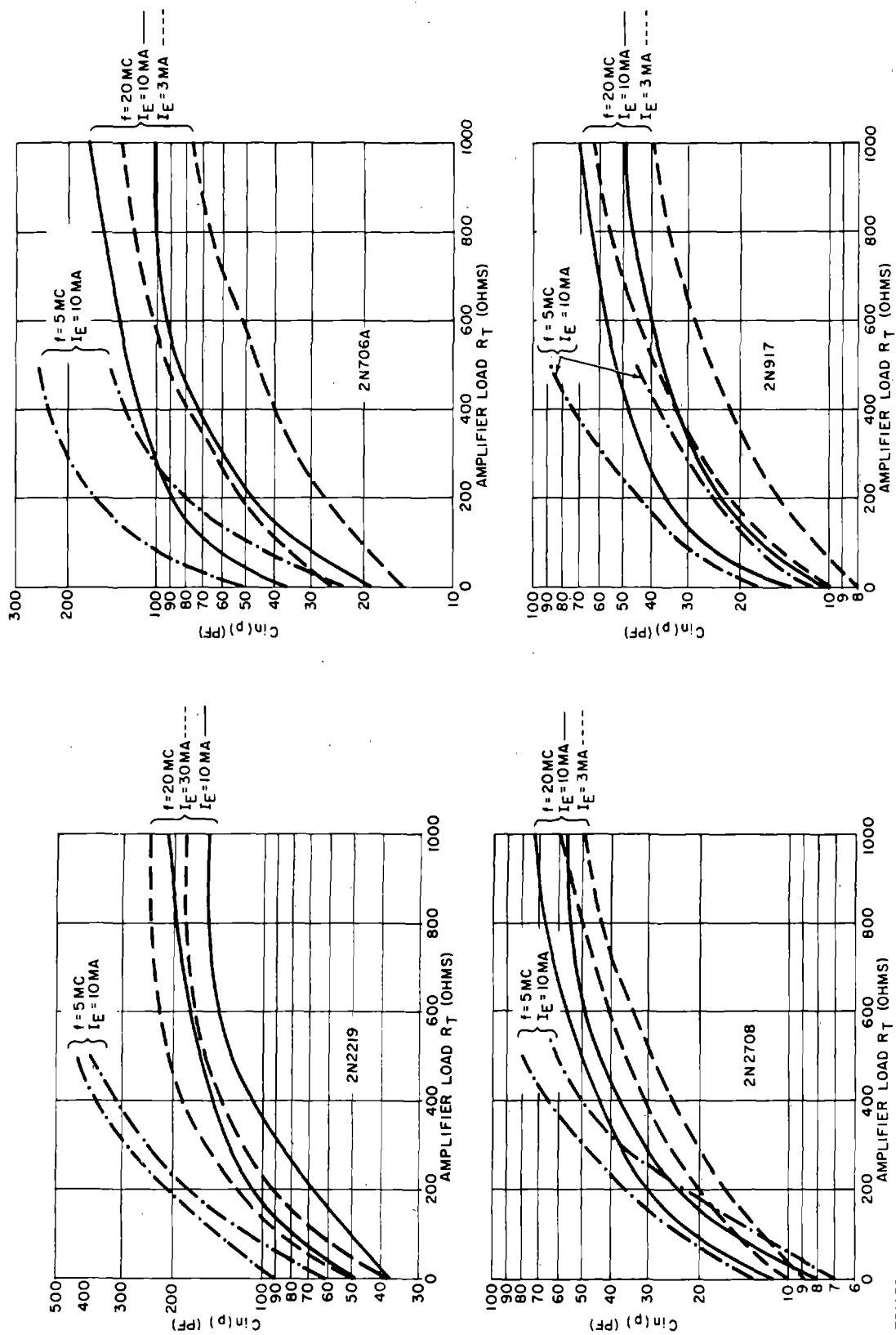


Figure 3-11. Amplifier Parallel Input Resistance Measurements, 5-MC Frequency

in input resistance of from 30 to 50 percent of the short-circuited output value; while at 5 MC the decrease was from 10 to 30 percent with, in general, the lower f_T transistor types showing the greater reduction.

The increase in input resistance following the minima is due to the positive feedback occurring within the transistor, which at much higher frequencies than those considered here is capable of causing sustained oscillation. Up to 20 MC, at the amplifier load levels considered, this condition is not likely to occur and the major effect is the increase in parallel input resistance. Input resistance equations based on the equivalent circuit of Figure 3-4 do not account for this effect, but give a reasonably accurate estimate of the input resistance when the amplifier output is short-circuited. The short-circuit parallel input impedance for the transistor equivalent circuit of Figure 3-4, assuming $X_{C_{cb}'}$ and R_D are much larger than $X_{C_{b'e}}$ and $R_{b'e}$, respectively, is:



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Figure 3-12. Amplifier Parallel Input Capacitance Measurements

$$R_{in(p)} = (r_{bb'} + R_{b'e}) \left[\frac{1 + \left(\frac{r}{X_{C_{b'e}}} \right)^2}{1 + \frac{r \cdot R_{b'e}}{(X_{C_{b'e}})^2}} \right] \quad (3-58)$$

where r is the parallel resistance of $r_{bb'}$ and $R_{b'e}$. But from Equations (3-38) and (3-39):

$$\frac{r}{(X_{C_{b'e}})} = \frac{r}{r_e} \cdot \frac{f}{f_T} \quad (3-59)$$

and:

$$\frac{r \cdot R_{b'e}}{(X_{C_{b'e}})} \approx h_{FE} \cdot \frac{r}{r_e} \cdot \left(\frac{f}{f_T} \right)^2 \quad (3-60)$$

Therefore:

$$R_{in(p)} \approx (r_{bb'} + R_{b'e}) \left[\frac{1 + \left(\frac{r}{r_e} \cdot \frac{f}{f_T} \right)^2}{1 + h_{FEmin} \cdot \frac{r}{r_e} \cdot \left(\frac{f}{f_T} \right)^2} \right] \quad (3-61)$$

(The minimum value of h_{FE} is used in Equation (3-61) to obtain the minimum value of $R_{in(p)}$.)

Substituting the previously derived experimental values of r_e and $r_{bb'}$, and minimum h_{FE} and typical f_T values obtained from the data sheets, into Equation (3-61) gives the calculated values of $R_{in(p)}$ shown in Table 3-6. These represent the minimum expected values of $R_{in(p)}$ with the amplifier output shorted. Comparison with the measured values also given in Table 3-4 shows a reasonable degree of agreement between the lowest measured values and the calculated values, particularly since only one transistor out of the entire number tested had a current gain approaching the minimum value.

It will subsequently be shown that in the Pierce-type oscillator the condition placed on the amplifier parallel input resistance is that it should not be less than a certain value determined by crystal loading. It is therefore not necessary to know the input resistance accurately, provided that this minimum condition is satisfied. Further, this limiting value of parallel input resistance is not a rigidly determined condition, but is rather, a condition determined on the basis of circuit feasibility and desirable crystal loading conditions. In view of this, it is considered sufficient for design purposes to consider the amplifier input resistance to be the value calculated for short-circuited output conditions using the minimum value of h_{FE} . The amplifier input resistance for the majority

TABLE 3-6. SHORT-CIRCUIT INPUT RESISTANCE CALCULATIONS

$V_{bb} = 60\Omega, V_{CE} = 7 \text{ VDC}$															
Type	Freq (MC)	I_E (MA)	$h_{FE \text{ min}}$	r_c (ohms)	R_{Dc} (ohms)	r_c (ohms)	$\frac{r}{r_c}$	$\left(\frac{r}{r_c}\right)^2$	I_T (Typical) (MC)	$\frac{I}{I_T}$	$\left(\frac{I}{I_T}\right)^2$	$\left(\frac{r \cdot f}{r_c \cdot f_T}\right)^2$	$h_{FE} \cdot \frac{r(f)}{r_c(f_T)}$	$R_{in(p)}$ (ohms)	Measured $R_{in(p)}$
2N706A	20	10	20	2.5	50	27	11	116	300	0.067	45×10^{-4}	0.052	0.099	110	124, 120, 175, 146, 150, 182
	20	3	15	8.5	128	41	4.8	23	200	0.1	0.01	0.23	0.75	130	235, 233, 360, 330, 370
2N2219	20	10	75	2.8	210	47	17	284	300	0.067	45×10^{-4}	1.3	5.7	93	138, 143, 155, 240
	20	30	85	1.1	94	37	34	1130	300	0.067	45×10^{-4}	5.1	13	67	97, 116, 116, 185
	20	3	60	8.6	516	54	6.3	40	250	0.08	64×10^{-4}	0.256	2.4	215	225, 245, 230, 340
	5	10	75	2.8	210	47	17	284	300	0.017	2.9×10^{-4}	0.08	0.37	210	290, 340, 320, 500
2N2708	5	30	85	1.1	94	37	34	1130	300	0.017	2.9×10^{-4}	0.33	0.84	110	163, 200, 187, 300
	20	10	~ 30	4	120	40	10	100	1100	0.018	3.3×10^{-4}	0.03	0.1	170	400, 270, 230

of transistors will then be larger than this value for all conditions of loading, and only occasional transistors will result in lower values (and then only for a narrow range of amplifier loads).

Another factor justifying this approach is the behavior of the input impedance under the actual large signal operating conditions that occur in an oscillator. The signal voltage appearing across the emitter-base junction is then usually large compared to the "linear" operating region of the junction, and the input resistance can then only be considered in terms of its average value. Since this cannot be readily specified or related to the small signal input resistance, it appears unrealistic to attempt a more accurate determination of $R_{in(p)}$ than that outlined above.

The frequency dependence of $R_{in(p)}$ varies appreciably between transistor types. In general, when all other characteristics are similar, a transistor type having a high value of $h_{FE \min}$ will show a greater frequency dependence of $R_{in(p)}$ than a transistor type having a lower $h_{FE \min}$. This is because $R_b'e$ is larger, and therefore $X_{C_b'e}$, which will have a similar value for both types, becomes comparable with $R_b'e$ at a lower frequency. Also, high values of f_T will result in a smaller frequency dependency. The 2N917 and 2N2708 types tested showed negligible frequency dependence of $R_{in(p)}$ up to 20 MC.

3-21. Common Emitter Amplifier Parallel Input Capacitance

The behavior of the tuned transistor amplifier parallel input capacitance is shown in Figure 3-12 as a function of amplifier load resistance at frequencies of 5 and 20 MC. In these plots the pairs of similar lines represent the limits within which the measured input capacitance values lie for the indicated emitter currents. Similar general behavior is evident for all the transistors tested; as R_T increases from zero value, the capacitance at first increases rapidly and then slows gradually, apparently approaching a terminal value for amplifier loads in the region of 1 to 2 K.

The increase in $C_{in(p)}$ is due to the Miller effect action of $C_{cb'}$ between the intrinsic base and the collector, and the stray capacitance between the extrinsic base and the collector. The effect of $C_{cb'}$ is to place a capacitance in parallel with $C_b'e$ approximately equal to $C_{cb'}$ times the amplifier voltage gain. In the lower f_T transistors, this can amount to several hundred picofarads at amplifier load levels of a few hundred ohms. This increased capacitance is reflected into the base-emitter terminals by the action of $r_{bb'}$ and $R_b'e$. The stray capacitance between base and collector may also reflect an input capacitance of 100 PF into the base circuit, particularly if care is not taken in the circuit layout to avoid adding further strays.

In the Pierce oscillator, the amplifier input is terminated in a capacitance forming part of the feedback network. The amplifier parallel input capacitance forms a part of this capacitance; and consequently it need not be known accurately during the preliminary design calculations, since any discrepancies can be remedied during the experimental stage of the design, provided $C_{in(p)}$ does not exceed the required total value of the feedback network capacitance. In practice it is desirable, because of the instability of $C_{in(p)}$, that it should be much smaller than the required total. In view of this it is considered preferable, when considering the use of other transistor types, to use the plots of Figure 3-12 to estimate $C_{in(p)}$ rather than to attempt to calculate its value, particularly since the equation for $C_{in(p)}$ based on the transistor equivalent circuit of Figure 3-4 is unwieldy and of limited accuracy.

The estimation of $C_{in(p)}$ for other transistor types should be made on the basis of the relative values of f_T and h_{FE} to those of the transistor types tested.

In this sub-section it has been determined that:

- (a) The parallel input resistance of a common-emitter amplifier can be calculated with sufficient accuracy using Equation (3-61).
- (b) The parallel input capacitance can be estimated with adequate accuracy from the plots of Figure 3-12.

3-22. Amplifier Phase Shift

The behavior of the phase angle between the amplifier input and output voltages has not been investigated in detail, primarily due to the lack of suitable test equipment. However, crude measurements of tuned amplifier phase angle were made at a frequency of 60 MC for an amplifier load of 200 ohms and an emitter current of 10 MA using a dual-trace sampling oscilloscope. At this frequency it was found that, for the 2N706A, 2N2219, 2N709, 2N917 and 2N2708 type transistors, the amplifier phase shift, when tuned to maximum output, was in the region of 40 to 60 degrees.

As shown by the amplifier response plots of Figures 3-6, 3-7, and 3-8 at 60 MC, the amplifier was in all cases working well above the cutoff frequency in the region where the tuned voltage gain has a response of 12 to 14 DB per decade. Network theory suggests that a network exhibiting a slope of this order will have a phase angle of 50 to 65 degrees, which closely agrees with the values measured. Assuming that this agreement is not coincidental, this result can be extrapolated indicating an amplifier phase shift of approximately 30 degrees at the cutoff frequency f_v . Amplifier phase angles of more than 20 degrees are not desirable, primarily because of the variations which may occur due to environmental

condition changes and which will cause oscillator frequency drift. It is therefore desirable to work the amplifier below f_T if at all possible. For the lower f_T transistors at frequencies above a few megacycles, this entails working under low voltage gain conditions. The use of emitter degeneration will also be helpful in increasing the effective value of f_T and reducing phase shift.

3-23. Common-Base Amplifier Input Impedance

In oscillators using a common-base transistor amplifier, it is usually desirable to know the series components of the amplifier input impedance. Input impedance measurements were made at several frequencies on groups of four types of transistors at various amplifier load resistance values, and the results obtained are shown in Figures 3-13 and 3-14. In these plots each pair of similar lines indicates the limits of the impedance values obtained under the specified test condition.

a. Common-Base Amplifier Series Input Resistance

Figure 3-13 shows the behavior of the series input resistance of the various transistor types as a function of frequency. Comparison of the plots shows the same general pattern of behavior for all the transistor types. At low frequencies, the series input resistance is essentially independent of the load resistor value and is approximately equal to:

$$R_{in(s)} \approx r_e + r_{bb'} (1 - \alpha_o) \quad (3-62)$$

In the vicinity of 10 to 20 MC, depending on transistor type and emitter current level, $R_{in(s)}$ begins to increase above the value given by Equation (3-62) at a steadily increasing rate until a maximum is reached in the 40- to 80-MC range. The peak is then followed by an equally sharp decrease in $R_{in(s)}$, with resistance values at 100 MC approaching or less than the low-frequency value of $R_{in(s)}$.

This peculiar variation of the amplifier input resistance is due to the complex feedback occurring within the transistor. The initial increase is caused by negative feedback which is then counterbalanced at a higher frequency by a positive feedback component, causing the peak. The positive feedback then becomes dominant at higher frequencies, causing the input resistance to decrease. This is the positive feedback effect referred to previously as occurring in non-unilateralized amplifiers at high frequencies and which is capable of causing sustained oscillation. The plots of Figure 3-13 show that the series resistance was positive for all cases measured. However, the 2N2219 with a load resistance of 500 ohms has a series input resistance of 3 ohms or less at 100 MC, and it appears that the input resistance would be negative for some transistors of this type at this frequency with a load resistance of 1 K. The effect is less pronounced

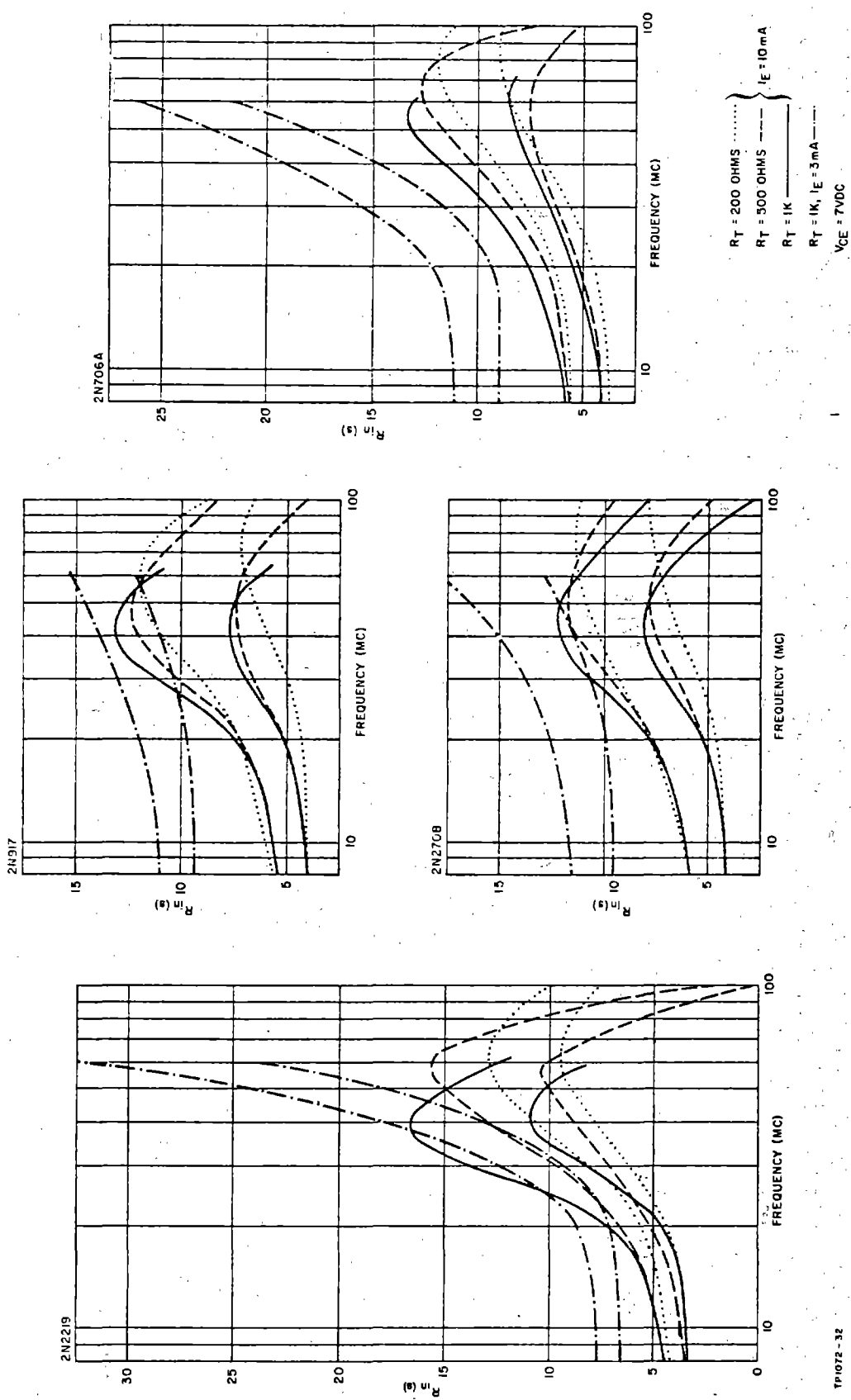


Figure 3-13. Common Base Amplifier Series
Input Resistance

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for the other types of transistor, and it appears that the input resistance will not be negative with a 1-K load resistance below 150 MC for these types.

The plots of Figure 3-13 show the behavior of the amplifier input resistance at the frequency to which the amplifier is tuned. It is also possible that, at frequencies adjacent to that to which the amplifier is tuned, the positive feedback will be increased due to the additional phase shift, to the point where the input resistance is negative. The oscillator stability will then be dependent on the resistance and reactance of the driving source. Oscillation may then occur if the driving source effective series resistance is smaller in magnitude than the negative amplifier input resistance, and if the source series reactance is equal in magnitude to the amplifier input reactance but of opposite sign. At frequencies above 30 MC where the positive feedback within the transistor is likely to cause a negative amplifier input resistance, only series resonance crystal units are employed. The crystal unit resonance resistance is in the range of 40 to 100 ohms, and a good crystal termination is obtained by inserting the crystal into the loop in series with the amplifier input. The crystal unit then constitutes the major part of the amplifier driving source impedance; and since its reactance can change rapidly for only small frequency changes, it is entirely possible that the driving source and amplifier input reactance cancellation can occur. A positive amplifier input resistance does not therefore guarantee that the amplifier will be sufficiently stable. Sustained oscillation at a frequency other than that of the crystal unit is unlikely because of the relatively large value of the crystal unit resonance resistance which has to be cancelled for this to occur. However, it is found that smaller amounts of positive feedback than that resulting in complete instability will cause undesirable characteristics of the crystal-controlled oscillation. Notable among these is the distortion of the oscillator tuning response and of the frequency-versus-temperature response. An example of this is a 50-MC oscillator using a 2N706A transistor where it was found that the amplifier load could not exceed 500 ohms because of these effects.

This appears to be an effect that can only be determined experimentally, and it may be necessary to redesign the oscillator at several amplifier load levels before a satisfactory oscillator is obtained.

b. Common-Base Amplifier Series Input Inductance

Figure 3-14 shows the behavior of the series inductive reactance $X_{L(s)}$ of the various transistor types as a function of frequency. Comparison of the plots shows the same general pattern of behavior, with the inductive reactance approximately doubling with every octave increase in frequency, indicating that over the frequency range of measurement the amplifier effective input inductance remains fairly constant.

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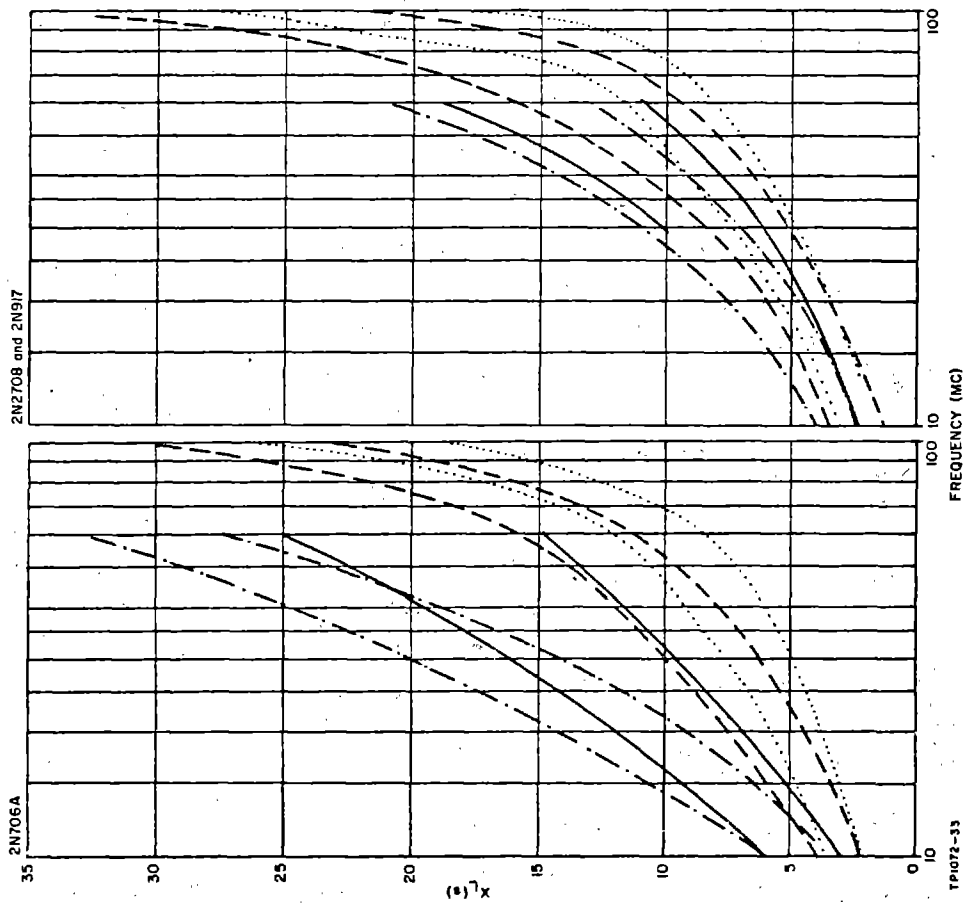
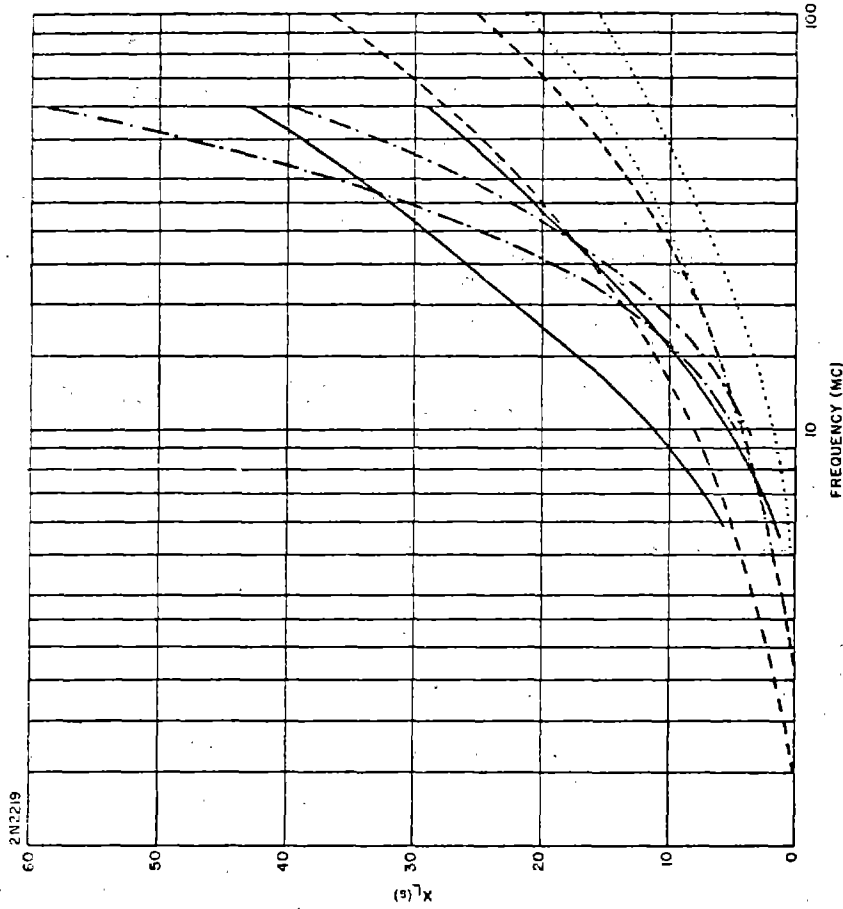


Figure 3-14. Common Base Amplifier Series
Input Inductance Reactance

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The inductive reactance approaches equality with the series resistance in the frequency range of 7 to 30 MC, depending on transistor type and amplifier load resistance; and, because of the peak in the amplifier input resistance characteristic, the input resistance and inductive reactance tend to increase approximately in unison for 1 or 2 octaves until the peak of input resistance occurs. At higher frequencies than that at which the peak of series input resistance occurs, the amplifier input impedance becomes predominantly inductive.

It has not been possible to find an equation which adequately characterizes the behavior of the amplifier input inductive component. However, at frequencies below 30 MC for an oscillator design where the crystal unit is inserted immediately preceding the amplifier and, as is good crystal unit terminating resistance practice, the amplifier series input resistance is small compared to the crystal resonance resistance, the combined resistance will be large compared to the inductive reactance, which will then have a negligible effect. This is further discussed in Section 7. At design frequencies above 30 MC, this no longer applies and experimental methods must be employed.

3-24. Equivalent Circuit of a Common-Emitter Transistor Amplifier with an Unbypassed Emitter Resistor

Although the transistor hybrid- π equivalent circuit does not adequately describe the behavior of a transistor amplifier for high voltage gain conditions, it does give reasonable accuracy when the amplifier voltage gain is low. It will subsequently be shown that for the Pierce oscillator the important amplifier characteristic is the product of voltage gain and parallel input resistance, and that no loss is incurred by decreasing the amplifier voltage gain provided that a proportional increase in input resistance is obtained. The inclusion of an unbypassed emitter resistance gives this result, as shown in the following analysis.

Referring to Figure 3-15, the object is to prove the equivalence of circuits (a) and (d). It is more convenient to show that (d) is equivalent to (a) than vice-versa.

For a given voltage $V_{b'e}$ across $R_{b'e}$, the current generator must be equal in both circuits (a) and (c) and therefore:

$$g_m \cdot V_{b'e} = G_M \cdot V_{b'E} \quad (3-63)$$

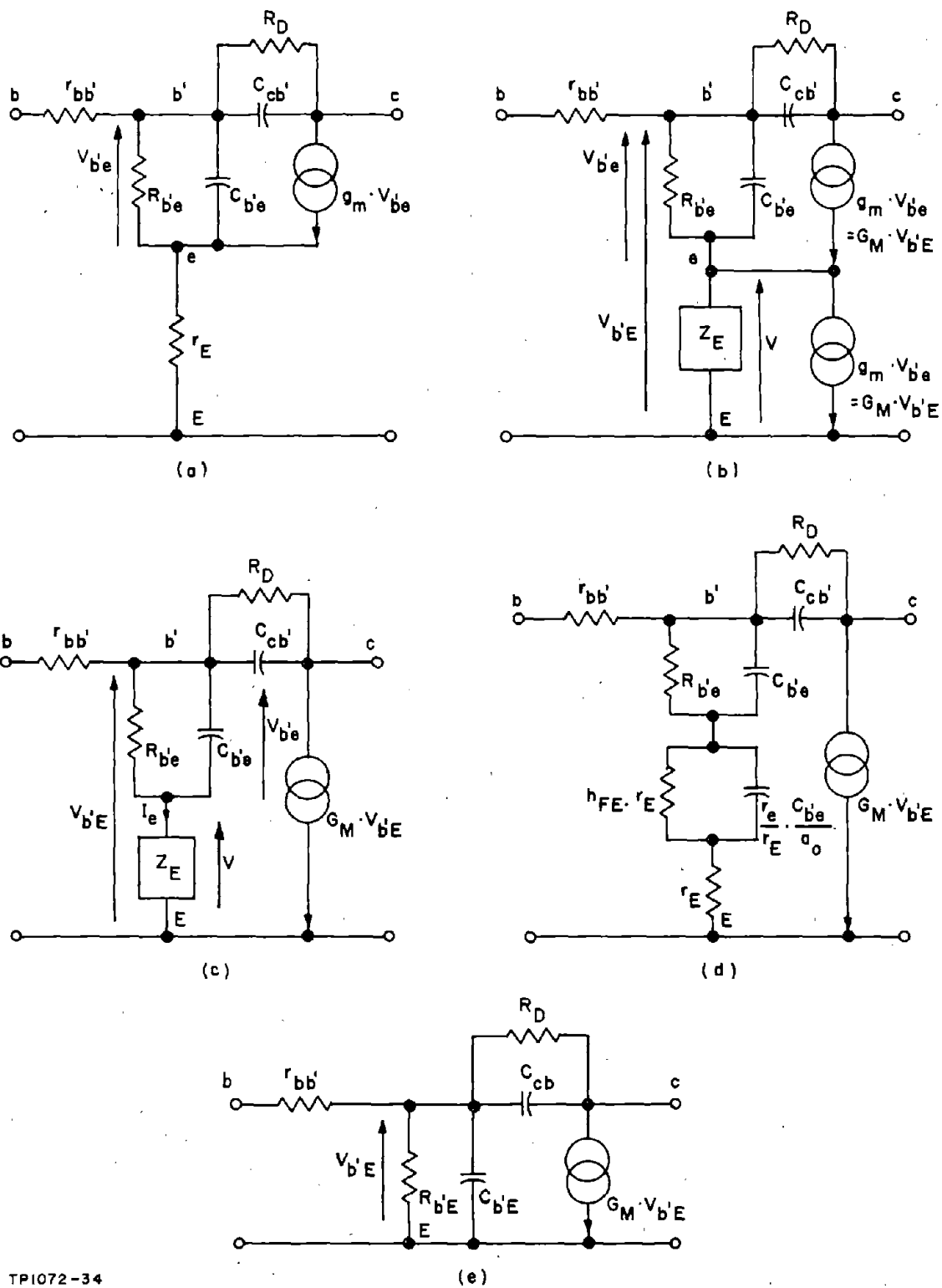
Also

$$V_{b'E} = V + V_{b'e} \quad (3-64)$$

and

$$\frac{V_{b'E}}{V_{b'e}} = \frac{I_e (Z_{b'e} + Z_E)}{I_e \cdot Z_{b'e}} = 1 + \frac{Z_E}{Z_{b'e}} \quad (3-65)$$

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Figure 3-15. Circuit Transformations Used in Analyzing Effect of an Unbypassed Emitter Resistor

Substituting for $V_{b'e}$ from Equation (3-63) into Equation (3-64) gives:

$$V_{b'E} = \frac{V}{1 - \frac{G_M}{g_m}} \quad (3-66)$$

The current generator of Figure 3-15 (c) can be rearranged as shown in Figure 3-15 (b) without changing the circuit conditions (the two generators are equal, and therefore the connection between the emitter (e) and the mid-point of the two generators will carry no current). The generator connected across Z_E now has the voltage V across its terminals and can be replaced by an impedance Z . From Equation (3-66):

$$Z = \frac{V}{G_M \cdot V_{b'E}} = \frac{1}{G_M} - \frac{1}{g_m} \quad (3-67)$$

From Equations (3-63) and (3-65):

$$\frac{1}{G_M} = \frac{V_{b'E}}{g_m \cdot V_{b'e}} = \frac{1}{g_m} \left[\frac{Z_E \left(1 + j \frac{R_{b'e}}{X_{Cb'e}} \right)}{R_{b'e}} + 1 \right] \quad (3-68)$$

Substituting from Equation (3-68) into Equation (3-67) gives:

$$Z = \frac{Z_E}{g_m \cdot R_{b'e}} \left(1 + j \frac{R_{b'e}}{X_{Cb'e}} \right) \quad (3-69)$$

For the circuits of (a) and (c) to be equivalent, the parallel combination of Z_E and Z must equal r_E . That is:

$$r_E = \frac{Z_E \left(1 + j \frac{R_{b'e}}{X_{Cb'e}} \right)}{g_m \cdot R_{b'e} \left[1 + \frac{\left(1 + j \frac{R_{b'e}}{X_{Cb'e}} \right)}{g_m R_{b'e}} \right]} \quad (3-70)$$

Transposing gives:

$$Z_E = \frac{r_E \left(1 + g_m R_{b'e} + j \frac{R_{b'e}}{X_{Cb'e}} \right)}{1 + j \frac{R_{b'e}}{X_{Cb'e}}} \quad (3-71)$$

But:

$$g_m \cdot R_{b'e} = h_{FE} \quad (3-72)$$

and

$$R_{b'e} = \frac{r_e}{1 - \alpha_0} \quad (3-73)$$

Therefore:

$$\begin{aligned} Z_E &= \frac{r_E}{1 - \alpha_0} \cdot \frac{1 + j \frac{r_e}{X_{C_{b'e}}}}{1 + j \frac{r_e}{(1 - \alpha_0) X_{C_{b'e}}}} \\ &= \frac{r_E}{1 - \alpha_0} \cdot \frac{1 + j \frac{f}{f_T}}{1 + j \frac{f}{(1 - \alpha_0) f_T}} \end{aligned} \quad (3-74)$$

Z_E is, therefore, the series - parallel combination shown in Figure 3-15 (d).

At frequencies well below f_T , the effect of the complex numerator term of Equation (3-74) will be small and can be ignored. With this approximation, Z_E behaves as a parallel combination of resistance and capacitance with a cutoff frequency at $\frac{f_T}{1 - \alpha_0}$. This is the same cutoff frequency exhibited by $R_{b'e}$ and $C_{b'e}$ and, therefore, these networks can be combined as shown in Figure 3-15 (e) where:

$$R_{b'E} = \frac{r_e + r_E}{1 - \alpha_0} = R_{b'e} \left(1 + \frac{r_E}{r_e} \right) \quad (3-75)$$

$$C_{b'E} = \frac{C_{b'e}}{1 + \frac{r_E}{r_e}} \quad (3-76)$$

$$G_M = \frac{\alpha_0}{r_e + r_E} = \frac{g_m}{1 + \frac{r_E}{r_e}} \quad (3-77)$$

This analysis shows that the effect of an unbypassed emitter resistor is to effectively increase $R_{b'e}$ and decrease $C_{b'e}$ and g_m by a factor of $\left(1 + \frac{r_E}{r_e}\right)$ in the equivalent circuit. Therefore, for amplifier loading or frequency conditions where the effects of voltage sensitive feedback within the transistor are small, the amplifier voltage gain is decreased and the input impedance increased by virtually equal amounts. That is, the product of input impedance and voltage gain is practically constant.

3-25. Transformer from Hybrid $-h$ to π (Admittance) Equivalent Transistor Circuit

In one type of Pierce oscillator to be subsequently considered, the bilateral behavior of a transistor poses difficulties in the analysis of the circuit and in the development of a design procedure. These difficulties are removed if the transistor equivalent circuit is divided into two parts; one part of which behaves as a unilateralized amplifier, and the other part, which represents the internal feedback within the transistor, is incorporated into the oscillator feedback network. The object of the following analysis is to effect this transformation of the transistor equivalent circuit.

It has been shown that, at frequencies below the cutoff frequency f_V , the hybrid- h equivalent transistor circuit, and hence circuits derived from it, adequately represent the behavior of a transistor amplifier. Therefore, for these conditions, the network conversion shown in Figure 3-16 is valid. The values of the π equivalent circuit elements are derived as follows.

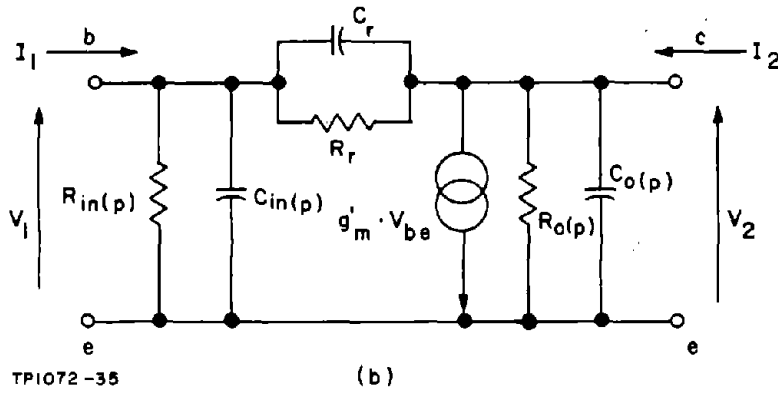
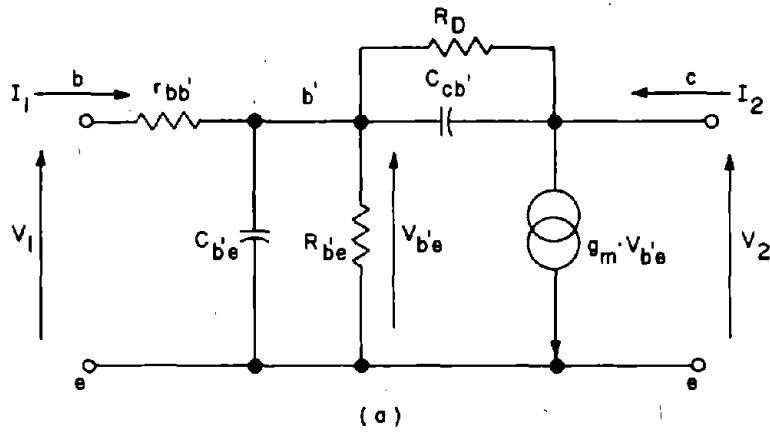
a. R_r and C_r (Y_r)

Y_r is the reverse transconductance from the transistor output terminals (c) and (e) to the short-circuited input terminals (b) and (e). The derivation of Y_r is simplified when it is noted that $V_{b'e}$ will be small compared to V_2 . This permits the base current due to R_D and $C_{cb'}$ to be calculated separately and combined by superposition. The resistive component of Y_r then consists of two parallel components. That is:

$$R_r = R_D \cdot \frac{(R_{b'e} + r_{bb'})}{R_{b'e}} \left[1 + \left(\frac{r}{X_{C_{b'e}}} \right)^2 \right] \quad (3-78)$$

in parallel with

$$r_{bb'} \left[1 + \frac{C_{be'}}{X_{C_{b'e}}} + \frac{X_{C_{cb'}} \cdot X_{C(p)}}{r^2} \right]$$



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Figure 3-16. Hybrid- π and π Equivalent Transistor Circuits

where

$$r = \frac{r_{bb'} \cdot R_{b'e}}{r_{bb'} + R_{b'e}} \quad (3-79)$$

and

$$X_{C(p)} = \frac{1}{\omega(C_{b'e} + C_{cb'})} \quad (3-80)$$

The capacitive component of Y_r is:

$$C_r = (C_{cb'} + \frac{r}{R_D} \cdot C_{b'e}) \frac{R_{b'e}}{(r_{bb'} + R_{b'e}) \left[1 + \left(\frac{r}{X_{C_{b'e}}} \right)^2 \right]} \quad (3-81)$$

b. $Y_f (g'_m)$

Y_f is the forward transconductance from the transistor input terminals (b) and (e) to the short-circuited output terminals (c) and (e), neglecting the current through R_D and C_{ob}' . That is:

$$g'_m = g_m \frac{R_{b'e}}{(r_{bb'} + R_{b'e}) (1 + j \frac{r}{X_{C(p)}})} \quad (3-82)$$

c. $R_{o(p)}$ and $C_{o(p)}$ (Y_o)

Y_o is the admittance appearing between terminals (c) and (e) due to the activation of the current generator by the current passing through R_D and C_{cb}' in response to V_2 when terminals (b) and (e) are short-circuited. Because of the relative values of $V_{b'e}$ and V_2 , the currents through R_D and C_{cb}' can again be considered separately giving:

$$R_{o(p)} = R_D \cdot \frac{r_e}{\alpha_o \cdot r} \left[1 + \left(\frac{r}{X_{C_{b'e}'}} \right)^2 \right] \quad (3-83)$$

in parallel with

$$\frac{r_e}{\alpha_o \cdot r} \left[1 + \frac{C_{b'e}'}{C_{cb}'} + \frac{X_{C_{cb}'} \cdot X_{C(p)}}{r^2} \right]$$

$$C_{o(p)} = \frac{\alpha_o \cdot r}{r_e \left[1 + \left(\frac{r}{X_{C(p)}} \right)^2 \right]} \left\{ C_{cb}' + \frac{r}{R_D} \cdot C_{b'e}' \right\} \quad (3-84)$$

d. Y_{in}

Y_{in} is the admittance at the input terminals (b) and (e) when the output terminals (c) and (e) are short-circuited. Y_{in} includes R_r and C_r , and the admittance required to determine $R_{in(p)}$ and $C_{in(p)}$ alone is:

$$Y'_{in} = Y_{in} - Y_r \quad (3-85)$$

However, R_D and C_{cb}' are much larger than $R_{b'e}$ and $C_{b'e}$ and Y_{in} is practically equal to the admittance of $r_{bb'}$, $C_{b'e}'$, and $R_{b'e}$.

then:

$$R_{in(p)} = (r_{bb'} + R_{b'e}) \left[\frac{1 + \left(\frac{r}{X_{C_{b'e}'}} \right)^2}{1 + \frac{R_{b'e} \cdot r}{X_{C_{b'e}'}}} \right] \quad (3-86)$$

and:

$$C_{in(p)} = C_{b'e} \left(\frac{R_{b'e}}{R_{b'e} + r_{bb'}} \right)^2 \left[\frac{1}{1 + \left(\frac{r}{X_{C_{b'e}}} \right)^2} \right] \quad (3-87)$$

These equations also apply when emitter degeneration is used, provided $R_{b'E}$, $C_{b'E}$, $(C_{b'E} + C_{cb'})$, and G_M are substituted for $R_{b'e}$, $C_{b'e}$, $(C_{b'e} + C_{cb'})$, and g_m , respectively. The effects of emitter degeneration can be determined by considering these substitutions in Equations (3-78) to (3-87). These are:

- (a) C_r will remain almost constant with, possibly, a small decrease in value caused by the effective decrease in $C_{b'e}$.
- (b) The component of R_r due to R_D will decrease slightly while that component due to $X_{C_{b'e}}$, which is virtually proportional to $X_{C_{b'e}}$, will increase rapidly with increasing r_E .
- (c) G'_M will decrease rapidly with increasing r_E .
- (d) $R_{O(p)}$ is proportional to r_E and will increase.
- (e) $R_{in(p)}$ increases with increasing r_E .
- (f) $C_{in(p)}$ decreases with increasing r_E . Therefore, C_r is the only circuit element practically unaffected by emitter degeneration.

3-26. Common-Emitter Amplifier Input Resistance Due to the Transistor Base-Biasing Network

The base biasing network of the transistor amplifier is in parallel with the transistor input and, consequently, places an additional parallel resistive load across the amplifier input terminals. The value of this load $R_{b(p)}$ is the parallel combination of the base-to-B+ resistor R_{b1} and the base-to-ground resistor R_{b2} . It will be subsequently shown that the attenuation of the feedback network in a Pierce oscillator is dependent on the amplifier parallel input resistance, requiring a larger attenuation and therefore a larger amplifier voltage gain as the amplifier parallel input resistance is decreased. It is therefore desirable to make $R_{b(p)}$ as large as possible commensurate with maintaining adequate stability of the transistor operating point with the transistor interchange and with temperature variations. Three effects have to be considered:

- (a) For the normal practice of batching transistors for a maximum-to-minimum h_{FE} ratio of 3 to 1, interchange of transistors will cause a possible 3-to-1 change in base current for a constant emitter current.

- (b) Over the temperature range of -55 to $+105^{\circ}\text{C}$, the expected variation of h_{FE} is typically from 60 percent of the 25°C value at -55°C to 150 percent of the 25°C value at $+105^{\circ}\text{C}$.
- (c) The variation of the base-to-emitter DC voltage with temperature is approximately 2 MV per degree Centigrade. For the 160°C range considered, the total change in V_{BE} will therefore be 320 MV.

The following discussion considers (a) and (b) and relates these effects to a transistor having the minimum value of h_{FE} of its type. For a given emitter current, let X milliamperes of base current be required at 25°C . Then, at -55°C , the base current required to maintain the emitter current constant will be $1.67X$ MA. Consider next a transistor of the same type having a maximum value of h_{FE} (assumed here to be 3 times the minimum value). The base current required for the given emitter current will now be $\frac{X}{3}$ MA at 25°C . And at $+105^{\circ}\text{C}$ it will decrease to $\frac{X}{4.5}$ MA. The total range of base current variation is therefore 7.5 to 1.

The transistor biasing network to be considered is as shown in Figure 3-17, and the problem is that of determining the maximum values of R_{b1} and R_{b2} that can be used while maintaining V_{BG} , and hence I_E , reasonably constant with the 7.5:1 possible variation of I_B . For a given change ΔV_{BG} in V_{BG} , the change in I_{B2} is:

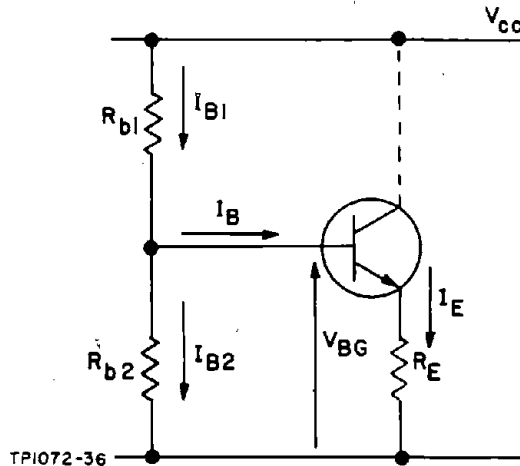


Figure 3-17. Circuit Used for Base-Biasing Network Analysis

$$\Delta I_{B2} = \frac{\Delta V_{BG}}{V_{BG}} \cdot I_{B2} \quad (3-88)$$

And the change in I_{B1} is:

$$\Delta I_{B1} = -\frac{\Delta V_{BG}}{V_{CC} - V_{BG}} \cdot I_{B1} \quad (3-89)$$

The change in I_B for the given change in V_{BG} is:

$$\Delta I_B = - (\Delta I_{B1} + \Delta I_{B2}) \quad (3-90)$$

Substituting for ΔI_{B1} and ΔI_{B2} gives:

$$\frac{\Delta I_B}{I'_B} = - \frac{\Delta V_{BG}}{V_{BG}} \left[\frac{I_{B1}}{I'_B} \cdot \frac{V_{BG}}{V_{CC} - V_{BG}} + \frac{I_{B2}}{I'_B} \right] \quad (3-91)$$

where I'_B is a current whose value lies intermediate to the two extremes and which will be determined later. The current ratios $\frac{I_{B2}}{I'_B}$ and $\frac{I_{B1}}{I'_B}$ are related by the condition:

$$\frac{I_{B2}}{I'_B} = \frac{I_{B1}}{I'_B} - 1 \quad (3-92)$$

The possible 7.5 to 1 range of variation of I_B is related to ΔI_B and I'_B by the equation:

$$\frac{I'_B + \Delta I_B}{I'_B - \Delta I_B} = 7.5 \quad (3-93)$$

or

$$\frac{\Delta I_B}{I'_B} = \pm 0.765 \quad (3-94)$$

By inserting values of V_{BG} , V_{CC} , and the desired ratio of $\frac{\Delta V_{BG}}{V_{BG}}$ into Equation (3-91), together with compatible values of the ratios $\frac{I_{B1}}{I'_B}$ and $\frac{I_{B2}}{I'_B}$, the fractional change in I_B is obtained. If the value of $\frac{\Delta I_B}{I'_B}$ obtained is equal to or greater than 0.765, the transistor biasing network meets the base voltage variation requirements.

Having obtained the required ratios of I_{B1} and I_{B2} to I'_B , substituting for I'_B gives I_{B1} and I_{B2} and hence, R_{b1} and R_{b2} . I'_B is calculated from:

$$I'_B = \frac{I_E}{1.06 [h_{FE}(\text{min at } 25^\circ\text{C}) + 1]} \quad (3-95)$$

Equation (3-95) is obtained from consideration of the maximum base current at -55°C .

As previously stated, the base current of a transistor at -55°C is approximately 167 percent of its 25°C value. Also, the base current of a transistor having a minimum h_{FE} value at -55°C is given by Equation (3-94) as $1.765 I'_B$. Relating these gives:

$$1.67 I_B (h_{FE} \text{ min at } 25^{\circ}\text{C}) = 1.765 I'_B \quad (3-96)$$

or

$$I'_B = \frac{I_B (h_{FE} \text{ min at } 25^{\circ}\text{C})}{1.06} \quad (3-97)$$

I_B is related to I_E by:

$$I_B = \frac{I_E}{h_{FE} + 1} \quad (3-98)$$

The following example, which is used later in an oscillator design, illustrates the procedure:

$$V_{CC} = 28 \text{ VDC}$$

$$V_{BG} = 18 \text{ VDC}$$

$$h_{FE \text{ min}} = 85$$

$$I_E = 35 \text{ MA}$$

If an emitter current change of ± 12 percent is considered permissible, the allowable variation in V_{BG} is:

$$\Delta V_{BG} = \pm 0.12 \times 18 = \pm 2.2 \text{ V}$$

If:

$$\frac{I_{B1}}{I'_B} = 2.6$$

and:

$$\frac{I_{B2}}{I'_B} = 1.6$$

Then:

$$\frac{\Delta I_B}{I'_B} = 0.77$$

The condition of Equation (3-94) is therefore satisfied.

Then:

$$I'_B = \frac{35}{106 \times 86} = 0.38 \text{ MA}$$

and:

$$I_{B1} = 1 \text{ MA}$$

$$I_{B2} = 0.6 \text{ MA}$$

giving:

$$R_{b1} = 10 \text{ K}$$

$$R_{b2} = 30 \text{ K}$$

The input resistance of the base biasing network is then:

$$R_{b(p)} = 7.5 \text{ K}$$

This is the maximum value that $R_{b(p)}$ can have for this emitter current at the given transistor bias point.

The effect of the emitter-base voltage change with temperature on the emitter current will be negligible, amounting to approximately $\pm 160 \text{ MV}$ in 18 V . For emitter-to-ground voltages of less than, say, 3 volts, this effect will play an increasing part in the transistor operating point instability and must also be considered.

SECTION 4

IMPEDANCE TRANSFORMING NETWORKS

4-1. GENERAL

Because of the large differences in impedance level likely to occur between the crystal unit and the active device, at least one impedance transforming network is usually necessary in an oscillator circuit. Possible applications of impedance transforming networks in oscillators are:

- (a) To transform the impedance level of the feedback network to that required at the active device output
- (b) To transform the input impedance of the active device to a suitable terminating level for the feedback network
- (c) To transform the oscillator external load to a level suitable for connection to the active device.

In applications (a) and (b) an additional requirement has to be met. Not only must the network transform impedance levels, it must also introduce a desired amount of phase shift between input and output. This will nominally be 0 degree or 180 degrees, depending on the oscillator configuration; but it may be desirable to introduce small additional phase shifts to compensate for those introduced in other parts of the circuit. A definite objective in designing an impedance transforming network is, therefore, to obtain a desired phase angle, and design processes resulting in this objective are required.

Commonly used impedance transforming networks are shown in Figure 4-1. These networks are normally used in conjunction with a tuning reactance as shown in dashed lines in (a) to (e). These components play no part in the impedance transforming action, their function being solely to tune out the reactive component reflected across the input terminals. These networks, or the tuning coil in the case of (d), contain resistive elements in the form of coil losses that result in power loss. This power loss reduces the efficiency of power transfer through the network and must be accounted for in the oscillator design.

The impedance transforming network characteristics that are required are:

- (a) The impedance transforming ratio
- (b) The input-output voltage ratio

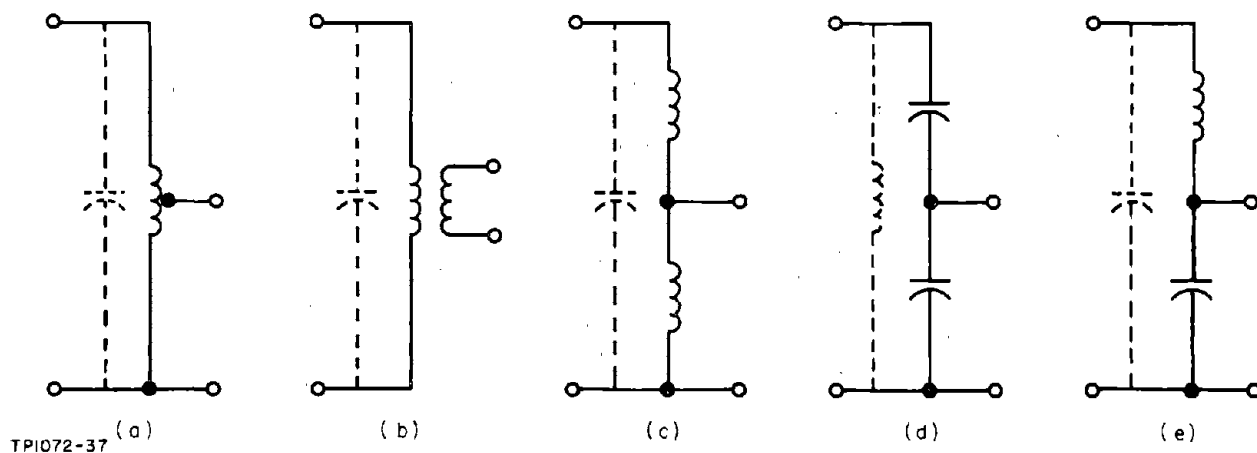


Figure 4-1. Impedance Transforming Networks

(c) The input-output phase angle

(d) The efficiency of power transfer

The operation of the networks shown in Figure 4-1 are analyzed below, and design equations are developed from these analyses.

4-2. π NETWORK

The useful property of this network, in addition to its impedance transforming characteristic, is its phase inverting action between input and output when the component values are chosen appropriately. This characteristic is useful when the power amplifier phase angle is close to 180 degrees. Above 20 or 30 MC, crystal units are normally used in a manner giving zero phase angle transmission at an impedance level suitable for grounded cathode or base operation. Consequently, unless two impedance transforming networks are used in the feedback loop (a configuration usually not justified on the grounds of complexity when an alternative is available), the usage of the network is confined to frequencies below 20 to 30 MC. It can, however, be used at all frequencies for matching to the oscillator load.

The following analysis is based on the practical aspects of the network and is intended to show how the impedance transformation occurs. This is not the most elegant approach, but it is believed to yield a better practical appreciation of the impedance transforming action of the network. The analysis is developed through the series-parallel circuit transformations given in Figure 4-2 which show only that portion of the network active in the impedance transforming function; the capacitor placed across the input to tune with L' is not shown. The load resistance r_s in this circuit is representative of the parallel resistance of the succeeding circuit. The parallel reactive component of this circuit is considered to form part of C.

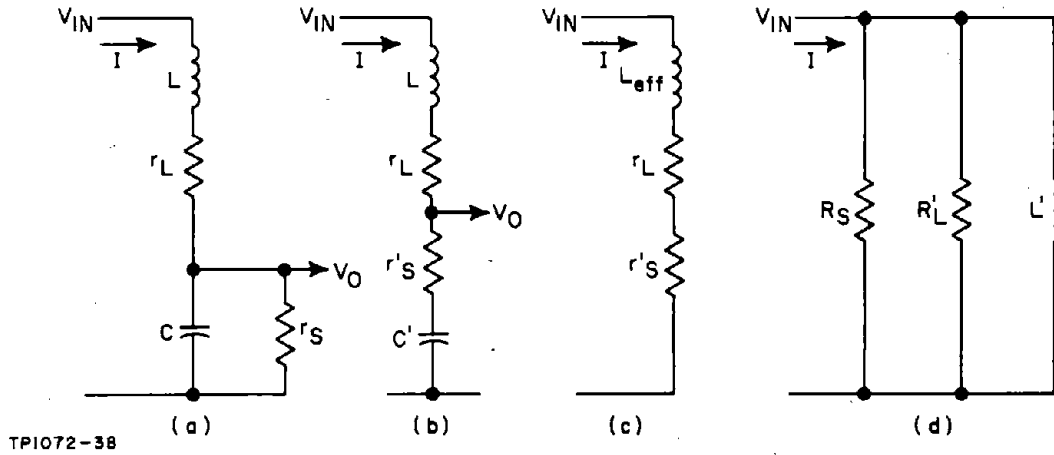


Figure 4-2. π Network Transformations

Transforming from (a) to (b), Figure 4-2, the relationships between r'_s and r_s and C' and C (Table 1-3, c) are:

$$r'_s = r_s \left[\frac{1}{1 + \left(\frac{r_s}{X_C} \right)^2} \right] \quad (4-1)$$

and

$$C' = C \left[1 + \left(\frac{X_C}{r_s} \right)^2 \right] \quad (4-2)$$

Transforming from (b) to (c), Figure 4-2, gives:

$$X_{Leff} = X_L - X_{C'} \quad (4-3)$$

Transforming from (c) to (d), Figure 4-2 (Table 1-3, b):

$$\frac{R_s \cdot R'_L}{R_s + R'_L} = (r'_s + r_L) \left[1 + \left(\frac{X_{Leff}}{r'_s + r_L} \right)^2 \right] \quad (4-4)$$

and

$$X_{L'} = X_{Leff} \left[1 + \left(\frac{r'_s + r_L}{X_{Leff}} \right)^2 \right] \quad (4-5)$$

The values of R_s and R'_L can be obtained separately by equating r_L and r'_s to zero, respectively, in Equation (4-4).

The voltage attenuation ratio A_V is obtained from Figure 4-2 (b) and (c) as:

$$A_V = \frac{V_o}{V_{in}} = \frac{r'_s - jX_{C'}}{r_L + r'_s + jX_{Leff}} \quad (4-6)$$

And when $r_L + r'_s$ and r'_s are smaller than $\frac{\omega_{Leff}}{3}$ and $\frac{1}{3\omega C'}$, respectively, which will be necessary if the phase angle is to approach 180 degrees, Equation (4-6) can be approximated with less than 10 percent error as:

$$A_V \approx - \frac{X_{C'}}{X_{Leff}} \quad (4-7)$$

Further, for the prescribed condition, Equations (4-1) and (4-2) show that the value of C' is within 10 percent of C and therefore:

$$A_V \approx - \frac{X_C}{X_{Leff}} \quad (4-8)$$

From power transfer considerations the impedance transformation ratio can also be written as:

$$\begin{aligned} T_r &= \frac{R_s}{r_s} \\ &= \frac{1}{A_V^2} \end{aligned} \quad (4-9)$$

The power transfer efficiency is:

$$E = \frac{r'_s}{r'_s + r_L} = \frac{R'_L}{R_L + R_s} \quad (4-10)$$

The phase angle of the current I relative to V_{in} is:

$$\phi_I = \tan^{-1} \frac{X_{Leff}}{r'_s + r_L} \quad (\text{Lagging}) \quad (4-11)$$

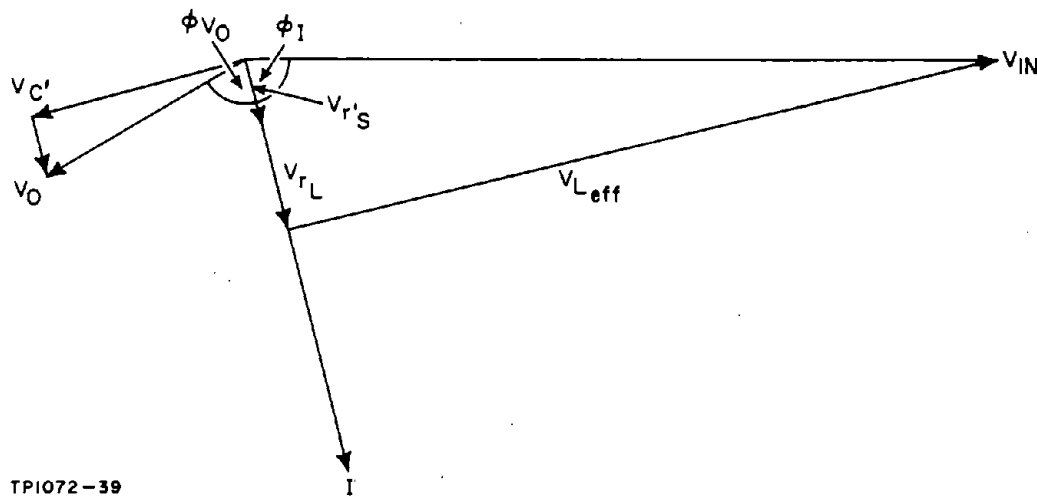
The phase angle of V_o relative to I is:

$$\phi_{V_o} = \tan^{-1} \frac{X_{C'}}{r'_s} \quad (\text{Lagging}) \quad (4-12)$$

The phase lag of V_O relative to V_{in} is, therefore:

$$\phi_I + \phi_{V_O} = \tan^{-1} \frac{X_{Leff}}{r'_s + r_L} + \tan^{-1} \frac{X_{C'}}{r'_s} \quad (4-13)$$

Figure 4-3 illustrates the vector relationships between the various quantities, and shows that for any practical network there will exist a phase lag of V_O relative to V_{in} which can approach, but never exceed, 180 degrees. The difference from 180 degrees is due to the finite Q of the coil and the presence of r_s in the circuit.



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Figure 4-3. π Network Vector Relationships

4-3. π Network Design

When used in the feedback loop, the known requirements for the network are:

- The value of R_S . The known ratio of output power to feedback power determines R_S .
- The value of r_s . This is the value of the parallel input resistance of the succeeding network.
- The value of the succeeding networks' parallel input reactance. If this is capacitive, it may determine the minimum value of C .
- The desired phase shift deviation from 180 degrees may be known.

The network unknowns are C , r_L , and L . With this number of unknowns the network design becomes involved, especially when phase requirements have to be met. A relatively rapid method that enables the designer to pay constant attention to these requirements is the graphical approach outlined below. This is based on the vector diagram of Figure 4-3.

Since r_s and R_s are known and represent the same power dissipation, the ratio of V_o/V_{in} can be calculated as follows:

$$\frac{V_{in}}{V_o} = \sqrt{\frac{R_s}{r_s}} \quad (4-14)$$

Using suitable scaling, draw a line of length V_{in} on the reference axis. From the origin of the vector V_{in} , draw a partial circle of radius V_o in the third quadrant. Bisect V_{in} and, using this point as origin, draw a semicircle in the fourth quadrant of diameter V_{in} . These two circular segments are the loci of V_o and $V(r'_s + r_L)$, respectively. If the required phase angle between V_o and V_{in} is known, the vector V_o can be drawn; if not, a value must be assumed.

Specifying any one of the remaining four vector quantities will automatically complete the design, since V_{Leff} and $V_{C'}$ are in opposition to each other and mutually perpendicular to $V_{r's}$ and $V(r'_s + r_L)$. The choice resolves into the assumption of a value ϕ_I , and the following factors may influence this choice. For a fixed phase angle between V_o and V_{in} , the value of ϕ_I used determines the power transfer efficiency E , since:

$$E = \frac{r'_s}{r'_s + r_L} = \frac{V_{r's}}{V(r'_s + r_L)} \quad (4-15)$$

As ϕ_I approaches 90 degrees, the efficiency increases. This is the same as saying the coil losses approach zero. This may be an important factor in the design of low gain amplifier circuits.

Using these factors as a design basis, a value for ϕ_I can be selected; and the values of C , L , and r_L can be calculated, using Equations (4-16) through (4-20). It should be noted that in these equations $V_{r's}$, $V_{C'}$, V_{Leff} , and V_{r_L} are voltage magnitudes.

$$r'_s = r_s \cdot \frac{V_{r's}^2}{V_o^2} \quad (4-16)$$

$$X_{C'} = r'_s \cdot \frac{V_{C'}}{V_{r's}} \quad (4-17)$$

$$X_C = X_{C'} \left[1 + \frac{r_s'^2}{X_{C'}^2} \right] \quad (\text{Table 1-3, d}) \quad (4-18)$$

$$X_{Leff} = X_{L'} \frac{1}{1 + \left[\frac{V(r_s' + r_L)}{V_{Leff}} \right]^2} \quad (\text{Table 1-3, b}) \quad (4-19)$$

$$X_L = X_{Leff} + X_{C'} \quad (4-20)$$

$$r_L = r_s' \cdot \frac{V_{r_L}}{V_{r_s'}} \quad (4-21)$$

The Q of the inductance is:

$$Q_L = \frac{X_L}{r_L} \quad (4-22)$$

If this Q is not a feasible value (either too small or too large), the design can be optimized by recalculating, using a new value of ϕ_I . Increasing ϕ_I will require a higher Q for the coil and vice-versa. A typical design is shown in Figure 4-4.

4.4 CAPACITIVE DIVIDER NETWORK

This network introduces near to zero phase angle when properly terminated. Its major advantages are the control of phase angle that can be obtained by varying the values of C_1 and C_2 and the simplicity of design.

The circuit to be analyzed is shown in Figure 4-5 where C_1 and C_2 form the impedance transforming network and r_s is the load.

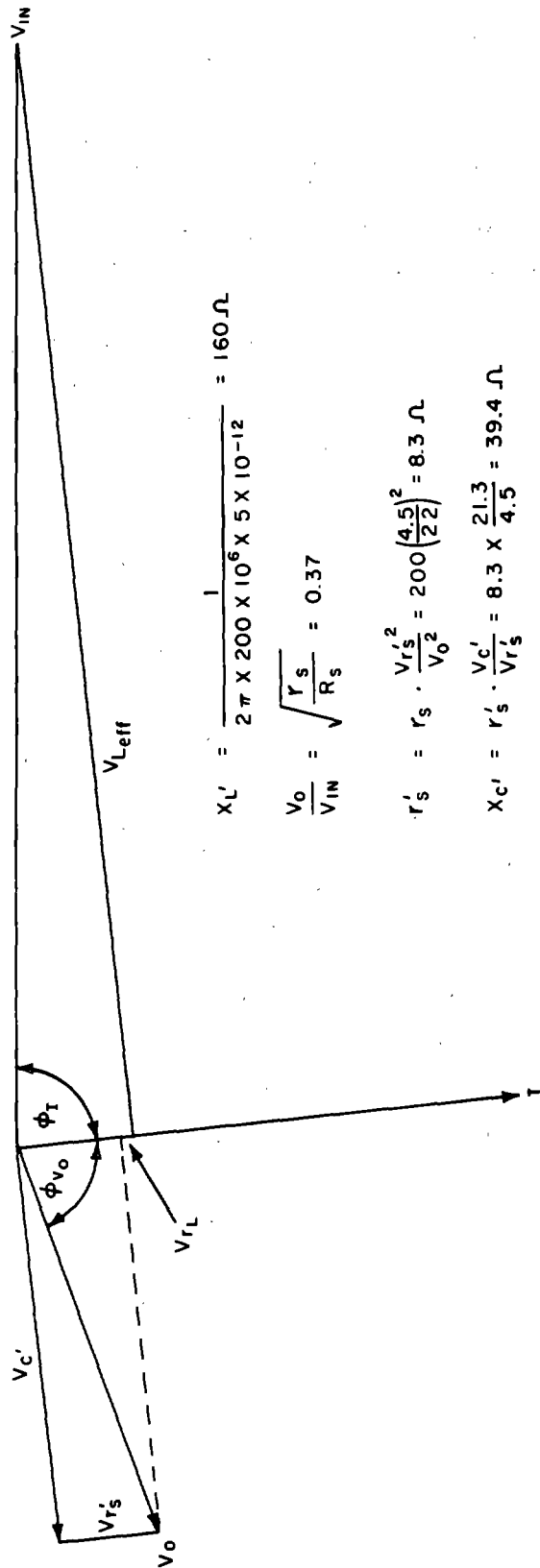
The voltage attenuation ratio of this network is:

$$\begin{aligned} A_V &= \frac{V_2}{V_1} \\ &= r_s \cdot \frac{j\omega C_1}{1 + j\omega (C_1 + C_2) r_s} \\ &= \frac{\omega C_1 r_s}{\sqrt{1 + \omega^2 (C_1 + C_2)^2 r_s^2}} \angle 90^\circ - \tan^{-1} \omega (C_1 + C_2) r_s \quad (4-23) \end{aligned}$$

DESIGN INFORMATION:

$r_s = 200 \Omega$; $R_s = 1.5 K$; TO BE USED AT 200 MC WITH APPROXIMATELY 5pF TUNING CAPACITANCE

PHASE ANGLE OF V_o RELATIVE
TO V_{in} TO BE 160° (LAGGING)



$$X_L' = \frac{1}{2\pi \times 200 \times 10^6 \times 5 \times 10^{-12}} = 160 \Omega$$

$$\frac{V_o}{V_{in}} = \sqrt{\frac{r_s}{R_s}} = 0.37$$

$$r_s' = r_s \cdot \frac{V_{r_s}^2}{V_o^2} = 200 \left(\frac{4.5}{22} \right)^2 = 8.3 \Omega$$

$$X_C' = r_s' \cdot \frac{V_C'}{V_{r_s}} = 8.3 \times \frac{21.3}{4.5} = 39.4 \Omega$$

$$X_C = X_C' \left[1 + \frac{r_s'}{X_C'} \right] = 39.4 \left[1 + \frac{8.3}{39.4} \right] = 48 \Omega$$

$$X_{Leff} = X_L' \cdot \frac{1}{1 + \left[\frac{V(r_s' + r_L)}{V_{Leff}} \right]^2} = 160 \cdot \frac{1}{1 + \left(\frac{0.64}{6} \right)^2} = 120 \Omega$$

$$X_L = X_{Leff} + X_C' = 160 \Omega$$

$$r_L = r_s' \cdot \frac{V_{r_L}}{V_{r_s}} = 8.3 \times \frac{0.5}{5} = 0.83 \Omega$$

$$Q = \frac{X_L}{r_L} = \frac{160}{.83} = 190$$

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Figure 4-4. Example of π Network Design

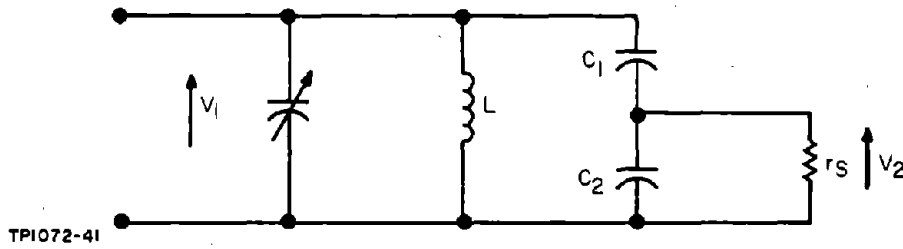


Figure 4-5. Capacitive Divider Coupling Network

Usually the phase lead required from the network to correct for phase lags occurring in the other parts of the loop will not be greater than 20 to 30 degrees; that is, $\tan^{-1} \omega (C_1 + C_2) r_S$ will be greater than 60 degrees. $\tan 64^\circ$ is approximately equal to 2 and, therefore, the minimum likely value of $\omega (C_1 + C_2) r_S$ is 2.

For the condition $\omega (C_1 + C_2) r_S \geq 2$, the magnitude of the voltage attenuation ratio can be simplified with a maximum error of 12 percent to:

$$A_V = \frac{C_1}{C_1 + C_2} \quad (4-24)$$

The power dissipation of the transformed load resistance R_S is equal to that of r_S . That is:

$$\frac{V_1^2}{R_S} = \frac{V_2^2}{r_S} \quad (4-25)$$

The transformation ratio T_r is, therefore:

$$\begin{aligned} T_r &= \frac{R_S}{r_S} \\ &= \left(\frac{V_1}{V_2} \right)^2 = \frac{1}{A_V^2} \end{aligned} \quad (4-26)$$

Substituting from Equation (4-23) into Equation (4-26) gives:

$$T_r = \frac{1 + \omega^2 (C_1 + C_2)^2 r_S^2}{\omega^2 C_1^2 r_S^2} \quad (4-27)$$

When $\omega (C_1 + C_2) r_S \geq 3$, Equation (4-27) simplifies to:

$$T_r \approx \left(\frac{C_1 + C_2}{C_1} \right)^2 \quad (4-28)$$

The relative values of $X(C_1 + C_2)$ and r_s required for various phase angles can be found from the phase angle term of Equation (4-23). The phase of V_2 relative to V_1 is:

$$\phi = 90^\circ - \tan^{-1} \frac{r_s}{X(C_1 + C_2)} \quad (4-29)$$

Therefore:

$$\phi = 10 \text{ degrees when } r_s \approx 6 X(C_1 + C_2)$$

$$\phi = 18 \text{ degrees when } r_s \approx 3 X(C_1 + C_2)$$

$$\phi = 26 \text{ degrees when } r_s \approx 2 X(C_1 + C_2)$$

This is the phase shift due to the relative values of $(C_1 + C_2)$ and r_s . The tuning of this network by an inductor can also introduce a phase angle if mistuning occurs.

The input capacitance of the network at the input terminals is:

$$C = C_1 \left[\frac{1 + \frac{r_s^2}{X_{C_2} \cdot X(C_1 + C_2)}}{1 + \frac{r_s^2}{X(C_1 + C_2)^2}} \right] \quad (4-30)$$

For the condition $\omega (C_1 + C_2) r_s \geq 2$, this simplifies to:

$$C = \frac{C_1 \cdot C_2}{C_1 + C_2} \quad (4-31)$$

4-5. INDUCTIVE TRANSFORMER

The circuit to be analyzed is shown in Figure 4-6, where

L_1 is the primary winding inductance

n_1 is the number of turns of the primary winding

L_2 is the secondary winding inductance

n_2 is the number of turns of the secondary winding

r_s is the load resistance in the secondary circuit

k is the coefficient of coupling of the windings

M is the mutual inductive coupling between the windings

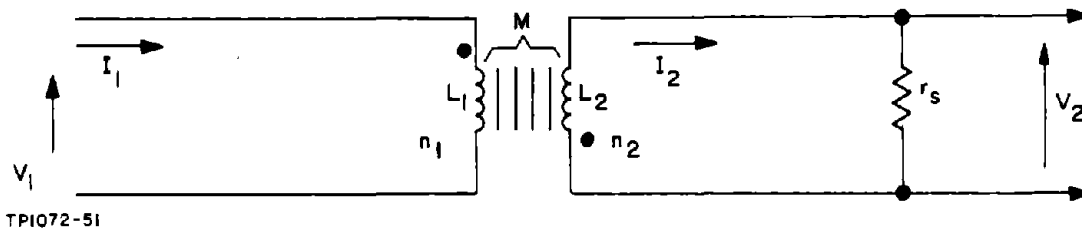


Figure 4-6. Inductive Transformer

M , k , L_1 , and L_2 are related by the expression:

$$M = k \sqrt{L_1 \cdot L_2} \quad (4-32)$$

The relationship between the primary and secondary winding inductances and number of turns is:

$$\frac{L_1}{L_2} = \left(\frac{n_1}{n_2} \right)^2 \quad (4-33)$$

The dots in Figure 4-6 indicate the polarities of the windings. The analysis is presented for the nominally phase-inverting transformer, but is equally valid for the nominally zero phase-shift transformer if a 180-degree phase shift of the secondary winding relationships is introduced. The resistance of the windings is assumed to be negligible in comparison to r_s and the driving source resistance.

The loop equations for the circuit of Figure 4-6 are:

$$V_1 = I_1 \cdot j\omega L_1 + I_2 \cdot j\omega M \quad (4-34)$$

$$0 = I_1 \cdot j\omega M + I_2 (r_s + j\omega L_2) \quad (4-35)$$

From these:

$$V_2 = I_2 \cdot r_s = \frac{-I_1 \cdot j\omega M \cdot r_s}{r_s + j\omega L_2} \quad (4-36)$$

and

$$V_1 = I_1 \left[j\omega L_1 + \frac{\omega^2 M^2 (r_s - j\omega L_2)}{r_s^2 + \omega^2 L_2^2} \right] \quad (4-37)$$

Because of the large number of variables involved, a general analysis is difficult and attention is confined to two particular cases often met in practice. The first of these is when the secondary winding inductive reactance is large compared to the secondary load resistance; the second, when the secondary load resistance is large compared to the secondary winding reactance. When

$\omega L_2 \geq 3r_s$, Equation (4-37) simplifies to:

$$V_1 \approx I_1 k^2 \frac{L_1}{L_2} r_s \left[1 + j \frac{\omega L_2}{r_s} \left(\frac{1-k^2}{k^2} \right) \right] \quad (4-38)$$

$$\approx I_1 k^2 \frac{L_1}{L_2} r_s \sqrt{1 + \frac{\omega^2 L_2^2}{r_s^2} \left(\frac{1-k^2}{k^2} \right)^2} \angle \tan^{-1} \frac{\omega L_2}{r_s} \left(\frac{1-k^2}{k^2} \right) \quad (4-39)$$

For the prescribed relative values of ωL_2 and r_s , Equation (4-36) can be approximated as:

$$\begin{aligned} V_2 &\approx -I_1 \frac{Mr_s}{L_2} \angle 90^\circ - \tan^{-1} \frac{\omega L_2}{r_s} \\ &\approx -I_1 k \sqrt{\frac{L_1}{L_2}} r_s \angle 90^\circ - \tan^{-1} \frac{\omega L_2}{r_s} \end{aligned} \quad (4-40)$$

The primary-to-secondary voltage ratio is then:

$$\frac{V_2}{V_1} \approx - \frac{\sqrt{\frac{L_2}{L_1}}}{k \sqrt{1 + \frac{\omega^2 L_2^2}{r_s^2} \left(\frac{1-k^2}{k^2} \right)^2}} \angle 90^\circ - \tan^{-1} \frac{\omega L_2}{r_s} - \tan^{-1} \frac{\omega L_2}{r_s} \left(\frac{1-k^2}{k^2} \right) \quad (4-41)$$

The resistance reflected into the primary terminals due to r_s is:

$$\begin{aligned} R_s &= \left(\frac{V_1}{V_2} \right)^2 r_s \\ &= k^2 \frac{L_1}{L_2} \left[1 + \frac{\omega^2 L_2^2}{r_s^2} \left(\frac{1-k^2}{k^2} \right)^2 \right] r_s \end{aligned} \quad (4-42)$$

For the simple case where k approaches closely to 1, Equations (4-41) and (4-42) become:

$$\begin{aligned} \frac{V_2}{V_1} &= -\sqrt{\frac{L_2}{L_1}} \angle 90^\circ - \tan^{-1} \frac{\omega L_2}{r_s} \\ &= -\frac{n_2}{n_1} \angle 90^\circ - \tan^{-1} \frac{\omega L_2}{r_s} \end{aligned} \quad (4-43)$$

and

$$\begin{aligned} R_s &= r_s \frac{L_1}{L_2} \\ &= r_s \cdot \left(\frac{n_1}{n_2} \right)^2 \end{aligned} \quad (4-44)$$

For the stipulated ratio of ωL_2 to r_s , the phase angle of the transformer then approaches closely to the ideal value of 180 degrees, the phase error being +18 degrees or less, and the impedance transforming ratio is simply related to the inductance ratio of the windings. However, these are idealized relationships, and even small deviations of k from a value of unity can have an appreciable effect on the transformer action, particularly insofar as the phase angle of the transformer is concerned. This can be illustrated by the calculations presented in Table 4-1. These calculations are for a ratio of $\omega L_2/r_s$ equal to 3 and show that both the phase and voltage ratio errors are reasonably small when k is 0.9 or larger, but are appreciable when k is 0.85 and large when k falls below 0.8. The voltage ratio error as k decreases is not of great significance since the correct transformation ratio could be obtained by suitably adjusting the turns ratio, but the large phase error for k less than 0.9 is undesirable if the transformer is used in the oscillator loop.

TABLE 4-1. TRANSFORMER PHASE ANGLE AND VOLTAGE RATIO AS A FUNCTION OF THE COUPLING FACTOR k .

$\frac{\omega L_2}{r_s} = 3, \quad \tan^{-1} \frac{\omega L_2}{r_s} = 72^\circ$			
k	$\tan^{-1} \frac{\omega L_2}{r_s} \left(\frac{1-k^2}{k^2} \right)$ (Degrees)	Transformer Phase Angle (Referenced to 180°)	Voltage Transformation Error (%)
0.9	35	-17	- 9
0.85	49	-31	-23
0.8	59	-41	-36
0.75	67	-49	-43
0.7	72	-54	-56

Normally, the amplifier circuit, in addition to its nominal zero or 180-degree phase shift, will have a phase lag between input and output due to the inherent time delay of signals passing between input and output. At low frequencies this will be negligible, but at high frequencies the phase lag may be appreciable, particularly in transistor amplifiers. If anything, therefore, it is desirable that the impedance transforming network should contribute a phase lead rather than an appreciable lag, as is the case for an inductive transformer with a coupling coefficient of less than 0.9.

It is therefore necessary to minimize the transformer phase lag by making the coupling as close as possible. At frequencies below, say, 10 MC, coupling coefficients of 0.9 or larger can be achieved relatively easily using high permeability toroidal cores ($\mu_0 = 400$ or larger), if intimate contact between windings occurs. This generally entails minimizing the spread of the windings around the core and winding one of the windings tightly over the other. At the low radio frequencies and audio frequencies, even these precautions are frequently unnecessary when high permeability toroidal or pot cores are used. The flux external to the core is then often negligible, permitting the windings to be distributed around the core.

At frequencies above, say, 10 MC, however, the losses occurring in the high permeability cores may often be prohibitively large, making their use unfeasible. An example of this would be a transformer connected to the output of the amplifier for the purpose of impedance level matching to a crystal unit, where the loading of the amplifier due to the transformer losses may be as large as that due to the oscillator external load.

The cores suitable for use above 10 or 20 MC have a lower permeability, increasing the likelihood of flux leakage and the difficulty of approaching a coupling coefficient of 0.9. If the terminating resistance levels are relatively low, it is sometimes possible to achieve this degree of coupling by placing the windings on the core in the form of a group of wires tightly twisted together; the primary and secondary windings then being made up of several of these individual windings connected in series or, in some cases, in parallel. This is the technique used in broadband transformer design which is essentially an extension of the bifilar method of obtaining close coupling.

It should be emphasized that the values given in Table 4-1 are for a ratio of ωL_2 to r_s of 3. If this ratio is made larger, the phase and voltage transformation errors will increase for a given coefficient of coupling. Therefore, the optimum design condition is ωL_2 equal to $3 r_s$.

The second case considered occurs when the load applied to the transformer secondary is large compared to the secondary winding reactance. When $r_s \geq 3 \omega L_2$, Equation (4-37) simplifies to:

$$\begin{aligned}
 V_1 &\approx I_1 \left[\frac{\omega^2 M^2}{r_s} + j \omega L_1 \left(1 - \frac{k^2 \omega^2 L_2^2}{r_s^2} \right) \right] \\
 &\approx I_1 \omega L_1 \left(\frac{k^2 \omega L_2}{r_s} + j 1 \right) \\
 &\approx I_1 \omega L_1 \angle \tan^{-1} \frac{r_s}{k^2 \omega L_2}
 \end{aligned} \tag{4-45}$$

The secondary output voltage is:

$$V_2 \approx -I_1 \omega M \angle 90^\circ - \tan^{-1} \frac{\omega L_2}{r_s} \quad (4-46)$$

Then

$$\frac{V_2}{V_1} \approx -k \sqrt{\frac{L_2}{L_1}} \angle 90^\circ - \tan^{-1} \frac{\omega L_2}{r_s} - \tan^{-1} \frac{r_s}{k^2 \omega L_2} \quad (4-47)$$

$\tan^{-1} \frac{\omega L_2}{r_s}$ will always be less than or equal to 18 degrees for the given condition, while $\tan^{-1} \frac{r_s}{k^2 \omega L_2}$ will be between 72 and 90 degrees. The maximum input-output voltage deviation from 180 degrees is therefore -18° which occurs when $r_s = 3 \omega L_2$ and $k \ll 1$, decreasing as r_s increases relative to ωL_2 . The transformer phase angle is therefore always close to ideal. The resistance reflected across the primary winding terminals due to r_s is:

$$\begin{aligned} R_s &= \left(\frac{V_1}{V_2} \right)^2 r_s \\ &= -\frac{1}{k^2} \left(\frac{n_1}{n_2} \right)^2 r_s \end{aligned} \quad (4-48)$$

The parallel reactive component across the input terminals is approximately equal to ωL_1 .

4-6. THE AUTOTRANSFORMER

The network to be analyzed is shown in Figure 4-7 where:

L_1 is the inductance between the input terminal and the tap point.

L_2 is the inductance common to both input and output circuits.

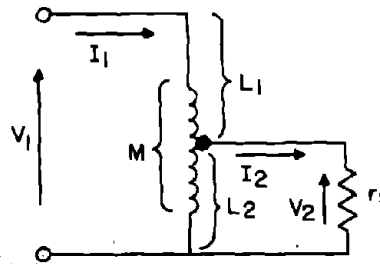
M is the mutual inductance of L_1 and L_2 .

k is the coupling coefficient of the windings.

r_s is the load resistance.

M , k , L_1 , and L_2 are related by the expression:

$$M = k \sqrt{L_1 \cdot L_2} \quad (4-49)$$



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Figure 4-7. Autotransformer Relationships

The relationship between L_1 and L_2 and their respective number of turns, n_1 and n_2 , is:

$$\frac{L_1}{L_2} = \left(\frac{n_1}{n_2} \right)^2$$

The resistance of the windings is considered to be small compared to the driving source resistance and r_s .

The equations for the circuit of Figure 4-7 are:

$$V_1 = I_1 j\omega [L_1 + L_2 + 2M] - I_2 j\omega [L_2 + M] \quad (4-50)$$

$$I_2 [r_s + j\omega L_2] = I_1 j\omega [L_2 + M] \quad (4-51)$$

$$V_2 = I_2 r_s \quad (4-52)$$

Therefore:

$$I_1 = I_2 \left[\frac{r_s + j\omega L_2}{j\omega (L_2 + M)} \right] \quad (4-53)$$

$$V_1 = I_2 \left\{ (r_s + j\omega L_2) \left[\frac{L_1 + L_2 + 2M}{L_2 + M} \right] - j\omega (L_2 + M) \right\} \quad (4-54)$$

and:

$$\frac{V_1}{V_2} = \frac{r_s + j\omega L_2}{r_s} \left[\frac{L_1 + L_2 + 2M}{L_2 + M} \right] - \frac{j\omega}{r_s} [L_2 + M] \quad (4-55)$$

$$= \frac{L_1 + L_2 + 2M}{L_2 + M} \left[1 + \frac{j\omega L_2}{r_s} \left[1 - \frac{\left(1 + \frac{M}{L_2} \right) (L_2 + M)}{L_1 + L_2 + 2M} \right] \right] \quad (4-56)$$

Substituting for M in terms of L_1 , L_2 , and k and manipulating finally gives:

$$\frac{V_1}{V_2} = \left[1 + k\sqrt{\frac{L_1}{L_2}} + \frac{L_1}{L_2} \left(\frac{1-k^2}{1 + k\sqrt{\frac{L_1}{L_2}}} \right) \right] \times \left[1 + j \frac{\omega L_2}{r_s} \left(1 - \frac{k^2 + \frac{L_2}{L_1} + 2k\sqrt{\frac{L_2}{L_1}}}{1 + \frac{L_2}{L_1} + 2k\sqrt{\frac{L_2}{L_1}}} \right) \right] \quad (4-57)$$

Equation (4-57) may also be written as:

$$\frac{V_1}{V_2} = \left[1 + k\sqrt{\frac{L_1}{L_2}} \right] \left[1 + \frac{L_1}{L_2} \cdot \frac{1-k^2}{\left(1 + k\sqrt{\frac{L_1}{L_2}} \right)^2} \right] \times \left[1 + j \frac{\omega L_2}{r_s} \cdot \frac{L_1}{L_2} \left[\frac{1-k^2}{\left(1 + k\sqrt{\frac{L_1}{L_2}} \right)^2 + \frac{L_1}{L_2} (1-k^2)} \right] \right] \quad (4-58)$$

For the simple case where k approaches closely to 1, Equations (4-57) or (4-58) reduce to:

$$\frac{V_1'}{V_2} = 1 + \sqrt{\frac{L_1}{L_2}} \quad (4-59)$$

The accuracy of Equation (4-59) as an approximation for Equations (4-57) or (4-58) not only depends on how closely k approaches unity, but also on the relative values of L_1 and L_2 . This is illustrated in the plots of Figure 4-8, where a comparison is made of the actual voltage ratio magnitude $\left| \frac{V_2}{V_1} \right|$ to the idealized ratio $\frac{V_2'}{V_1}$ for various values of k and for $\omega L_2/r_s$ equal to 3. These plots show that for $\omega L_2/r_s$ equal to 3, Equation (4-59) can only be regarded as a suitable design equation when k is 0.9 or larger or, for lower values of k , when L_1/L_2 is less than 1.

The phase angle of V_2 relative to V_1 is also plotted in Figure 4-8. These curves show that the phase lag is undesirably large when k is less than 0.9, except when L_1/L_2 is less than 1. These curves are for $\omega L_2/r_s$ equal to 3; smaller values of this ratio will give a lower voltage ratio error and phase lag,

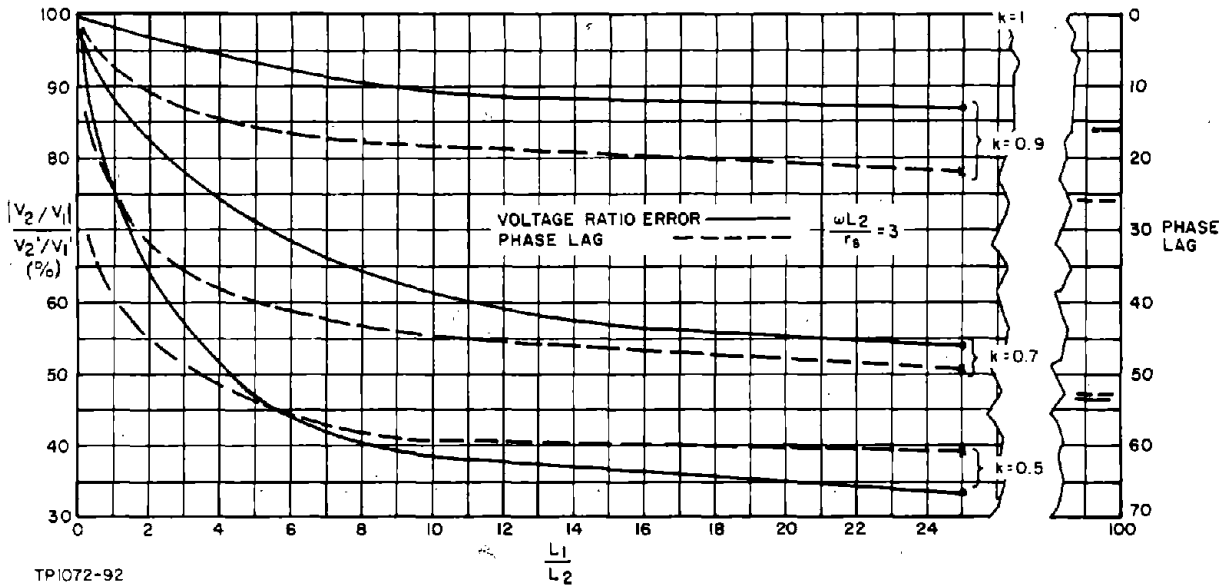


Figure 4-8. Autotransformer Voltage Ratio Error and Phase Angle Relative to the Ideal Case When $k = 1$

and a larger ratio will increase the voltage ratio error and the phase lag. When using the autotransformer as a feedback element, it is therefore good practice to minimize the ratio $\omega L_2/r_s$ as much as possible consistent with not presenting too low an inductive reactance to the preceding circuit.

The autotransformer input impedance is obtained from Equations (4-50) and (4-51) as:

$$Z = \frac{V_1}{I_1} = j\omega \left[L_1 + L_2 + 2M - \frac{(k^2 L_1 + L_2 + 2M)}{1 - j \frac{r_s}{\omega L_2}} \right] \quad (4-60)$$

For the extreme condition when

$$r_s \ll \omega L_2,$$

this reduces to:

$$Z = r_s \left(1 + k \sqrt{\frac{L_1}{L_2}} \right)^2 + j\omega L_1 (1 - k^2) \quad (4-61)$$

and for $r_s \gg \omega L_2$:

$$\begin{aligned} Z &\approx \frac{\omega L_2}{r_s} \cdot \omega (k^2 L_1 + L_2 + 2M) + j\omega (L_1 + L_2 + 2M) \\ &\approx j\omega (L_1 + L_2 + 2M) \end{aligned} \quad (4-62)$$

The parallel input resistive component due to r_s is:

$$R_s = \left(\frac{V_1}{V_2} \right)^2 r_s \quad (4-63)$$

For the case where k approaches closely to 1, this becomes:

$$R_s = \left(1 + \sqrt{\frac{L_1}{L_2}} \right)^2 r_s \quad (4-64)$$

A simplification of the voltage ratio expression is also obtained when $k \sqrt{\frac{L_1}{L_2}} \gg 1$.
Then:

$$\frac{V_1}{V_2} = \frac{1}{k^2} \sqrt{\frac{L_1}{L_2}} \left[1 + \frac{j\omega L_2}{r_s} (1 - k^2) \right] \quad (4-65)$$

The autotransformer does not appear to offer any advantages over the two-winding transformer, except possibly when the impedance transformation ratio required is small.

4-7. WIEN BRIDGE NETWORK

The Wien Bridge network has frequency selective properties that may be useful in low-frequency oscillators. The network is shown in Figure 4-9.

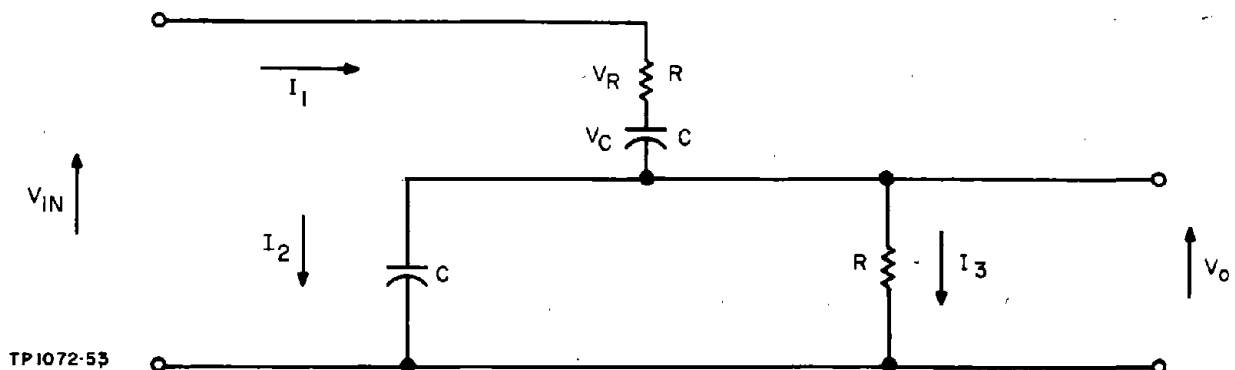


Figure 4-9. Wien Bridge Network Circuit

The equations for this circuit are:

$$V_{in} = I_1 \left[R + \frac{1}{j\omega C} + \frac{R}{1 + j\omega CR} \right] \quad (4-66)$$

$$V_o = I_1 \cdot \frac{R}{1 + j\omega CR} \quad (4-67)$$

$$\frac{V_o}{V_{in}} = \frac{R}{(1 + j\omega CR) \left(R + \frac{1}{j\omega C} + \frac{R}{1 + j\omega CR} \right)} \quad (4-68)$$

$$= \frac{1}{3 + j \left(\frac{\omega}{\omega'} - \frac{\omega'}{\omega} \right)} \quad (4-69)$$

where

$$\omega' = \frac{1}{CR}$$

At $\omega = \omega'$, the reactive component in the denominator is zero and:

$$\frac{V_o}{V_{in}} = \frac{1}{3} \quad (4-70)$$

At angular frequencies in the vicinity of ω' , the response is similar to that of a tuned circuit.

The vector relationships within the network at angular frequency ω' can be determined by noting that:

$$R = \frac{1}{j\omega' C} \quad (4-71)$$

and therefore:

$$|I_2| = |I_3| \quad (4-72)$$

Figure 4-10 shows the vector diagram for the network at $\omega = \omega'$.

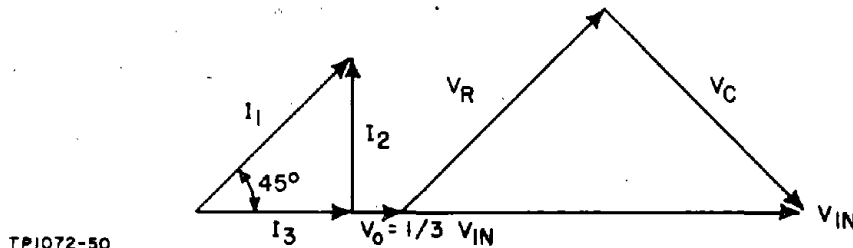


Figure 4-10. Wien Bridge Network Vector Diagram

The input impedance is:

$$Z_{in} = \frac{V_{in}}{I_1} = \frac{3}{2} \cdot R (1 - j) \quad (4-73)$$

Or transforming to parallel elements, the parallel resistance is:

$$R' = 3 R \quad (4-74)$$

and the parallel capacitive reactance is:

$$X'_C = 3 R \quad (4-75)$$

This analysis is for one particular case of this type of network. If the network is analyzed in its general form where R_1 and C_1 are the series elements and R_2 and C_2 are the parallel elements, the input and output voltages are in phase when:

$$\omega^2 = \frac{1}{C_1 C_2 R_1 R_2} \quad (4-76)$$

The relationship between $\frac{V_o}{V_{in}}$ at zero phase angle is:

$$\frac{V_o}{V_{in}} = \frac{R_2}{R_1 + R_2 \left(1 + \frac{C_2}{C_1} \right)} \quad (4-77)$$

SECTION 5 GENERAL OSCILLATOR TOPICS

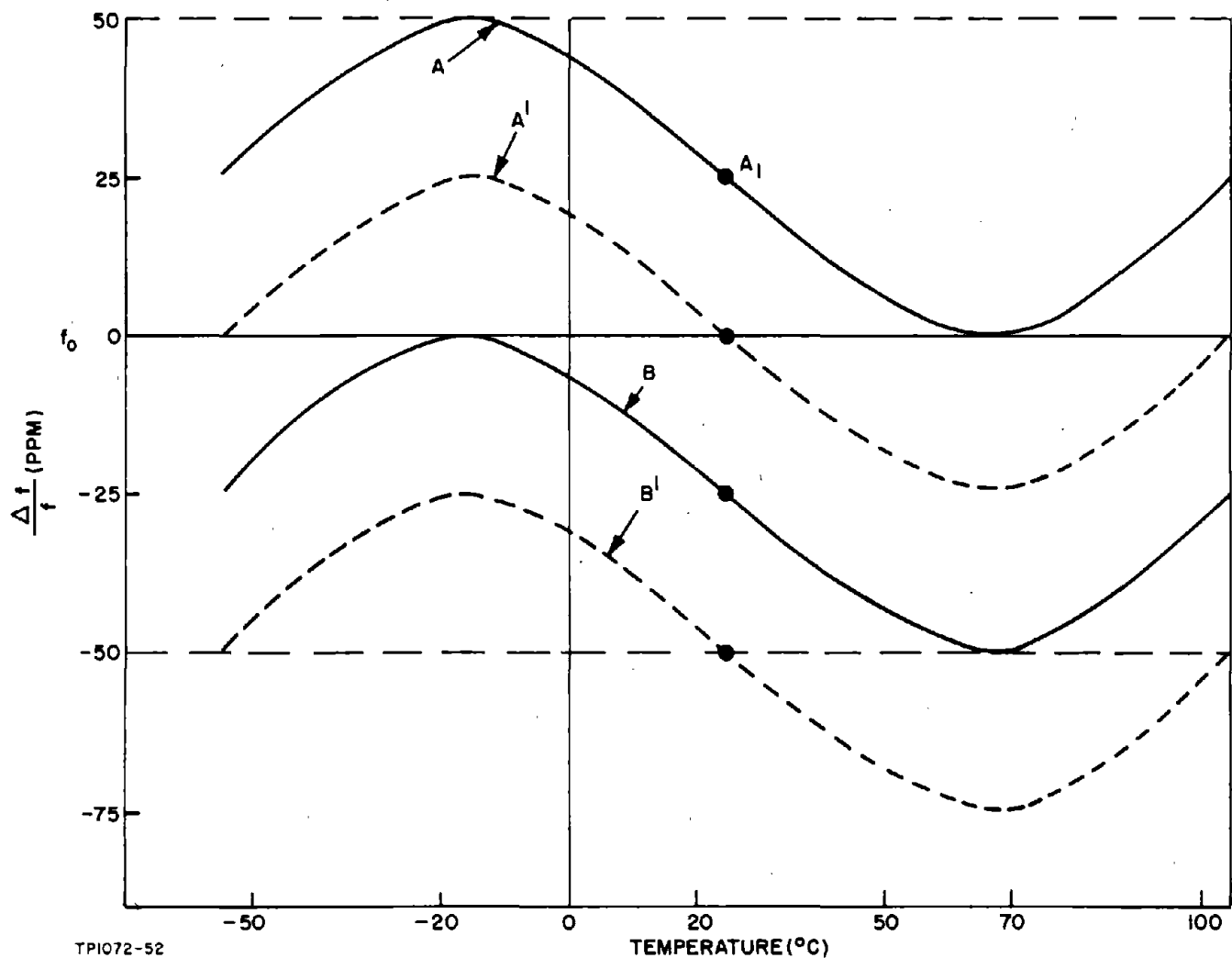
5-1. OSCILLATOR FREQUENCY TOLERANCE

The oscillator overall frequency tolerance depends on the conditions of usage. If the service conditions are such that the oscillator can be readjusted to frequency periodically and whenever a tube, transistor, crystal unit or other oscillator component is replaced, the oscillator overall frequency tolerance can generally be made less than that of the crystal unit, since the crystal unit fabrication tolerance can then be cancelled. If, as is very often the case, it will be impractical or undesirable to readjust the oscillator to nominal frequency after the initial adjustment, the oscillator overall frequency tolerance will inevitably be wider than that of the crystal unit alone, particularly if many oscillators are to be used. For this condition of operation it is entirely possible that crystal units exhibiting the maximum permitted frequency deviation from nominal will be used in some of the oscillators, and circuit variations with temperature, supply power, or load variations, etc. will then widen the oscillator tolerance beyond that of the crystal unit.

This latter condition of service is the one most frequently encountered; and in order to obtain the minimum oscillator overall frequency tolerance, certain conditions must be met in the design. One of the major causes of an excessive overall frequency tolerance and one that can easily be avoided concerns the initial adjustment of the oscillator. It is frequently found that the oscillator is mistuned or adjusted to give an output frequency equal to the nominal design frequency. If the particular crystal unit employed during this initial adjustment has a frequency characteristic which is off-centered within its overall frequency tolerance, it is possible that the oscillator tolerance will be appreciably widened if another crystal unit is substituted at some future time. This can be illustrated by an extreme example using Figure 5-1.

Figure 5-1 shows the frequency-versus-temperature characteristics of two crystal units A and B of the same type and nominal frequency. Each one just meets the overall frequency tolerance of ± 50 PPM due to the offset caused by the fabrication tolerance of the crystal units. These characteristics and the frequency tolerance are typical of the AT cut crystal unit commonly used at all frequencies above 800 KC.

If crystal unit A was used for the initial oscillator adjustment and the circuit tuned to oscillate at the crystal unit nominal frequency f_0 at room temperature, the oscillator frequency variation with temperature will then be as shown by curve A¹, assuming no variation due to the other oscillator components.



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Figure 5-1. Effect of Pulling Oscillator to Crystal Nominal Frequency

If crystal unit A is now replaced by unit B without readjusting the circuit, the frequency offset introduced initially will now cause the oscillator frequency to follow curve B¹ over the temperature range, again assuming no variation due to the effects of temperature on other oscillator components. The oscillator tolerance is now increased by 50 percent relative to that of the crystal unit. This may be further increased by the effect of temperature and other variables on the other oscillator circuit components.

This is an extreme example and, although possible, it is not possible that the effect will be so severe. Nevertheless, an appreciable unnecessary increase in oscillator overall frequency tolerance is likely to occur when this method of initially tuning the oscillator is used. The correct method is to

initially adjust the oscillator to the actual crystal unit resonance frequency. There will then be no frequency offset, and the sole cause of the increase in oscillator tolerance relative to that of the crystal will be component variation in the remainder of the oscillator circuit.

It is not always desirable to measure the frequency of each crystal unit, and the necessity for this can be obviated if one crystal unit of known characteristics is used as a standard for initially adjusting all oscillators. The frequency offset or miscorrelation, when the crystal units intended for use with the oscillators are inserted in circuit, will then be less than 5 PPM and typically less than 2 PPM. It is good practice to determine the extent of this effect during the oscillator design evaluation stage by measuring the frequency miscorrelation for several known crystal units, preferably having a wide range of equivalent resistance.

The effect could be much worse in low frequency oscillators because of the parabolic temperature characteristic of the crystal units employed below 500 KC. Similar reasoning to the above indicates that tuning the oscillator to nominal frequency could lead to an increase of 100 percent in the oscillator tolerance over that of the crystal unit if a subsequent crystal unit change was made without a tuning readjustment.

Other effects that will cause the oscillator frequency to deviate from that of the crystal unit are:

- (a) Changes in loop gain will cause variations in crystal unit dissipation. This may cause frequency variations of from 0.5 to 5 PPM per milliwatt change in dissipation, depending on crystal unit type.

One of the major causes of loop gain change is the wide range of crystal unit equivalent resistance. Loop gain differences of several times can be expected between several oscillators of the same type because of this variation between crystal units. Consequently, oscillator and crystal unit frequency miscorrelation of several parts per million can be expected if several crystal units are interchanged in an oscillator circuit.

- (b) Changes in loop phase angle due to component changes other than the crystal will require a complementary phase change by the crystal unit and hence a change in oscillator frequency. In a series resonance oscillator the most likely causes of circuit phase changes will be the amplifier decoupling networks and the amplifier tank circuit when one is used. Decoupling network time constants should always be large compared to the design frequency period to minimize the effect of component change with temperature, etc. Amplifier tank circuits should, where possible, be

operated under conditions of low loaded Q . This will tend to make the phase angle of the loaded tuned circuit less sensitive to temperature, thereby reducing the amplifier phase angle variation that will occur over the operating temperature range. When the amplifier tank circuit loaded Q is low, the oscillator output is likely to have an appreciable harmonic content. This may conflict with oscillator output frequency purity requirements and a compromise will then be required or, alternatively, the use of further filtering. This should not apply in the majority of applications where the oscillator normally feeds a non-linear load such as a mixer, class B amplifier or harmonic generator. The non-linear operation of these circuits will automatically generate harmonic components, and the oscillator output components will be of little consequence.

It is also desirable in those oscillators using a tuned amplifier load that the tank circuit should tune to resonance at the crystal frequency. If this is not the case the amplifier will be operating on the slope of the resonance curve and, in addition to the undesired resultant phase angle, there will be a possibility of loop gain variation due to variations of the tuning capacitor and inductor with temperature. This is also desirable from the viewpoint of field maintenance. When a crystal unit, tube, or transistor is substituted, there will inevitably be a change in the oscillator tuning due to the difference in parasitic reactance, gain or resistance of the component changed.

In circuits where the amplifier is tuned to resonance, it is found that good correlation between crystal unit and oscillators can be maintained simply by tuning to maximum oscillator output voltage; an adjustment process requiring only a VTVM. All the design examples presented subsequently that employ an amplifier tank circuit were adjusted in this manner.

- (c) In an anti-resonant oscillator, the total load capacitance seen by the crystal unit can also contribute appreciably to the oscillator frequency instability. In the 0.8 to 20 MC range, for example, a change of 1 PF in the nominal loading capacitance value of 32 PF of a CR-18A/U crystal unit can cause a change in oscillator frequency of from 3 to 10 PPM. In a well designed oscillator of this type, a capacitor network usually contributes the greater part of the crystal loading capacitance, and that contributed by the amplifier circuit is made as small as possible in order to minimize the effect of its variation. To further reduce the oscillator frequency variation, it is desirable that the capacitor network should be constructed of low temperature coefficient capacitors.

- (d) Power supply and oscillator external load variations will also cause a change of oscillator frequency. The effect of these variations on the oscillator frequency is usually small, and their major effect is on the oscillator output voltage and power. The oscillator output voltage can be expected to change in direct proportion to the change in supply voltage and external load.

5-2. Oscillator Circuit Layout and Component Frequency Dependent Behavior

Few precautions are required when designing an oscillator at frequencies below a few megacycles. The oscillator circuit layout is not very critical, and no particular attention need be paid to the positioning of components. Capacitors and resistors will behave as expected, and measuring equipment input impedance is usually sufficiently high (or can easily be made so) so that circuit measurements can be made without influencing the oscillator performance.

At frequencies above 20 MC, the characteristics of the various components of an oscillator begin to be frequency-dependent due to the presence of parasitic reactance in its various forms. Circuit layout is also more critical for the same reasons and may be the determining factor in the level of performance that can be attained. Further, measurements become more difficult to make with any assurance of a reasonable accuracy. These effects are relatively mild at the lower frequencies and become worse as the frequency increases.

The prerequisite for design is to know the characteristics of the test equipment that will be used and to appreciate its influence on the circuit under test. It is not always sufficient to rely on manufacturers' specifications, since aging and other factors may degrade performance considerably. As an example, one vacuum-tube voltmeter used during early design evaluations had a parallel input resistance of a few hundred ohms in addition to the specified capacitance of 3 PF at 200 MC, making high impedance measurements meaningless. Another vacuum-tube voltmeter had a parallel input resistance of 5 K at 150 MC until the detector diode was changed, after which the parallel input resistance increased to over 25 K. Effects of this nature considerably influence the interpretation of measurements and should be constantly kept in mind. Similarly, circuit components are likely to differ considerably from their nominal values. Mica capacitors of nominal value exceeding 10 PF cannot be relied on to have an actual capacitance approaching the nominal value at the higher frequencies because of lead inductance. This effect can be important, particularly in impedance transforming networks. Carbon resistors also vary considerably from their nominal values, as shown in Figure 5-2. The deviation is particularly large for resistor values greater than 2 K and less than 40 ohms. These characteristics are those of a widely used make of 1/2 watt resistor. The same make of 1/4 watt resistor exhibits essentially similar frequency characteristics. In many cases this effect will be of little consequence; for example, in decoupling networks, etc.

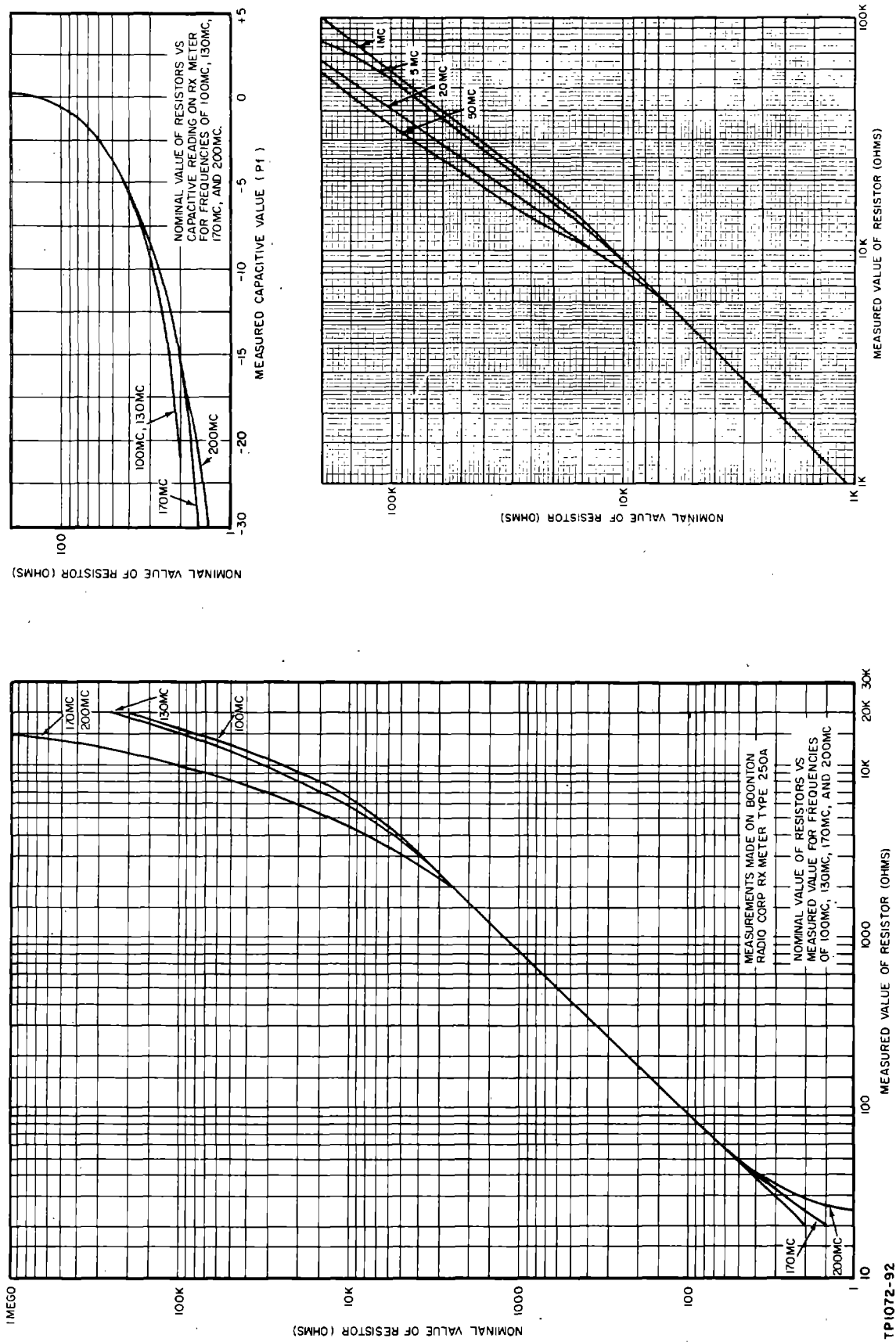


Figure 5-2. Variation of Resistance and Reactance With Frequency of 1/2 Watt Resistors

In other instances, such as using a resistor to load the oscillator for test purposes, it will be essential to know the actual value of resistance with reasonable accuracy.

Circuit wiring will also influence the performance of these elements. It is of little use to employ a component with a desired characteristic if the component will be wired into the circuit with long lead lengths. One inch of 20-gauge wire has a self-inductance of approximately 0.02 UH, corresponding to a reactance of 25 ohms at 200 MC. When working at low impedance levels, this inductance can have appreciable effect on circuit performance. Long lead lengths also increase mutual inductive coupling (the effects of which are more difficult to interpret) and stray capacitive coupling (which will have a maximum effect at high impedance points of the circuit).

When designing at high frequencies, because of the possible wide deviations from nominal of the components that will be used in the oscillator, it is advisable to measure the component values at the particular operating frequency to insure that design conditions are being fulfilled. In fact, the experiences of this program suggest that impedance measuring equipment is essential to the design effort at the high frequencies. Throughout that part of the program dealing with high-frequency oscillators, an RX meter was in constant use and proved invaluable in aiding the design effort.

The circuit layout problems posed during initial experimental design evaluation are somewhat different from those in a final design. It will be necessary to take measurements and change components in the circuit to evaluate the performance, while this will not be necessary in the final design. A more open construction is therefore necessary initially, to allow access for voltage measuring probes and to facilitate the changing of components. Figure 5-3 shows photographs of the layouts used for all the high-frequency oscillator test circuits evaluated during this program. In these layouts the output and input circuits were separated by the shield extending across the chassis. This shield is not essential; it was included during the early evaluations as an additional safeguard and, since the layout met the measurement needs, it was used throughout the high-frequency design program.

5-3. INITIAL DESIGN INFORMATION

Prior to the design of an oscillator, a specification is written fixing the oscillator performance requirements. These requirements are normally specified in the following form:

- (a) The frequency of oscillation, the frequency tolerance, and the frequency stability required of the oscillator when subjected to a certain range of environmental stress, to specified variations

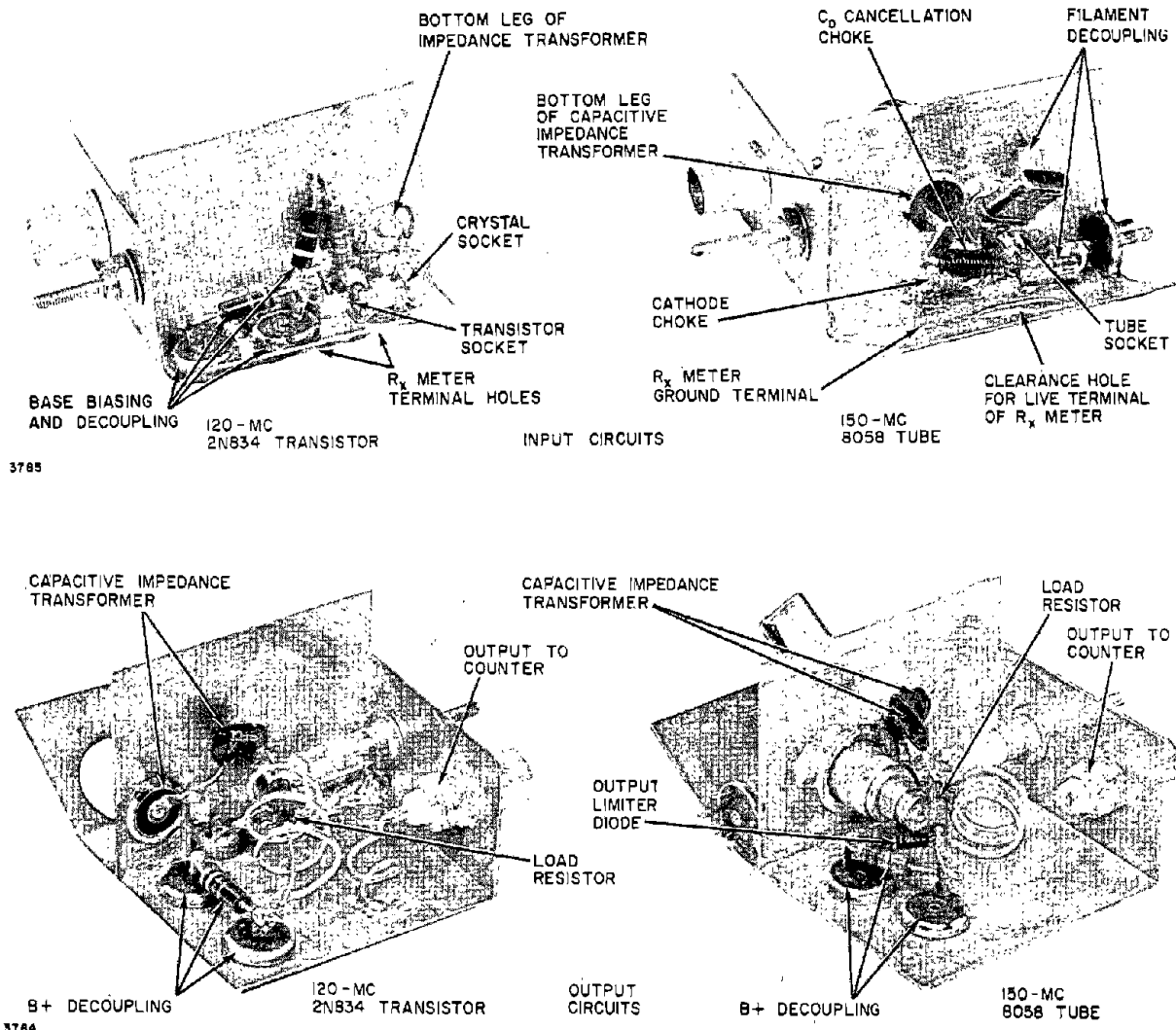


Figure 5-3. High-Frequency Oscillators, Input and Output Circuits

in oscillator loading, and to permissible power source variations. The minimum time period between readjustment of oscillator frequency to compensate for frequency drifts due to aging and the maximum harmonic output may also be specified.

- (b) The power output and its variation, when subjected to a certain range of environmental stress, specified variations in oscillator loading, and permissible power source variations.
- (c) The load impedance into which the oscillator will work. In some instances the load will be a mixer circuit or other non-

linear input impedance circuit, and, in this case, the load impedance is likely to be only vaguely defined.

- (d) The permissible input power, the DC input voltage level, and the expected range of variation.
- (e) The physical size of the oscillator.

In addition, the type of active device (that is, tube or transistor) and the maximum cost may be specified.

The task facing the designer is to meet all of the design requirements and, when a quantity of oscillators are to be built, to ensure that compliance is maintained when the likely range of variables such as amplifier gain, component tolerances, and crystal equivalent resistance are encountered. The following guidelines may be useful in making a preliminary assessment of design feasibility.

The causes of oscillator frequency instability have already been detailed in Paragraph 5-1, together with the precautions required to minimize this effect. As a general rule when many oscillators are to be constructed, the oscillator overall frequency tolerance is likely to be ± 10 to ± 15 PPM wider than that of the crystal unit, provided reasonable precautions are made in the selection of components. If oscillator adjustments are permissible when any maintenance changes are necessary, this tolerance will decrease to possible 50 percent of the crystal unit tolerance.

The oscillator power output is a function of the power supply voltage, the loop gain, and the oscillator external load. Because of the possible large variation in loop gain due to the wide range of crystal equivalent resistance likely to be encountered, the power output differences from unit to unit may exceed a ratio of 4:1. The change in power output caused by supply voltage variations will be approximately equal to the square of the supply voltage change.

Ignoring heater power requirements, vacuum tube oscillators are generally inefficient in converting supply power to oscillator output power. Crystal unit power dissipation usually limits the plate voltage swing to a fraction of the DC plate voltage, and plate current levels are frequently dictated by consideration of maximizing the amplifier gain. This is particularly the case at design frequencies above 20 MC where high transconductance, and, hence, high plate current tubes are practically essential. Transistor oscillators can be designed to give power conversion efficiencies of 30 to 40 percent, allowing for adequate biasing to meet wide temperature variations.

5-4. OSCILLATOR DESIGN PROCESS

Based on the design specification, a process of selection is necessary to arrive at a final design. This involves the selection of:

- (a) The crystal operating condition. At frequencies up to 20 to 25 MC, there is a choice between operation at resonance or anti-resonance; at higher frequencies, only crystals operating at resonance are available. Below 25 MC, anti-resonance crystal units are available and increase the number of oscillator circuits from which a selection can be made. In vacuum tube oscillators this increase is applicable throughout the range of 1 KC to 25 MC. In transistor oscillators, however, due to large incompatibilities between amplifier and crystal characteristics, anti-resonance oscillator circuits are essentially a variant of the series resonance circuits below 90 KC.
- (b) A particular type of crystal from those available at the desired frequency of operation.
- (c) The oscillator configuration.
- (d) The tube or transistor characteristics.
- (e) A particular tube or transistor type.
- (f) The type of impedance transforming network to be used.

There are many intangibles involved in arriving at a final design, and there is no single method of approach to a particular oscillator design that can be justifiably claimed as the optimum one. In each of the major design steps listed above there is a wide latitude of choice, particularly in steps (c) through (f). The following handbook sections consider in detail the individual characteristics of the various oscillator components in relationship to one another in a particular frequency range. A detailed design procedure is then arrived at, and design examples and their experimental evaluation data presented. This experimental data can then be used as a guide to estimate the performance capability of the various oscillator types.

SECTION 6

VACUUM TUBE SERIES RESONANCE OSCILLATOR DESIGN

6-1. GENERAL

Vacuum tube series type oscillators can be used throughout the entire frequency range from below 1 KC to 200 MC. Many types of circuits have been developed for use with this type of crystal unit, no one of which is usable throughout the entire range due to the wide variation of crystal unit characteristics encountered in the frequency range.

One circuit that is usable over a wide frequency range, when a suitable tube is selected, employs a grounded grid amplifier in the configuration shown in Figure 6-1 (a). This circuit can be used in the frequency range of 90 KC to 200 MC, although in the range of approximately 2 to 60 MC an additional impedance transformer is required between the crystal unit and the tube cathode if the design is to be optimized.

Below 90 KC, the oscillator configuration of Figure 6-1 (a) is no longer entirely suitable and a more useful configuration consists of a grounded cathode amplifier with a phase inverting feedback network, as shown in Figure 6-1 (b).

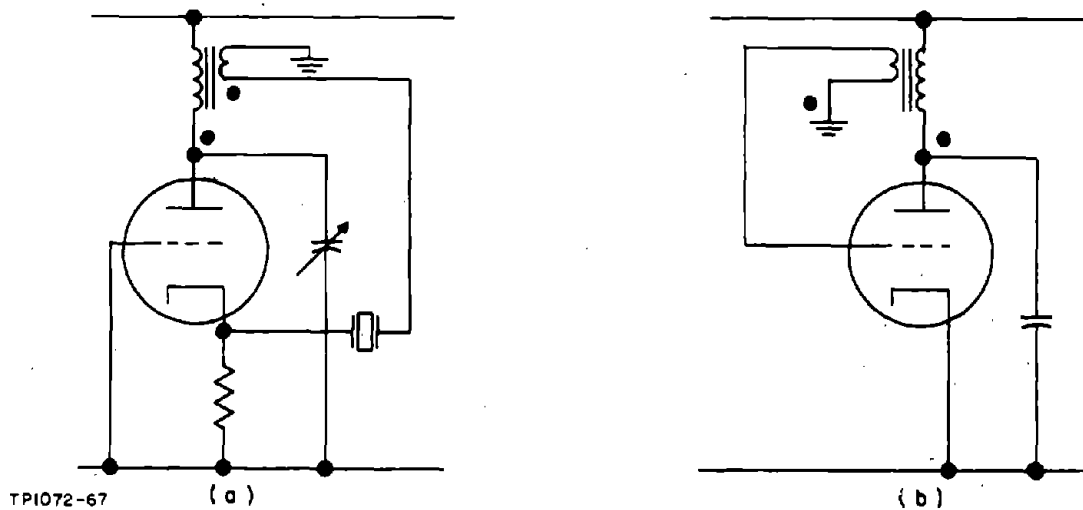


Figure 6-1. Series Resonance Oscillator Configurations

This configuration can be used throughout the range of 1 KC to 90 KC, or even 500 KC, although at frequencies below 10 or 20 KC the size or weight of the inductor required to give the impedance transforming and phase inverting action may be unduly large. It may then be preferable to employ another amplifier stage instead of the impedance transformer.

There are, therefore, three more or less distinct frequency ranges where the design technique changes sufficiently to necessitate a different emphasis, and the following discussion is sub-divided accordingly into three parts dealing with design in the 90 to 200 MC, 10 to 100 KC, and 1 KC to 10 KC ranges.

The discussion is given entirely in terms of the triode amplifier because of the simplicity of the resulting amplifier circuit. There is no reason, however, why pentode or tetrode amplifier circuits cannot be used.

6-2. SERIES RESONANCE CRYSTAL UNIT CHARACTERISTICS, 90 TO 200 MC RANGE

Table 6-1 gives the major characteristics of the military standard series resonance crystal units in the frequency range of 200 KC to 125 MC. More detailed specifications are given in MIL-C-3098, Supplement 1. There are no preferred series resonance crystal units in the 90 to 200 KC range, but the CR-37A/U anti-resonance type can be used as the equivalent of a series crystal unit if a 20 PF loading capacitor is connected in series with the crystal unit. This type and the CR-42A/U for use in controlled temperature applications, for which the appropriate series loading capacitance is 32 PF, are included in Table 6-1 with this proviso. Similarly, there are no military crystal units for the frequency range of 125 to 200 MC, but crystal units can be purchased in this range that meet the specifications of the CR-54A/U, CR-56A/U, CR-80/U, CR-82/U or CR-85/U types, except that the maximum resonance resistance may be increased to 80 or 100 ohms.

The multiplicity of crystal unit types in certain frequency ranges is due partly to the various types of crystal holders employed and also to there being usually two and sometimes three different frequency tolerances. In the majority of cases the actual quartz element is the same for all the various types at a given frequency, the differences being either the crystal holder type or the degree of precision employed in manufacturing the quartz element.

The maximum resonance resistance of crystal units varies appreciably over the frequency range of 90 KC to 200 MC, particularly at frequencies below 20 MC. This variation is plotted in Figure 6-2 illustrating the rapid change of this crystal unit characteristic below 20 MC. Only the maximum value of resonance resistance is specified, and the actual resonance resistance of individual crystal units varies widely. The actual range of values likely to be

TABLE 6-1. MILITARY STANDARD SERIES RESONANCE CRYSTAL UNITS, 90 KC TO 200 MC

Frequency Range (MC)	Operating Temperature Range (Centigrade)	Frequency Tolerance (\pm Percent)	Rated Drive (MW)	Maximum Resonance Resistance (ohms)	Crystal Unit Type	Holder Type
WIDE TEMPERATURE RANGE CRYSTAL UNITS						
*0.08 to 0.2	-40 to +70	0.01	2	2000 to 2500	CR-16B/U	HC-21/U
**0.09 to 0.25	-40 to +70	0.02	2	5000 to 5500	CR-37A/U	HC-13/U
0.2 to 0.5	-40 to +85	0.01	2	2500 to 7500	CR-25A/U	HC-6/U
0.455	-40 to +70	0.02	2	3300	CR-45/U	HC-6/U
0.8 to 20	-55 to +105	0.005	10 and 5	520 to 15	CR-19A/U	HC-6/U
0.8 to 20	-55 to +105	0.0025	10 and 5	520 to 15	CR-85/U	HC-6/U
5 to 20	-55 to +105	0.005	5	50 to 20	CR-60A/U	HC-18/U
*10 to 61	-55 to +105	0.005	20	40	CR-51A/U	HC-6/U
10 to 61	-55 to +105	0.005	2 and 4	40	CR-52A/U	HC-6/U
*15 to 50	-55 to +105	0.005	2	50 and 75	CR-24/U	HC-18/U
17 to 61	-55 to +105	0.005	2	40	CR-55/U	HC-18/U
17 to 61	-55 to +105	0.0025	2	40	CR-67/U	HC-18/U
17 to 61	-55 to +105	0.005	2	40	CR-72/U	HC-18/U
17 to 61	-55 to +105	0.0025	2	40	CR-76/U	HC-18/U
17 to 62	-55 to +105	0.002	2	40	CR-77/U	HC-25/U
17 to 61	-55 to +105	0.005	2	40	CR-81/U	HC-25/U
35 to 50					CR-73/U	
*50 to 87	-55 to +105	0.005	20	60	CR-53A/U	HC-6/U
50 to 125	-55 to +105	0.005	2	50 and 60	CR-54A/U	HC-6/U
50 to 125	-55 to +105	0.005	2	50 and 60	CR-56A/U	HC-18/U
50 to 125	-55 to +105	0.002	2	50 and 60	CR-80/U	HC-18/U
50 to 125	-55 to +105	0.005	2	50 and 60	CR-82/U	HC-25/U
50 to 125	-55 to +105	0.002	2	50 and 60	CR-83/U	HC-25/U
125 to 200	-55 to +105	0.005	2	80 to 100	Similar to CR-54A/U, CR-56A/U, CR-80/U, CR-82/U or CR-83/U	
TEMPERATURE CONTROLLED CRYSTAL UNITS						
*0.08 to 0.2	70 to 80	0.002	2	2000 to 2500	CR-30A/U	HC-21/U
**0.09 to 0.25	70 to 80	0.003	2	4500 to 5000	CR-42A/U	HC-13/U
0.2 to 0.5	70 to 80	0.002	2	2500 to 7500	CR-26A/U	HC-6/U
0.8 to 20	70 to 80	0.002	5 and 2.5	520 to 15	CR-28A/U	HC-6/U
0.8 to 20	80 to 90	0.002	5 and 2.5	520 to 15	CR-35A/U	HC-6/U
10 to 61	70 to 80	0.001	2 and 1	60 and 40	CR-65/U	HC-6/U
10 to 75	70 to 80	0.002	2 and 1	60 and 40	CR-32A/U	HC-6/U
17 to 61	80 to 90	0.002	2 and 1	40	CR-61/U	HC-18/U
17 to 61	80 to 90	0.002	2 and 1	40	CR-84/U	HC-25/U
50 to 125	80 to 90	0.002	1	50 and 60	CR-59A/U	HC-18/U
50 to 125	70 to 80	0.001	1	40	CR-75/U	HC-6/U
* Special Application ** Anti-resonance Units (see text)						

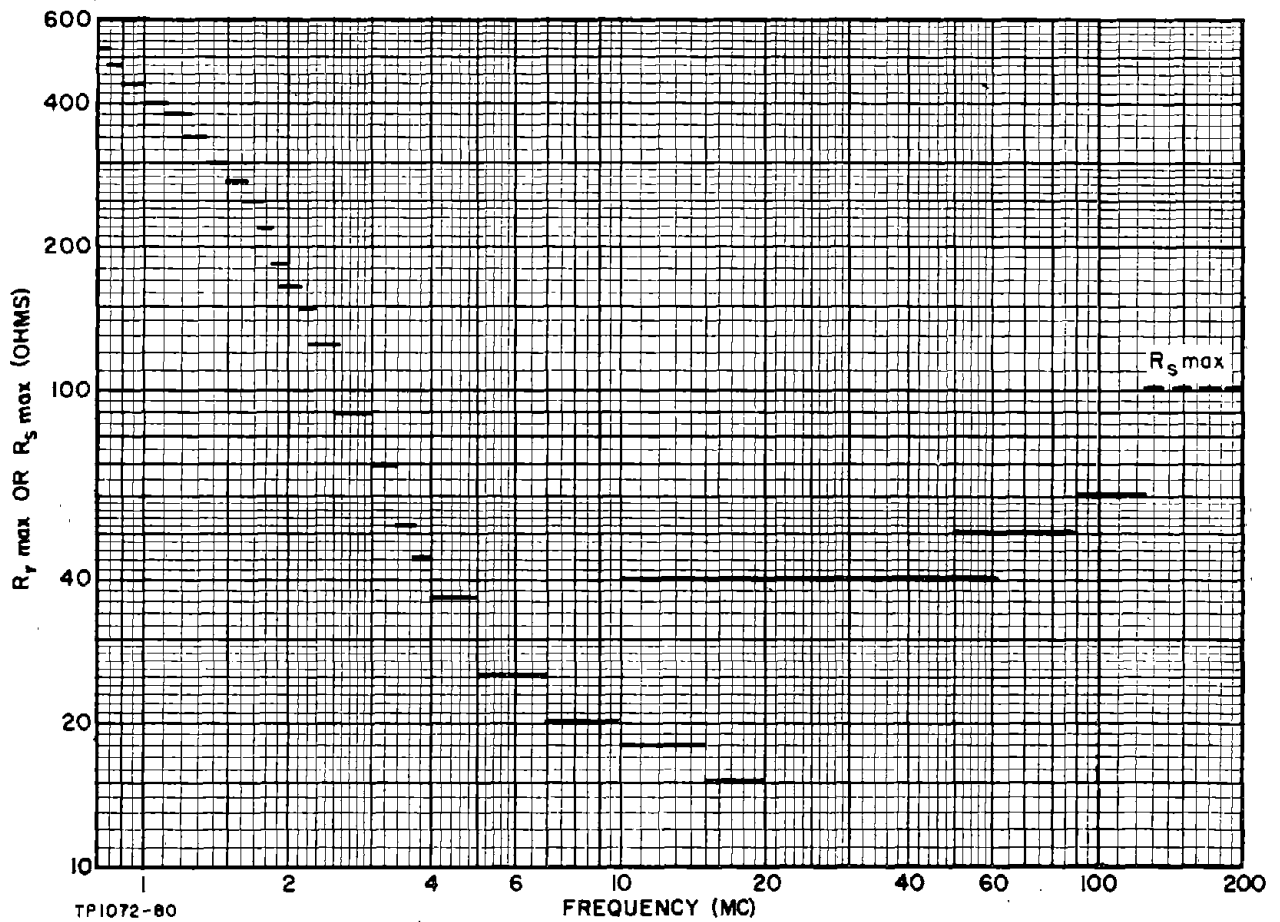
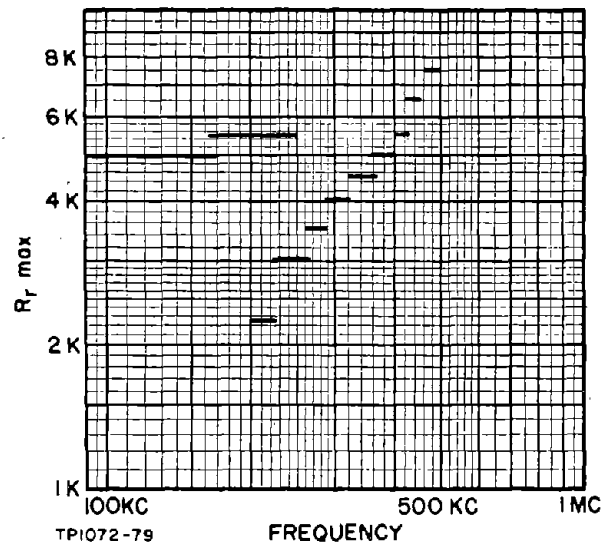


Figure 6-2. Variation of Crystal Unit Resonance or Series Resonance Resistance With Frequency

encountered will probably be from $R_r \text{ max}$ to $1/9 R_r \text{ max}$ at frequencies below 20 MC, $R_r \text{ max}$ to $1/4 R_r \text{ max}$ from 20 to 60 MC, and $R_r \text{ max}$ to $1/3 R_r \text{ max}$ above 60 MC.

For almost all of these crystal unit types the shunt capacitance C_o is approximately 7 PF and is generally of little importance insofar as oscillator design is concerned at frequencies below 100 MC. But above 100 MC C_o can degrade the crystal unit phase shifting capability, since the ratio of X_{C_o} to R_1 is then small. The reactance of a 7 PF capacitance varies from 230 ohms at 100 MC to 114 ohms at 200 MC, while the crystal series arm resistance may, in the worst case, be 60 ohms at 100 MC and 100 ohms at 200 MC.

The ratio X_{C_o} to R_1 , therefore, lies in the range of 1 to 5. The analysis of Paragraph 1-4 shows that the crystal unit phase shifting capability is severely degraded when this ratio is less than 3. At frequencies above 100 MC, therefore, this condition is either being approached or exceeded, and to prevent excessive degradation of the crystal unit phase shifting capability it is necessary to neutralize C_o . This is achieved by connecting an inductor, which resonates with C_o at the crystal unit frequency, in parallel with the crystal unit. The value of C_o at the operating frequency can vary appreciably from the value measured at low frequencies, and to obtain maximum effect C_o should be determined at a frequency close to the operating frequency, but sufficiently lower that the motional arm of the crystal unit has a negligible effect on the measurement. A frequency 5 to 10 percent below the operating frequency is usually satisfactory.

Complete cancellation of C_o is not essential since the object is simply to increase the parallel capacitive reactance to a value such that $\frac{X_{C_o}}{R_1}$ for a worst-case crystal will be larger than, say, 5. Therefore, an inductance which resonates with the typical value of C_o at the operating frequency will suffice for all crystal units of the particular type.

The Q of the inductor should be sufficiently large that its effective parallel resistance is at least 10 times the crystal unit series resonance resistance to avoid a degradation of the crystal unit phase shifting capability due to this cause. This is not a demanding requirement considering the low value of R_1 at these frequencies, and frequently the inductor is constructed in the form of a closely spaced single-layer coil wound on a 1/2 watt carbon resistor of 3 to 10 K nominal value. At all frequencies below 100 MC the ratio of X_{C_o} to R_1 is sufficiently large that it is unnecessary to neutralize the crystal unit shunt capacitance.

The crystal unit power dissipation rating also varies appreciably as a function of frequency. At frequencies below 10 MC the rating is such that it does not appreciably influence the oscillator design. Above 10 MC, however, it is an important factor as the subsequent discussion will show.

6-3. TRIODE AMPLIFIER CHARACTERISTICS

The basic triode amplifier design equations are given in Paragraph 3-5. These appear to be reasonably accurate, when suitable tube types are employed, for predicting amplifier small-signal characteristics at all frequencies below 50 or 60 MC, using parameter values derived from the plate characteristic curves and other related plots. The most useful of these plots are the small-signal transfer characteristics which relate U , R_p , and g_m to the DC plate current and voltage. If necessary, however, these parameters can be derived from the plate characteristics using the methods given in the majority of textbooks dealing with vacuum tube amplifier design.

In general, for this type of oscillator the effect of the tube reactive elements is small at frequencies below 60 MC, provided suitable tube types are selected at the higher frequencies. The tube can therefore be treated as an essentially resistive device, except, of course, insofar as the tube plate capacitance will influence the plate circuit tuning.

Above 50 or 60 MC, judging by measurements made during oscillator designs and evaluations, the accuracy of the basic amplifier design equations appears to gradually decrease, making them unsuitable for design purposes. The behavior of grounded grid triode amplifiers is then such that it appears as if the apparent plate resistance of the tube is reduced appreciably below the value applying at low frequencies. The effect of this is that, for a given plate load resistance, the amplifier voltage gain is substantially higher and the input resistance lower than predicted from the low frequency tube characteristics.

In view of this behavior, the most suitable method of design is to experimentally determine the amplifier characteristics for a variety of plate load resistance values. The method employed for the high-frequency oscillator designed for this handbook was to use an RX meter as the amplifier driving source and to measure the voltage gain and the amplifier input impedance. The measuring technique and the use of the derived data forms part of the design procedure for crystal oscillators above 60 MC and is fully discussed in Paragraph 6-17.

6-4. Limiting Action of a Tube

Because of the limitation on crystal unit dissipation, it is necessary to restrict the feedback power derived from the amplifier, which in turn necessitates limiting the plate signal voltage to a compatible level. Because of the large signal capabilities of a vacuum tube amplifier, obtaining signal limiting at a suitable level is a major design task at frequencies above a few megacycles where the requirements are particularly critical.

There are two ways in which the tube can be made to perform this function, one of which relies on the non-linear voltage gain relationship of the amplifier as a function of signal level. Referring to Figure 6-3, if the plate voltage and plate circuit load line are as designated by the symbol A, a signal of the amplitude indicated by A' and A'' would require a much larger negative than positive grid signal voltage excursion. That is, the instantaneous gain of the amplifier is severely reduced during the positive plate signal voltage swing, and consequently a form of plate signal limiting occurs.

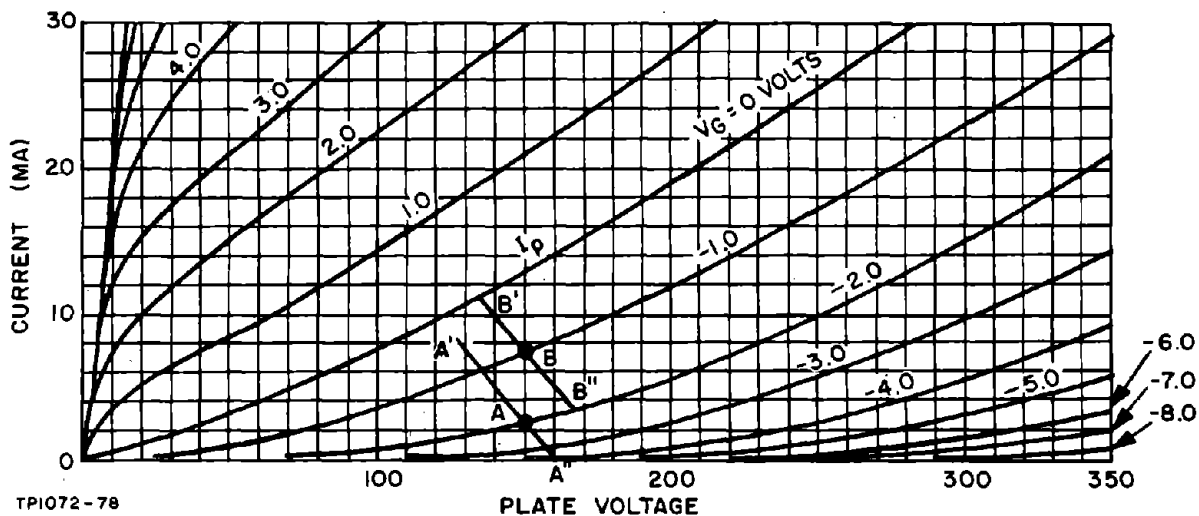


Figure 6-3. Triode Plate Characteristics

This method of introducing plate signal limiting is seldom possible in series oscillators where the emphasis, due to the crystal unit characteristics, is usually on obtaining a high voltage gain at as low a plate resistance level as possible. This generally involves operating the tube at high current levels where the plate characteristic curves approach a linear slope. This is the exact opposite of the tube operating conditions favoring current limiting, which usually occurs when the tube is biased at relatively low plate current levels and, hence, in a region where the plate resistance is high. In general, therefore, this is not a practicable method of providing plate signal voltage limiting in oscillators.

The other method of plate signal limiting depends on the action of the diode formed by the grid and cathode of the tube. Referring again to Figure 6-3, if the DC plate voltage and the plate circuit load line are as designated by the symbol B, a grid-cathode signal voltage sufficient to produce a plate voltage swing from B' to B'' will forward-bias the diode on the negative peak of the plate voltage swing, tending to limit the tube drive voltage amplitude. The signal level at which limiting occurs is a function of the tube DC operating point, the total DC grid-to-cathode resistance, and the plate load resistance.

The DC operating point in conjunction with the plate circuit load line determine the level at which limiting can commence as denoted approximately by the intersection of the load line with the plate characteristic curve for zero grid voltage. The actual point at which a significant degree of limiting will occur, however, is a function of the grid-cathode circuit DC resistance and, to a lesser extent, the DC plate current of the tube. If the DC resistance of the grid-cathode circuit is low, the increased loading of the signal source by the diode will not cause substantial limiting until the grid has an appreciable instantaneous positive bias relative to the cathode, and the plate signal voltage will then be larger than anticipated from the load line relationships. Alternatively, if the grid-cathode circuit DC resistance is high, the input signal loading contribution of the diode will be significant when the instantaneous grid-cathode signal voltage approaches zero volts, and the plate signal voltage will accordingly be decreased below that anticipated from the load line relationships.

The signal limiting action of the tube is related to the DC plate current to the extent that, as the plate current level is decreased, a given amount of instantaneous grid current is more effective in producing signal limiting. The lowest grid-cathode signal level at which limiting can be made to occur is also a function of the diode characteristics. In a thermionic diode a few microamperes of current flow when the diode is reverse-biased, typically having a value of 5 to 10 UA when the cathode is positive relative to (in this case) the grid by 0.7 V and perhaps a value of 1 UA at 1 volt reverse-bias. At grid bias levels of 1 volt or larger, the effects of this current are negligible under all likely circuit conditions. But if a tube operating point which requires a grid bias voltage of less than 1 volt is desired, this current can substantially affect the bias condition achieved if the grid-cathode circuit DC resistance is high.

The oscillator circuit requirements are usually such that the only way in which a high cathode-grid circuit DC resistance can be obtained is by using a high-value grid leak resistor and, depending on the amplifier configuration, an associated coupling or decoupling capacitor. Under these conditions, the relatively large quiescent grid current flowing at bias levels of less than 1 volt charges this capacitor in the sense that increases the grid bias level. Consequently, the desired grid bias point is not obtained, and in addition the amplifier voltage gain is less than that contemplated. Because of this behavior, it is therefore not practicable, using a high DC resistance grid-cathode circuit, to design for tube operation at grid bias levels of less than 1 volt with any assurance of obtaining the expected amplifier gain or input resistance.

If the relative limiting characteristics of a triode, having a high DC grid-cathode circuit resistance and operating at a grid bias of 1 volt, are compared to those of the same triode having a low DC grid-cathode circuit resistance and operating at a grid bias of less than 1 volt, it appears that the former will cause limiting at a lower plate signal level. Consequently, this is considered

the most suitable design approach. It should be noted, however, that it is possible to obtain limiting at still lower levels by using a large DC grid circuit resistance and designing for a grid bias point below 1 volt. This is not satisfactory from the design viewpoint, however, because of the resulting uncertainty regarding the amplifier voltage gain and input resistance.

Having established a minimum grid bias voltage of 1 volt, it follows that the minimum plate voltage amplitude at which limiting commences is then primarily a function of the tube amplification factor and the plate load resistance. This can be seen by rotating a load line on the plate characteristics of Figure 6-3 and noting the plate voltage excursion obtained between the curves for grid voltages of 0 and -1 volt. When the plate load resistance is close to the value of the tube plate resistance, the plate signal negative voltage swing is approximately $\mu/2$. Since this is an amplifier load condition that is often approached, this value is a useful guideline for estimating the plate signal voltage level at which limiting can be achieved. Considering only the signal limiting characteristics of the tube, this would favor the use of low μ tubes. Unfortunately, in the frequency range where limiting is most critical, this type of tube is not compatible with other circuit requirements. The high μ , low R_p type tubes having amplification factors in the range of 50 to 70 are then to be preferred. Using the guideline previously stated, this suggests that the minimum level at which plate signal limiting can be attained is approximately 20 VRMS. This value will subsequently be used as a design condition.

6-5. Diode Limiting

It is also possible to use an auxiliary circuit to provide the plate voltage limiting action. One such method is shown in Figure 6-4. In this circuit the diode connected to the plate of the tube is reverse-biased by the volt-drop across resistor R' . Consequently, for peak plate signal voltage amplitudes

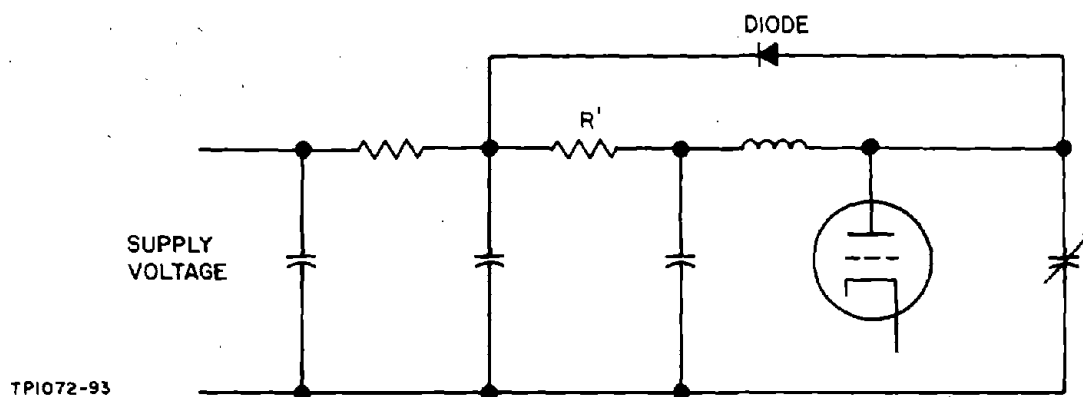


Figure 6-4. Diode Limiter Circuit

smaller than the reverse-bias voltage, the diode has no effect on the circuit operation. But when the peak plate signal voltage amplitude attempts to exceed this bias level, the diode conducts and the signal amplitude is stabilized. This circuit provides a means of limiting the plate signal voltage at virtually any desired amplitude and almost entirely divorces the limiting action from the amplifier, permitting the amplifier to now be optimized for its sole function of amplification.

The characteristics required of the diode are as follows:

- (a) Low capacitance and high dynamic resistance relative to the amplifier load at the operating reverse-bias voltage.
- (b) The peak inverse voltage rating must exceed the peak-to-peak signal voltage.
- (c) Good rectification efficiency at the operating frequency.

The 1N3062 family of diodes has proved satisfactory for this function at frequencies up to 200 MC. These have a capacitance of approximately 1.5 PF at 10 V reverse-bias and a dynamic resistance in excess of 100 K at 20 MC. If operation at temperatures above 80°C is not required, the 1N67A germanium point-contact diode (which is less costly) should also be suitable at the lower frequencies and possibly at higher frequencies, judging by experimental results obtained at 20 MC.

6-6. MAJOR FACTORS INFLUENCING DESIGN

There are two major factors that have a great influence on the impedance and voltage level relationship required between the various circuits that make up the oscillator. One of these is the relationship required between the crystal unit resonance resistance and its driving source and load resistances.

Paragraph 1-8 shows that if the phase-shifting capability of the crystal unit and hence its frequency stabilizing property is not to be unduly degraded by the remainder of the oscillator circuit, the terminating resistance levels on both sides of the crystal unit should be small in comparison to the crystal unit resonance resistance. Ideally these should be negligibly small in comparison to R_p , but in practice, with the simple type of circuit considered here, this cannot be approached and a compromise is necessary. For any type of crystal unit, at any given frequency, that unit having the largest permissible value of resonance resistance for its type will have the worst phase-shifting capability.

Therefore, in an oscillator the worst performance in this respect can be expected for this worst-case crystal unit. Since the oscillator should operate

satisfactorily with any crystal unit meeting the type specification, this worst-case condition of operation is the one which should be considered when arriving at a suitable compromise value of crystal unit terminating resistance. The phase-shifting capability of the crystal unit in the oscillator circuit relative to that of the crystal unit alone is given in Paragraph 1-8 (when R_r is replaced by $R_r \text{ max}$) as:

$$\frac{d\phi_1}{dQ_s} \bigg/ \frac{d\phi}{dQ_s} = \frac{R_r \text{ max}}{R_r \text{ max} + R_l + r} \quad (6-1)$$

where r and R_l are the crystal unit drive source and load terminating resistances, respectively.

Substituting relative values into Equation (6-1) shows that if the total terminating resistance is equal to $R_r \text{ max}$, $0.5 R_r \text{ max}$, or $0.33 R_r \text{ max}$, the circuit phase-shifting capability is, respectively, 50, 67, or 75 percent of that of the crystal unit. The last of these values causes a relatively small degradation and is a suitable choice of terminating resistance level, disregarding all other considerations. Except when using diode limiting, however, the characteristics of triode amplifiers are such that, at the crystal dissipation levels allowed, this type of oscillator would be impractical over a wide range of frequencies if the total terminating resistance was restricted to this value. In order to obtain design feasibility it has been found necessary in practice to compromise further and to regard a total terminating resistance equal to or less than $R_r \text{ max}$ as acceptable at frequencies up to 60 MC.

The sacrifice in circuit phase-shifting capability incurred by this relaxation is not excessive, resulting in a reduction from 75 to 50 percent of that of the crystal unit. This is considered warranted by the resulting relaxation in amplifier limiting performance and gain requirements obtained:

In practice, it is difficult to control both the terminating resistance values simultaneously. Fortunately, the drive source resistance is usually found to be acceptable when attention is concentrated solely on the output terminating resistance.

The second factor having a major influence on design is the problem of preventing crystal unit overdrive posed by the relatively large signal level at which limiting occurs in tube amplifiers. The allowable signal voltage across the crystal unit is limited by its dissipation rating which should not be exceeded for any conditions of oscillator operation. When the crystal unit is operated into a terminating resistance, this in turn places a restriction on the allowable voltage at the crystal unit input terminal. This effect is considered in Paragraph

1-9 where the allowable input voltage is shown to be a function of the output terminating resistance, the relationship being:

$$V_{\max} = 2 \sqrt{P_{\text{CMAX}} \cdot R_i} \quad (6-2)$$

The allowable crystal unit input voltage at any frequency can be determined by relating R_i to $R_{r \text{ max}}$ for the known value of P_{CMAX} and applying Equation (6-2). This gives the values of V_{\max} shown in Table 6-2 for typical crystal unit types when R_i is chosen to provide a satisfactory crystal unit terminating resistance.

TABLE 6-2. V_{\max} AND $T_{V_0}^{-1}$ AS FUNCTIONS OF CRYSTAL UNIT CHARACTERISTICS

Frequency	$R_{r \text{ max}}$ (ohms)	P_{CMAX} (MW)	$R_i = 1/3 R_{r \text{ max}}$		$R_i = 0.5 R_{r \text{ max}}$		$R_i = R_{r \text{ max}}$	
			$V_{\max \text{ RMS}}$	$1/T_{V_0}$	$V_{\max \text{ RMS}}$	$1/T_{V_0}$	$V_{\max \text{ RMS}}$	$1/T_{V_0}$
90-170 KC	5000	2	3.6	5.5	4.5	4.5	6.3	3.2
170-250 KC	5500	2	3.8	5.4	4.7	4.2	6.6	3
200 KC	2500	2	2.6	7.7	3.2	6.2	4.5	4.5
500 KC	7500	2	4.5	4.5	5.5	3.6	7.7	2.6
1 MC	440	10	2.4	8.3	3	6.7	4.2	4.8
2 MC	185	10	1.6	12.5	1.9	10.5	2.7	7.4
5 MC	37	10	0.7	29	0.86	22	1.2	16.7
10 MC	20	10	0.52	38	0.63	32	0.9	22
10-15 MC	18	5	0.35	57	0.42	48	0.6	33
15-20 MC	15	5	0.32	63	0.39	51	0.55	36
10-61 MC	40	2	0.33	61	0.4	50	0.57	35

The crystal unit input terminal signal voltage is related to the plate signal voltage by the voltage transformation ratio T_{V_0} of the interposed impedance transforming network.

From the foregoing discussion of tube limiting characteristics and the values of V_{\max} given in Table 6-2, it is possible to estimate the maximum value of T_{V_0} which may be employed when using tube limiting at the various frequencies. Assuming the 20 VRMS plate signal limiting criterion previously arrived at, this gives the plate signal to crystal input signal ratios $\left(\frac{1}{T_{V_0}}\right)$ given in Table 6-2 for

the various relative crystal unit output terminating resistance levels. The values are given in this form because it allows a readier appreciation of the problem when it is realized that the product of the amplifier gain and the step-up voltage ratio of the amplifier input transformer (when used) must exceed the values of $\frac{1}{T_{V_0}}$. For example, using the values contained in the bottom line of Table 6-2, above 10 MC when R_i is equal to $1/3 R_{r \text{ max}}$, the voltage "gain" from the crystal output terminal to the plate circuit must be in excess of 61 because of the voltage reduction in the transformer connected between the tube plate and the crystal input terminal. A further attenuation occurs across the crystal unit, and in actuality the voltage "gain" from crystal output terminal to the tube plate would need to be in excess of 300. At the impedance levels involved, this is not feasible with the available triodes. If, alternatively, R_i is equal to $R_{r \text{ max}}$, the actual voltage "gain" required is approximately 100; a value that is just feasible using the most suitable tube type.

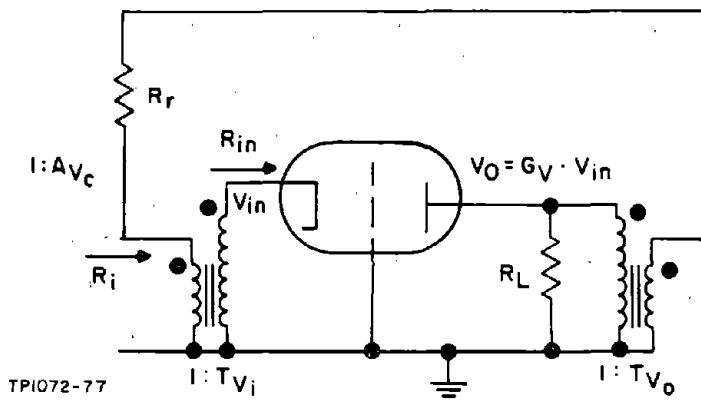
Above 10 MC, therefore, it is only practicable to use crystal output terminating resistance levels approaching the maximum resonance resistance of the crystal unit if tube limiting is employed. Using diode limiting, T_{V_0} can be increased to practically any desired value, reducing the requirements on the remainder of the circuit and allowing the use of a lower relative value of R_i .

Below 10 MC, the allowable values of T_{V_0} increase, and the amplifier requirements are then not as critical. And at the lowest frequencies, this effect is no longer a design problem.

6-7. OSCILLATOR LOOP GAIN EQUATIONS APPLICABLE BELOW 60 MC

Referring to Figure 6-5 the loop gain of the oscillator circuit can be conveniently divided into four factors as follows:

- (a) The amplifier voltage gain G_V from cathode to plate circuit.
- (b) The voltage ratio T_{V_0} of the impedance transforming network connected between the tube plate and the input side of the crystal unit.
- (c) The voltage attenuation A_{V_C} from the crystal unit input to output terminals.
- (d) The voltage ratio T_{V_i} of the impedance transforming network between the crystal unit output terminal and the amplifier input. Below 2 MC the amplifier input resistance provides a suitable terminating level for the crystal unit and an impedance transforming network is not required at the amplifier input. This factor is then ignored.



NOTE

The use of inductive transformers is purely diagrammatic. Other types may be used and are, in fact, often to be preferred.

Figure 6-5. Circuit Defining Loop Gain Factors

The loop voltage gain is, therefore:

$$G_{V_L} = G_V \cdot T_{V_0} \cdot A_{VC} \cdot T_{V_i} \quad (6-3)$$

For the worst-case design where R_R is equal to $R_{R \text{ max}}$, the factors in Equation (6-3) are as follows:

From Paragraph 3-3 the amplifier cathode input resistance and voltage gain are:

$$R_{in} = \frac{R_T + R_p}{\mu + 1} \quad (6-4)$$

and

$$G_V = \frac{(\mu + 1) R_T}{R_T + R_p} = \frac{R_T}{R_{in}} \quad (6-5)$$

The voltage ratio of the transformer at the amplifier input, assuming negligible losses, is:

$$T_{V_i} = \sqrt{\frac{R_{in}}{R_i}} = \sqrt{\frac{R_{in}}{k R_{r \max}}} \quad (6-6)$$

where R_i is the transformed amplifier input resistance which is related to $R_{r \max}$ by the expression:

$$k = \frac{R_i}{R_{r \max}} \quad (6-7)$$

A_{V_C} is the voltage division ratio of $R_{r\max}$ and R_i in series. That is:

$$AVC = \frac{R_i}{R_i + R_{r \max}} = \frac{k}{1+k} \quad (6-8)$$

The voltage ratio of the impedance transforming network interposed between the amplifier output and the crystal unit is a design variable which must be selected to satisfy both the loop gain and the crystal dissipation requirements. T_{V_0} is also related to the feedback network input resistance (neglecting losses) by the expression:

$$R_{FB} = \frac{R_i + R_{r \max}}{T_{V_0}^2} = \frac{(1 + k) R_{r \max}}{T_{V_0}^2} \quad (6-9)$$

The oscillator external load resistance reflected into the plate circuit is related to R_T and R_{FB} as:

$$R_T = \frac{R_{FB} \cdot R_L}{R_{FB} + R_L} \quad (6-10)$$

Substituting into Equation (6-3) for G_V , A_{V_C} , and T_{V_i} gives:

$$G_{V_L} = \frac{R_T}{\sqrt{k R_{in} \cdot R_{r \max}}} \cdot \frac{k}{(1 + k)} \cdot T_{V_0} \quad (6-11)$$

or, substituting for R_T in terms of R_{FB} and R_L :

$$G_{V_L} = \frac{R_L}{T_{V_0} \left[R_L + \frac{(1 + k) R_{r \max}}{T_{V_0}^2} \right]} \cdot \sqrt{\frac{k R_{r \max}}{R_{in}}} \quad (6-12)$$

For a worst-case design a small signal loop voltage gain of 1.4 is normally suitable to ensure satisfactory oscillation. Substituting this value for G_{V_L} then gives the relationship:

$$\begin{aligned} \frac{R_L}{(1 + k) R_{r \max}} &= \frac{1.4}{T_{V_0} \left[\sqrt{\frac{k R_{r \max}}{R_{in}}} - 1.4 T_{V_0} \right]} \\ &= \frac{1.4}{T_{V_0} \left[\frac{1}{T_{V_i}} - 1.4 T_{V_0} \right]} \end{aligned} \quad (6-13)$$

Equation (6-13) defines the relationships that must exist between the voltage ratios of the two transformers, the amplifier input resistance, the crystal unit output termination factor k , the oscillator external load, and the crystal unit resonance

resistance, if the small signal loop gain is to be adequate. This expression is too unwieldy to use directly as a design equation due to the number of variables involved; in order for it to be useful, a simplified presentation is required.

This is obtained by plotting $\frac{R_L}{(1+k) R_{r \max}}$ as a function of TV_0 using $\frac{1}{TV_1}$ as a parameter as shown in Figure 6-6.

For an amplifier whose input resistance is independent of its load resistance, which would be the case for a pentode or tetrode amplifier, the curves of Figure 6-6 completely define the possible oscillator relationships. For this type of amplifier, TV_1 is fixed once a selection is made of k and the amplifier DC operating conditions, and hence its mutual conductance and input resistance. All possible circuit relationships then lie on the curve having the appropriate value of $1/TV_1$ as a parameter. A suitable value of TV_0 is then selected on the basis of plate and crystal unit signal voltages.

For triode amplifiers, however, changes in R_T will substantially affect the value of R_{in} . And since R_T is a function of R_L , the relationship is not as straightforward, and it is then necessary to consider the effects of the amplifier load resistance on R_{in} and hence TV_1 . The amplifier total load resistance R_T will almost certainly lie in the range of $0.4 R_p$ to $2 R_p$, and relating this to Equation (6-4), the amplifier input resistance will then lie in the range of:

$$1.4 R_{in(s/c)} \leq R_{in} \leq 3 R_{in(s/c)} \quad (6-14)$$

where $R_{in(s/c)}$ is equal to $\frac{R_p}{\mu + 1}$, the input resistance when R_T is zero. Relating this to TV_1 then gives:

$$0.58 \sqrt{\frac{k R_{r \max}}{R_{in(s/c)}}} \leq \frac{1}{TV_1} \leq 0.85 \sqrt{\frac{k R_{r \max}}{R_{in(s/c)}}} \quad (6-15)$$

Equation (6-15) defines the likely range of values of $\frac{1}{TV_1}$ relative to the selected tube characteristics. With the aid of this relationship, while also considering the values of TV_0 dictated by the crystal dissipation, it is possible to locate the range of oscillator circuit relationships from which a suitable selection can be made.

In performing this process it is necessary to know the amplifier total load resistance R_T . This can be obtained by substituting for R_{FB} in Equation (6-10), giving:

$$\frac{R_T}{R_L} = \frac{1}{1 + \frac{TV_0^2}{(1+k)} \cdot \frac{R_L}{R_{r \max}}} \quad (6-16)$$

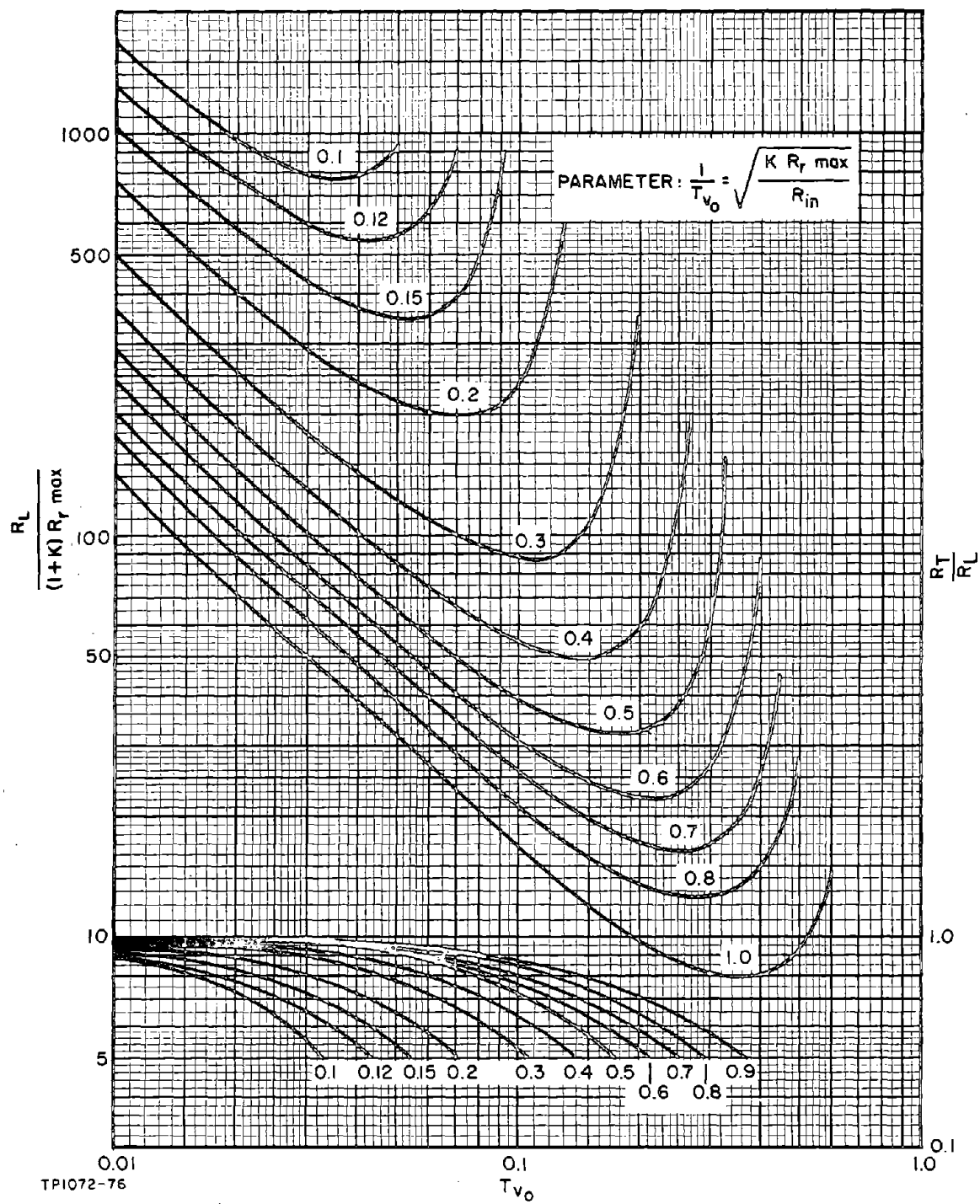


Figure 6-6. Oscillator Relationships

This expression is also plotted in Figure 6-6 using $\frac{1}{T_{V_i}}$ as a parameter.

6-8. DESIGN PROCEDURE FOR OSCILLATOR CIRCUITS, 90 KC TO 60 MC

Step 1 - Select a crystal unit type applicable at the desired operating frequency, and determine from the specification sheet the crystal unit dissipation rating $P_{C\text{MAX}}$ and maximum resonance resistance $R_{r\text{ max}}$ at this frequency.

Calculate the maximum allowable crystal unit input voltage for an output terminating resistance of $k \cdot R_{r\text{ max}}$, assigning to k values of 0.33, 0.5, and 1. The formula is:

$$V_{\text{max}} = 2 \sqrt{P_{C\text{MAX}} \cdot k \cdot R_{r\text{ max}}} \quad (6-17)$$

Estimate from the values of V_{max} obtained the maximum permissible values of T_{V_o} . At frequencies over 800 KC where high μ , low R_p triodes are most suitable, difficulty will probably be experienced in limiting the plate voltage to less than 20 VRMS using self-limiting, and the appropriate relationship is:

$$\text{Maximum } T_{V_o} \approx \frac{V_{\text{max}}}{20} \quad (6-18)$$

At frequencies below 500 KC where high R_p triodes are most suitable, the plate voltage can, if desired, be self-limited at a lower level, allowing the denominator term to be reduced to, say, 14.

Step 2 - Select a suitable tube type. At frequencies below 2 MC, a major factor influencing the selection will be the short-circuit input resistance $\frac{1}{g_m}$. Unless the designer is prepared to employ an impedance matching transformer between the crystal unit and the tube cathode, $\frac{1}{g_m}$ should be approximately in the range of 0.2 to 0.5 $R_{r\text{ max}}$. When connected as an amplifier, the cathode input resistance will then provide a satisfactory crystal unit terminating resistance level without introducing an excessive voltage attenuation between the crystal unit input terminal and the cathode.

Above 2 MC only low R_p , high μ triodes need be considered. This is dictated partially by the relatively low values of feedback network input resistance occurring at these frequencies, and partially by the high voltage gain required of the amplifier, due to the low value of T_{V_o} necessary to prevent crystal unit overdrive.

Above 20 or 30 MC, the stray reactive elements of the tube can be significant. This is discussed in Step 2 of the design procedure for triode oscillators above 60 MC which should be referred to when designing for operation above 20 MC.

A high μ is also desirable, although not essential at all frequencies.

Step 3 - Select a suitable operating point for the tube. At frequencies below 2 MC a major factor in the determination of the tube bias point will be to obtain a mutual conductance satisfying the relationship given in Step 2. Another requirement if self-limiting is employed will be that the operating point when viewed on the plate characteristics should be sufficiently close to the zero grid voltage curve that limiting will occur at a suitable level when considered relative to a typical load line.

At frequencies above 2 MC the major factor if self-limiting is employed will also be to find an operating point on the plate characteristics sufficiently close to the zero grid line curve to ensure adequate limiting. It is also usually necessary to minimize R_p as much as possible because of the relatively low input resistance of the feedback network. These two requirements generally necessitate operation under high current, low plate voltage conditions which, in turn, imply a low value of grid bias. If diode limiting is employed, a higher plate voltage is permitted, allowing a low R_p to be obtained at a higher grid bias voltage.

When using self-limiting the bias relationships are often critical, and experimental adjustment will frequently be required unless the choice of operating point is particularly fortunate. Tabulate the tube operating conditions selected (the DC plate voltage and current and the grid bias voltage) and the small signal characteristics (μ , R_p , and g_m) for these operating conditions.

Step 4 - Determine the short-circuit input resistance ($\frac{1}{g_m}$) of the tube for the selected tube operating conditions. At design frequencies above 2 MC where an amplifier input transformer is necessary, calculate the likely range of values of $1/T_{V_i}$ from:

$$0.58 \sqrt{\frac{k \cdot R_{r \max}}{R_{in(s/c)}}} \leq \frac{1}{T_{V_i}} \leq 0.85 \sqrt{\frac{k \cdot R_{r \max}}{R_{in(s/c)}}} \quad (6-19)$$

k should be assigned values of, say, 0.33, 0.5, and 1. The ranges of values of $\frac{1}{T_{V_i}}$ obtained and the maximum values of T_{V_o} obtained in Step 1 for the same k values locate the regions in Figure 6-6 suitable for investigation. For an

assumed value of k , feasible values of $\frac{R_L}{(1+k) R_{r \max}}$ must lie in a region bounded by the calculated range of values of $\frac{1}{T_{V_i}}$ and to the left of the maximum value of T_{V_o} calculated for that value of k in Step 1.

The process involved consists of selecting a value of $\frac{1}{T_{V_i}}$ lying within the range obtained for a particular value of k and locating a value of $\frac{R_L}{(1+k) R_{r \max}}$ on this curve which is compatible with the appropriate maximum value of T_{V_o} calculated in Step 1. The values of R_L and R_T are then obtained from the values of k , $\frac{1}{T_{V_i}}$, $R_{r \max}$ and the ratios of $\frac{R_T}{R_L}$ given in Figure 6-6. The value of R_T obtained is then used to calculate the actual amplifier input resistance from:

$$R_{in} = \frac{R_p + R_T}{\mu + 1} \quad (6-20)$$

Using this value of amplifier input resistance the actual voltage ratio of the amplifier input transformer that will give the assumed crystal unit terminating condition is calculated from:

$$T_{V_i} = \sqrt{\frac{R_{in}}{K \cdot R_{r \max}}} \quad (6-21)$$

The loop voltage gain is then calculated using the values of R_T , R_{in} , and T_{V_i} obtained in the three preceding calculations from:

$$G_{V_L} = \frac{k}{1+k} \cdot \frac{R_T \cdot T_{V_o} \cdot T_{V_i}}{R_{in}} \quad (6-22)$$

If the loop voltage gain obtained is 1.4 or larger, the design is feasible for the selected circuit relationships.

The least demanding circuit requirements occur when R_i , the transformed amplifier input resistance presented to the crystal unit is equal to $R_{r \max}$; that is, k equal to 1. It is suggested that this value be assigned to k for the first set of loop gain calculations. If a loop voltage gain well in excess of 1.4 is then obtained for a value of R_L sufficiently low to be feasible, k may then be decreased to improve the design. This may be done by estimating from the loop voltage gain formula the allowable decrease in k or, alternatively, by repeating the loop gain calculations for a lower assumed value of k . If the former method is used it should be noted that T_{V_i} will be affected by the change in the value of k .

Similarly, if the loop voltage gain calculated for k equal to 1 is only slightly less than 1.4 (say, 1.2 or larger), it may be possible to increase the loop gain sufficiently by increasing R_L and hence R_T . Here again, it should be noted that the change in R_T will also change R_{in} and T_{V_i} .

If the loop voltage gain calculated for k equal to 1 is much less than 1.4, it will be necessary to repeat the loop gain calculation commencing with a smaller assumed value for $1/T_{V_i}$.

The design feasibility will be dependent on obtaining a value of R_L which is practicable when referred to the actual oscillator external load and the losses to be expected in the plate tuning circuit and feedback network. These losses are taken into account by considering them to form a part of R_L . The actual value of R_L is then given by:

$$\text{Actual } R_L = \frac{R_L \cdot R_{LP}}{R_{LP} - R_L} \quad (6-23)$$

where R_{LP} is the effective parallel tuned circuit losses appearing at the plate terminals.

At frequencies above 10 MC and particularly above 30 MC, R_{LP} can be an appreciable part of the oscillator load, even when the Q of the network is high. This is due to the fact that the plate circuit tuning capacitance C will need to be from 10 to 20 PF. This is related to R_{LP} by the formula:

$$R_{LP} = \frac{Q}{\omega C} \quad (6-24)$$

At 50 MC, for example, the reactance of 20 PF is 160 ohms, giving R_{LP} equals 16 K for Q equal to 100.

At design frequencies below 2 MC where an amplifier input impedance transforming network is not used, T_{V_i} has a value of 1. Attention is then confined to the circuit relationships given by the lowest curve of Figure 6-6 in the region to the left of the appropriate maximum value of T_{V_o} determined in Step 1. The process is then the same as described above, $\frac{R_L}{(1+k) R_{r \max}}$ is read from Figure 6-6, and a value of k is assumed based on the short-circuit amplifier input resistance. R_L is calculated for the assumed value of k , and R_T determined from the plot of $\frac{R_T}{R_L}$ for $\frac{1}{T_{V_o}}$ equal to 1.

The actual amplifier input resistance for the calculated value of R_T is obtained from:

$$R_{in} = \frac{R_p + R_T}{\mu + 1} \quad (6-25)$$

This value of R_{in} is compared to $R_{r \max}$ to determine if a suitable crystal unit terminating condition has been obtained. The equation is:

$$k = \frac{R_{in}}{R_{r \max}} \quad (6-26)$$

If k is equal to or less than 1, the termination is considered satisfactory, although it is desirable when possible that R_{in} should be $0.5 R_{r \max}$ or less.

The loop gain is calculated from:

$$G_{V_L} = \frac{k}{1+k} \cdot \frac{R_T \cdot TV_o}{R_{in}} \quad (6-27)$$

If this is 1.4 or larger, the design is feasible.

The further manipulations required to finally fix the circuit relationships are then as previously described for designs above 2 MC.

The crystal unit terminating resistance level on the input side is difficult to ascertain since the amplifier output resistance is a function of the drive source resistance. A rough estimate can, however, be obtained by considering the amplifier output resistance to be equal to R_T . The crystal unit input terminating resistance is then equal to $R_T \cdot T_{V_o}^2$. This will usually be small compared to the output terminating level.

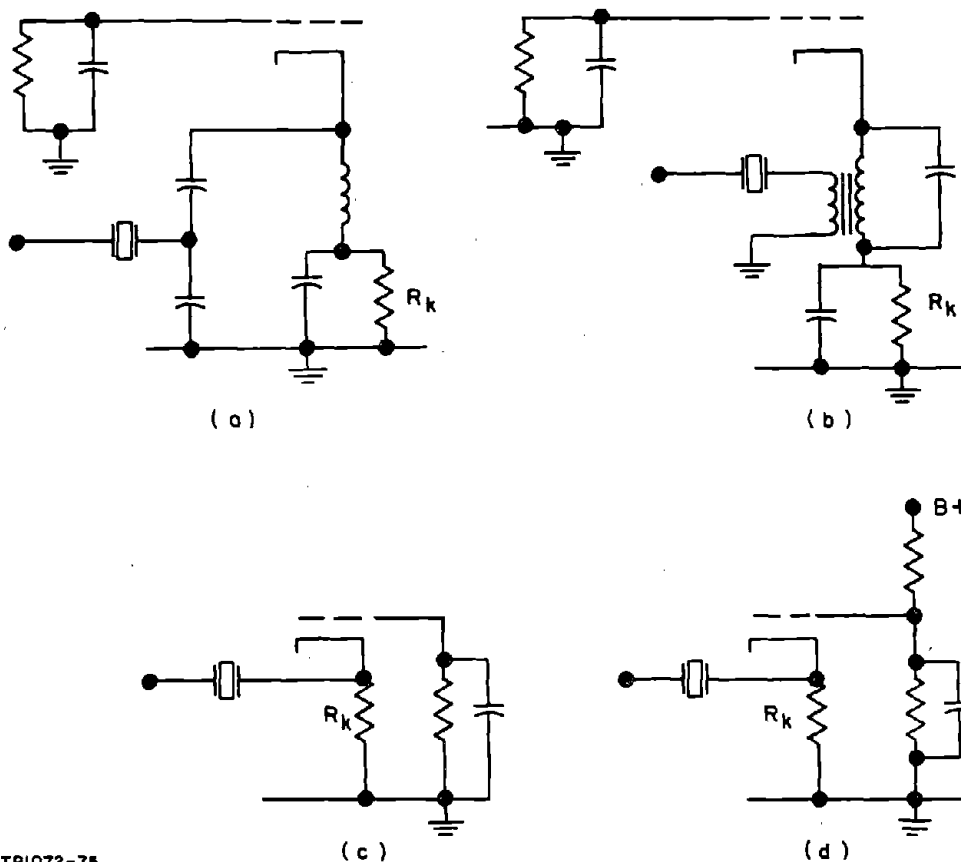
Step 5 - The remaining circuit component values are determined as follows:

(a) Cathode Bias Circuit

At frequencies above 2 MC the inductor associated with the impedance transforming network at the amplifier input can be used as a high AC-low DC impedance cathode current feedpath, as shown in Figure 6-7 (a) and (b). The cathode bias resistor R_k is then calculated for the DC plate current and grid bias previously selected from:

$$R_k = \frac{V_G}{I_p} \quad (6-28)$$

Below 2 MC this cathode inductor is not required as part of an impedance transforming network and, particularly at frequencies below 500 KC, it may not be desirable to use an inductor simply for the purpose of providing a high AC-low DC impedance cathode current feed. The reasons for this are that, in order to prevent a possible reduction in loop gain and also loop phase angle errors, this inductor will either need to be tuned, or alternatively, its reactance chosen sufficiently large so as to cause a negligible phase shift between the signals at the input and output terminals of the crystal.



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Figure 6-7. Cathode DC Current Feed Circuits

To meet the latter requirement the reactance of the inductor will need to be at least four times the resistance of the parallel combination of $R_r \text{ max}$ and R_{in} . Since $R_r \text{ max}$ and R_{in} will be of the order of several kilohms at frequencies below 500 KC, this may not be desirable because of the relatively large inductance required. The alternative is a resistive feed as shown in Figure 6-7 (c); the problem then is that of biasing the tube at the chosen operating point without appreciably reducing the amplifier input resistance and hence the loop gain because of loading caused by R_k . Frequently, it will be found that R_k is comparable with R_{in} if the biasing circuit of Figure 6-7 (c) is considered and a method of increasing R_k to at least 10 times R_{in} is required. One way in which this can be achieved is shown in Figure 6-7 (d) where the grid is biased positive relative to ground at a potential which enables the desired cathode current to be supplied via a suitably large value of resistance.

(b) Cathode Impedance Transforming Network

The amplifier input impedance transforming network may be of either of the types shown in Figure 6-7 (a) or (b). The first of these circuits will probably be most useful at frequencies above 20 MC, and the latter below 20 MC. The inductive transformer is perhaps the more economically desirable of the two, provided that the high coefficient of coupling between windings required by phase shift considerations can be achieved.

The winding of an RF transformer to obtain a high degree of coupling is in a sense an art which can only be learned by experience, and it is difficult to assess what can be achieved at a particular frequency at the impedance levels considered here. Judging from the writer's experience, couplings of 0.9 are difficult to achieve at frequencies over 20 MC at these impedance levels, although someone more skilled in suitable winding techniques, or with access to better toroidal cores would probably set a higher limit.

For someone with no experience in the techniques involved, it is probably better to use the capacitive divider circuit at all frequencies at least during the initial design stage, trying the inductive transformer if desired after all other features of the design have been firmed.

At the lower frequencies large values of capacitance will be required because of the condition that the total capacitive reactance should be small relative to the terminating resistance levels. This will probably necessitate the use of a variable inductor to adjust the circuit to resonance at the design frequency.

The design formula for these networks is given in Section 4. It is recommended that experimental verification of the impedance transformer design should be obtained; an RX meter or other similar bridge will be found useful for this purpose, together with phase angle measuring equipment, if available.

To obtain a transformer phase angle approaching zero degrees, the cathode side of the network should, of course, be tuned to resonance. No allowance is made in the design for losses occurring in this circuit other than that given by assuming a loop voltage gain of 1.4. The effective parallel resistance of the impedance transformer should therefore not be less than, say, 10 times the amplifier input resistance.

(c) Plate Circuit Impedance Transforming Network

The inductive transformer and the capacitive divider type impedance transforming networks are also appropriate for this circuit, and many of the feasibility considerations discussed in (b) are applicable here. The impedance levels involved are much higher, however, and the highest frequency at which

the inductive transformer can be used is correspondingly reduced; the larger number of turns required in the windings and the large primary-to-secondary turns ratio make it difficult to obtain a coupling coefficient of 0.9 while keeping losses low at frequencies above, say, 1 or 2 MC. The capacitive divider circuit is therefore probably the more appropriate circuit at all frequencies above 800 KC. Independent of the choice of impedance transformer type, it is desirable that the circuit should be experimentally evaluated to ascertain its correct functioning before incorporation into the oscillator circuit. Section 4 should be referred to for the design equations.

(d) Amplifier Grid Circuit

The amplifier grid circuit will normally consist of a parallel combination of a resistor and a capacitor. The value of capacitance required is determined by the need that the grid should be effectively at AC ground at the operating frequency. It will usually be satisfactory if the reactance is less than 10 ohms. Above 10 MC, the type of capacitor and the lead dress may be critical factors because of self-resonance. The ideal choice is then a capacitor that is self-resonant at the design frequency. A grid-dip meter is useful for determining a suitable value of capacitance meeting this condition.

The grid leak resistor can be conveniently used to adjust the level at which signal limiting occurs. A large grid resistance causes limiting at a lower signal level relative to a smaller resistance. The selection of a suitable grid resistor value is therefore made during the initial testing of the breadboarded oscillator. A 10 to 100 K resistor is a suitable one with which to commence testing.

Step 6 - Experimental Adjustments

After constructing the breadboard, it is helpful to check the loop gain experimentally. This can be done by applying a signal, at the design frequency, to the crystal output terminal point via a resistor equal to $R_{r \max}$ with the crystal unit removed from the circuit. An oscillator load resistance equal to R_L should be connected across the plate circuit and another resistor equal to $R_{r \max} + R_i$, simulating the feedback network load, should be connected from the crystal unit input terminal point to ground. The plate and cathode circuits are then tuned for maximum signal at the crystal unit input terminal points and a comparison made of this voltage relative to that at the signal input side of the resistor simulating $R_{r \max}$. Satisfactory oscillation will only be feasible if this ratio is larger than 1.3. The resistors used in this test should be measured at the design frequency, particularly above a few megacycles per second.

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Another useful test is to then disconnect the resistance simulating the feedback network load and substitute the resistor simulating $R_{r \text{ max}}$ across the crystal unit socket. Oscillation should then occur at a frequency close to the design frequency if the phase errors are small.

6-9. DESIGN EXAMPLES, 90 KC TO 60 MC

The following design calculations are presented to illustrate the process of selecting a suitable set of circuit relationships.

6-10. 1 MC, 12AT7 Series Oscillator

Crystal Unit Characteristics (CR-19A/U)

$$R_{r \text{ max}} = 440 \text{ ohms}, P_{C\text{MAX}} = 10 \text{ MW}$$

<u>k</u>	<u>V_{max} (RMS)</u>	<u>TV_O max</u>
0.33	2.4	0.12
0.5	3	0.15
1.0	4.2	0.21

Tube Characteristics (12AT7)

For $E_p = 120 \text{ VDC}$, $V_G = -1.2 \text{ VDC}$, and $I_p = 4 \text{ MA}$,

$$R_p = 15 \text{ K}, \mu = 58, g_m = 3.9 \text{ MA/volt.}$$

$$R_{in(s/c)} = 260 \text{ ohms} \approx 0.6 R_{r \text{ max}}.$$

For $TV_O = 0.1$, $k = 1$, Figure 6-6 gives:

$$R_L = 14.3 \text{ K}, R_T = 12.3 \text{ K}, R_{in} = 460 \text{ ohms.}$$

$GV_L = 1.37$, $R_T \cdot TV_O^2 \approx 120 \text{ ohms}$, and the total crystal unit terminating resistance is approximately $1.3 R_{r \text{ max}}$.

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6-11. 20 MC, 6CW4 Series Oscillator Using Diode Limiting

Crystal Unit Characteristics (CR-19A/U)

$$R_{r \max} = 15 \text{ ohms, } P_{C \max} = 5 \text{ MW}$$

<u>k</u>	<u>V_{max} (RMS)</u>	<u>T_{V₀ max}</u>
0.33	0.32	0.016
0.5	0.39	0.02
1	0.55	0.028

Tube Characteristics

For $E_p = 110 \text{ VDC}$, $V_G = -0.9 \text{ VDC}$, $I_p = 6 \text{ MA}$, and $R_p = 7 \text{ K}$.

$$\mu = 63, R_{in(s/c)} = 110 \text{ ohms.}$$

Let the crystal unit output terminating resistance be 8 ohms ($k = 0.53$), then

$\frac{1}{T_{V_i}}$ (s/c) is 0.27 and:

$$0.16 \leq \frac{1}{T_{V_i}} \leq 0.23$$

Setting $\frac{1}{T_{V_i}}$ equal to 0.2 and assuming diode limiting, a suitable set of circuit relationships is obtained for $T_{V_0} = 0.03$ where:

$$R_L = 300 \times 23 = 6.9 \text{ K, } R_T = 0.8 \text{ K, } R_L = 5.5 \text{ K,}$$

and

$$R_{in} = 200 \text{ ohms.}$$

$$\text{Actual } G_{V_L} = 1.45, R_T \cdot T_{V_0}^2 \approx 8 \text{ ohms.}$$

The total crystal unit terminating resistance is approximately equal to $R_{r \max}$.

The diode clipping level should be set to give V_{\max} less than 0.39 VRMS for a crystal unit having a resonance resistance of 8 ohms. This corresponds to a plate signal voltage level of 13 VRMS.

Using a capacitive divider amplifier output impedance transforming network and with the notation of Section 4, the network values are obtained as follows:

$$X_{(C_1 + C_2)} \leq \frac{1}{3} (R_{r \max} + R_i) = 8 \text{ ohms,}$$

giving:

$$C_1 + C_2 \geq 1000 \text{ PF}$$

$$\frac{C_1 + C_2}{C_1} = \frac{1}{0.03}$$

Therefore:

$$\frac{C_2}{C_1} = 32$$

Selecting $C_2 = 1000 \text{ PF}$ gives $C_1 = 32 \text{ PF}$.

The plate circuit inductor was selected to resonate with 44 PF to allow for the tube plate capacitance, strays, and the capacitance of the trimmer. This requires an inductance of 5.8 UH. The effective parallel resistance of the inductor was 28K.

An inductive transformer was employed at the amplifier input. The voltage ratio required is 5, and this was obtained using 5-turn and 1-turn windings on a toroidal core having a specified permeability of 400. The 5-turn winding was close wound on the core, and this was tightly overlaid with the 1-turn winding, consisting of 6 parallel wires arranged to envelope the 5-turn winding. The primary and secondary winding leads were brought out from the core as twisted pairs to reduce leakage reactance. Measurements indicated that the coupling coefficient was 0.9, the parallel loss resistance measured at the cathode winding terminals 1.8 k, and the required resonating capacitance 32 PF. A fixed tuning capacitance of 36 PF gave good oscillator frequency correlation.

A 1N3064 diode was selected to provide signal limiting. At a reverse bias of 12 V, the diode capacitance was 1 PF and its parallel resistance 150 K.

R_L therefore consists of the actual load and 150 K and 28 K in parallel. The actual plate load is then 10 K. This was later increased to 11 K because oscillation would not commence for a worst-case design ($R_r = R_r \text{ max}$) when the supply voltage was decreased by 20 percent.

A diode reverse bias of 12 VDC was found suitable for preventing crystal unit overdrive.

6-12. 20 MC Series Oscillator (6CW4 Triode) Evaluation Data

Crystal Units (CR-19A/U)	Series Resonance Frequency (MC)	R_r (ohms)
1	19.999710	7
2	19.999980	8
3	19.999980	8
4 (Unit 3 with 7 ohm series resistor)	19.999840	15

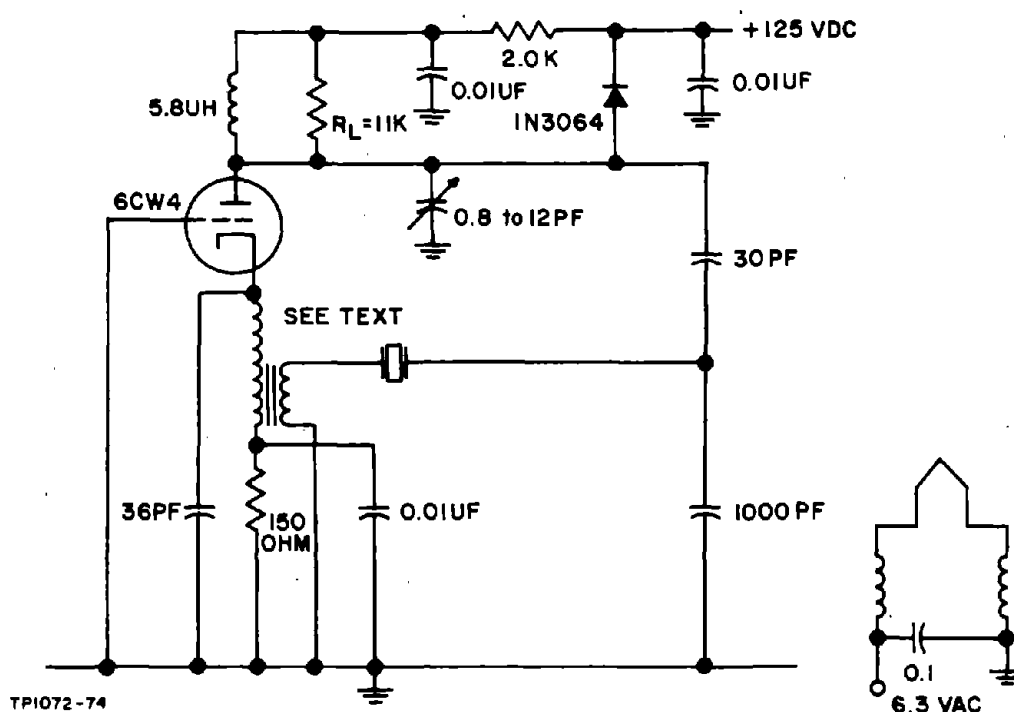


Figure 6-8. 20 MC Triode Series Oscillator, Schematic Diagram

Design Evaluation Data
(All results for worst-case crystal unit; $V_o = 11$ VRMS)

Effects of	Change
+15% B+ Change on Oscillator	Frequency V_o
	1 PPM $\Delta V_o = +20\%$

Design Evaluation Data (Cont)

Effects of		Change
-20% B+ change on oscillator	Frequency V_o	1 PPM $\Delta V_o = -30\%$
$\pm 10\%$ change in R_L on oscillator	Frequency V_o	± 1 PPM $\Delta V_o = \pm 10\%$
$\pm 10\%$ change in heater voltage on oscillator	Frequency V_o	$< \pm 1$ PPM $\Delta V_o < \pm 3\%$
-55°C to $+105^\circ\text{C}$ change in ambient temperature on oscillator	Frequency V_o	± 28 PPM $\Delta V_o = \pm 7\%$
Contribution of oscillator circuit to frequency deviations in temperature test		$< \pm 3$ PPM
Interchanging crystal units on oscillator	Frequency Miscorrelation V_o	± 2 PPM $\Delta V_o = \pm 22\%$

6-13. 50-MC Triode (6CW4) Series Oscillator

Crystal Unit Characteristics (CR-72/U)

$$R_r \text{ max} = 40 \text{ ohms}, P_{\text{CMAX}} = 2 \text{ MW}$$

k	V_{max}	$T_{V_o \text{ min}}$
0.33	0.33	0.016
0.5	0.4	0.02
1	0.57	0.028

Tube Characteristics

For $E_p = 110 \text{ VDC}$, $I_p = 6 \text{ MA}$, $V_G = -0.9 \text{ V}$, $R_p = 7\text{K}$, $\mu = 63$,
 and
 $R_{\text{in(s/c)}} = 110 \text{ ohms}$.

Let

$$R_i = 40 \text{ ohms (k = 1), then } \frac{1}{T_{V_i}} \text{ (s/c) is 0.6}$$

and:

$$0.35 \leq \frac{1}{T_{V_i}} \leq 0.51$$

$$\text{For } \frac{1}{T_{V_i}} = 0.4, T_{V_o} = 0.025, R_L = 12K, R_T = 11.5K,$$

$$R_{in} = 290 \text{ ohms, and } G_{V_L} = 1.32.$$

If T_{V_o} is made equal to 3 and R_T equal to 13 K, R_i is then 35 ohms, k is 0.88, and G_{V_L} is 1.43. R_L is then 14.6 K. $R_T \cdot T_{V_o}^2 \approx 8$ ohms. The total crystal unit terminating resistance is therefore approximately $1.1 R_{r \text{ max}}$.

Using a capacitive divider amplifier output network and with the notation of Section 4, the network values are obtained as follows:

$$X_{(C_1 + C_2)} \leq \frac{1}{3} (R_{r \text{ max}} + R_i) = 25 \text{ ohms}$$

giving:

$$C_1 + C_2 \geq 130 \text{ PF}$$

$$\frac{C_1 + C_2}{C_1} = \frac{1}{0.025} = 40$$

Therefore:

$$\frac{C_2}{C_1} = 39$$

Selecting C_2 as 390 PF gives:

$$C_1 = 10 \text{ PF}$$

The plate circuit inductor was selected to resonate with 20 PF, requiring an inductance of 0.5 UH. The effective parallel resistance of the inductor was 35 K, and that of the resonant circuit consisting of the inductor and the tuning capacitance network was 22 K. A capacitive divider network was also selected for the amplifier input transforming network. The relationships are:

$$X_{(C_1 + C_2)} \leq \frac{1}{3} (R_T \cdot T_{V_o}^2 + R_{r \text{ max}}) = 16 \text{ ohms}$$

$$C_1 + C_2 \geq 200 \text{ PF}$$

$$\frac{C_1 + C_2}{C_1} = 3$$

$$\frac{C_2}{C_1} = 2.$$

Selecting C_2 as 320 PF gives:

$$C_1 = 160 \text{ PF.}$$

The cathode inductor must therefore resonate with approximately 106 PF plus an additional 20 PF to allow for tuning. This requires an inductance of 0.04 UH.

R_L consists of the actual load in parallel with 22 K. The actual plate load is then 42 K.

The schematic of the circuit is shown in Figure 6-9. This design was breadboarded and partially tested but was not evaluated in detail. The partial testing consisted of ensuring that satisfactory oscillation occurred when a crystal

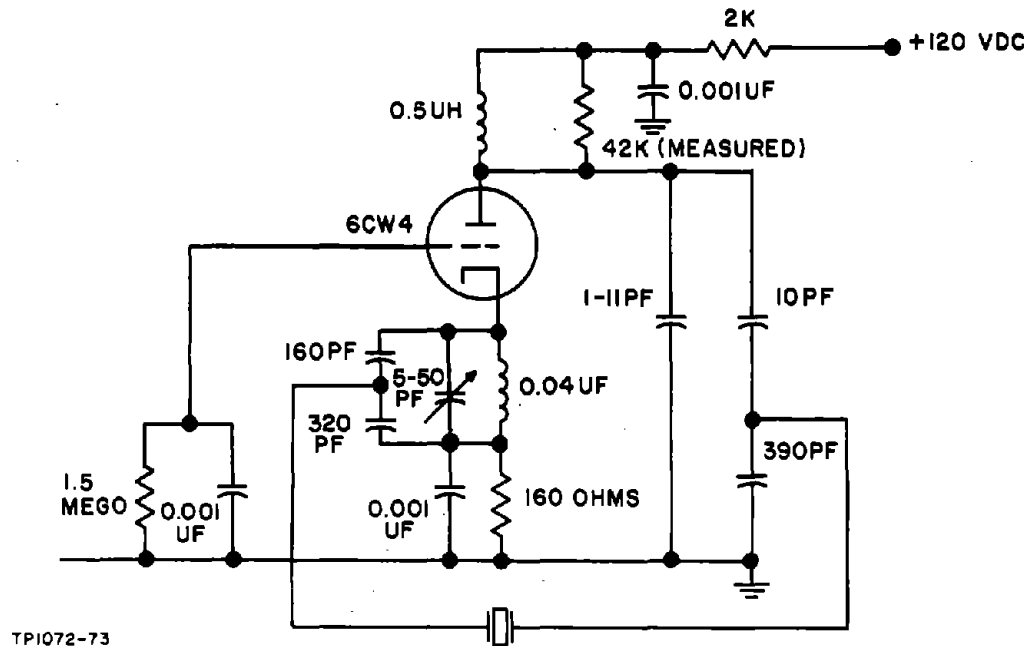


Figure 6-9. 50-MC Series Oscillator Circuit

unit having a resonance resistance of 40 ohms was in circuit and that the crystal unit dissipation could be held below 2 MW. Both of these conditions were satisfied, the latter requiring a 1.5 megohm grid leak resistor. The oscillator frequency correlation was within ± 5 PPM for several crystal units having resonance resistances of from 14 to 40 ohms. Oscillation would commence when operated at a reduced supply voltage of 90 volts. The tube could be changed without substantially affecting the oscillator performance. Voltage measurements at various points around the oscillator loop with the worst-case crystal in circuit indicated that the circuit was behaving much as predicted by the design calculation.

The plate circuit is very critical in this design, with the inductor and the capacitor network contributing the major part of the amplifier load. If a repetition of this design is attempted, care will be necessary in selecting the components of this network and measurement of their combined resistance before installation in the circuit is recommended. Otherwise, the amplifier load may be too small, preventing oscillation under worst-case conditions.

6-14. DESIGN OF SERIES OSCILLATORS, 60 to 200 MC

At high frequencies the characteristics of triodes appear to become frequency dependent. Judging from measurements of amplifier input impedance and voltage gain, the parameter affected most is the tube plate resistance which appears to decrease with increasing frequency. The effect of this on the amplifier characteristics is, for a given total load R_T , to increase the voltage gain and decrease the input resistance relative to what would be predicted by calculations based on the tube low-frequency parameters.

Insufficient measurements have been made of the characteristics of triode amplifiers to allow an estimate of the lowest frequency at which a significant difference occurs between measured and calculated characteristics. Presumably the effect depends to a great extent on the physical structure of the tube and is therefore likely to vary markedly between tube types. It is therefore uncertain as to what frequency should be employed as a transition point at which to adopt the experimental method of amplifier characterization. It does appear, however, that the change in amplifier behavior occurs above 60 MC in the types of tubes likely to be considered for use at these frequencies, making this (for want of a better criterion) a suitable transition frequency.

Another factor favoring an experimental approach above 60 MC is the increasing effect of stray circuit reactance. This may have an appreciable effect on the amplifier characteristics, even to the extent in severe cases of causing parasitic oscillation. The circuit layout and lead dress is therefore often an important design factor and, furthermore, one which can only be dealt with adequately using an experimental approach.

6-15. Feasible Design Requirements

It is evident from the preceding discussion of design below 60 MC that, at frequencies above 10 MC when using tube limiting, a critical selection of circuit relationships is necessary to fulfill the various design conditions. The relationships between the amplifier and crystal unit characteristics are such that the design is only feasible when using the most suitable tube types. This degree of design refinement is acceptable because of the ease with which the amplifier characteristics can be determined by calculation, it being possible to investigate a number of amplifier operating conditions in a short time. At these higher frequencies where the amplifier characteristics have to be investigated experimentally, this is no longer the case. The determination of the amplifier characteristics is then a relatively lengthy process, and it is no longer practicable to attempt the same degree of circuit optimization. It has therefore been found necessary, in order to keep the design process realistic, to relax the design conditions.

This relaxation is obtained in two ways: firstly, by considering that diode limiting is a necessity, and secondly, by relaxing the requirement on the crystal unit terminating resistance level. The first of these allows an increase in the plate circuit impedance transforming network voltage ratio, in turn reducing the amplifier voltage gain required. The second reduces the signal attenuation between the crystal unit input and output terminals, also decreasing the amplifier voltage gain required.

The advantage to be gained in relaxing the crystal unit terminating requirements is not too great unless a circuit simplification can also be obtained. This is feasible because of the reduction in loop gain made possible by the stipulation of diode limiting. Consideration of the characteristics of the types of triodes most suitable for this application indicates that, when used in the grounded grid configuration, the amplifier input resistance will almost certainly be below 250 ohms.

Relating this to the crystal unit series resistance shows that above 125 MC R_{in} will not be more than $2.5 R_1 \text{ max}$. Accepting this as a suitable terminating level then obviates the need for an impedance transforming network at the amplifier input, resulting in a worthwhile circuit simplification.

Below 125 MC, in the worst-case, R_{in} will be $5 R_r \text{ max}$. This is an undesirably large terminating level, but an improvement to a level of 2 to 3 $R_r \text{ max}$ can be obtained when necessary by connecting a suitable value resistor in parallel with the amplifier input.

Based on these considerations, the resulting oscillator circuit is as shown in Figure 6-10, where the resistor shown in dashed lines is the amplifier input loading resistor which may be necessary to reduce the crystal unit terminating level to a value of 2 to 3 R_r max.

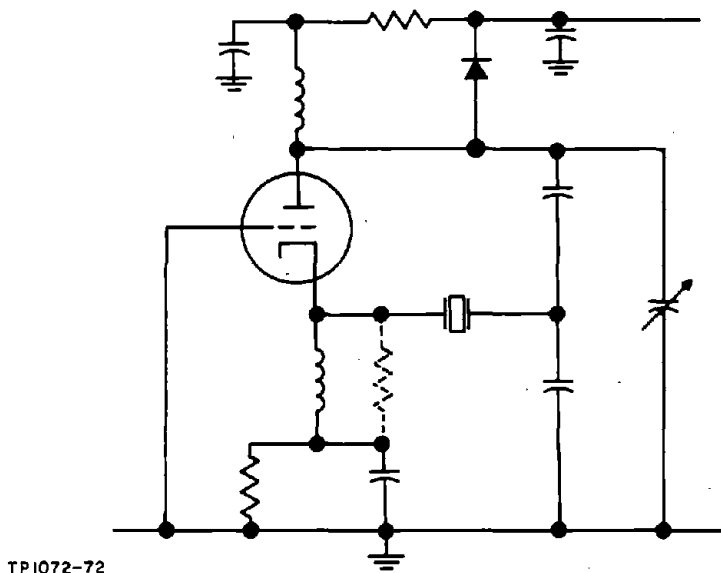


Figure 6-10. Series Oscillator Circuit, 60 to 200 MC

6-16. Loop Gain Formulae

The loop voltage gain relationships are similar to those derived in Paragraph 6-7 with the exception that the voltage ratio of the amplifier input impedance transformers is no longer a factor. The three items involved are:

- (a) The amplifier voltage gain (G_V) from the tube cathode to plate
- (b) The voltage ratio (T_{V_O}) of the amplifier output impedance transforming network
- (c) The voltage attenuation (A_{V_C}) between the crystal unit input and output terminals

These terms combine to give the loop voltage gain as:

$$G_{V_L} = G_V \cdot T_{V_O} \cdot A_{V_C} \quad (6-29)$$

The crystal unit voltage attenuation factor A_{VC} is related to the amplifier input resistance by the equation:

$$A_{VC} = \frac{R_{in}}{R_{r \max} + R_{in}} \quad (6-30)$$

Or, above 100 MC:

$$A_{VC} = \frac{R_{in}}{R_{1 \max} + R_{in}} \quad (6-31)$$

And the voltage ratio of the amplifier output transformer is related to the feedback network input resistance (neglecting losses) as:

$$R_{FB} = \frac{R_{r \max} + R_{in}}{T_{V_o}^2} \quad (6-32)$$

For a feasible design it is necessary that the feedback network input resistance should be larger than the total amplifier plate load resistance.

The amplifier measurements give values for G_V and R_{in} which in turn gives A_{VC} , leaving T_{V_o} as the only unknown in Equation (6-29). A loop voltage gain of 1.4 is usually suitable for a worst-case design, and substituting this value into Equation (6-29) gives:

$$T_{V_o} = \frac{1.4}{G_V \cdot A_{VC}} \quad (6-33)$$

6-17. DESIGN PROCEDURE FOR OSCILLATOR CIRCUITS, 60 TO 200 MC

Step 1 - Select a crystal unit type applicable at the desired operating frequency, and determine from the specification sheet the crystal unit dissipation rating PC_{MAX} and the maximum resonance resistance $R_{r \max}$ at this frequency. From 100 to 125 MC where neutralizing of the crystal unit parallel capacitance is required, the specified values of maximum resonance resistance can be regarded as equivalent to the maximum values of the motional arm resistance $R_{1 \max}$. Above 125 MC where no military specification exists for crystal units at this time, $R_{1 \max}$ can be specified to the manufacturer as 100 ohms, and the crystal dissipation rating can be considered as 2 MW.

Step 2 - Select a suitable tube type. In this frequency range the physical characteristics of the tube are equally as important as the usual electrical characteristics specified in the data sheets. In making a selection attention should be confined to those tubes having a small electrode structure and a minimum of lead length between the active parts of the structure and the connecting pins.

A multiplicity of grid connections is also indicative of high stable voltage gain at high frequencies, since when correctly used these decrease the possibility of interaction in the grid circuit between the plate and cathode signals.

With regard to the low-frequency electrical characteristics, the high μ , low R_p types appear to be most suited to this application. For although the amplifier voltage gain requirements are not as stringent as below 60 MC, because of the relaxation of the design conditions, the tendency of the amplifier to instability is significantly increased at the higher frequencies. It is normally possible to minimize the undesirable effects of this by operating at a low plate resistance level, a condition that can probably be most easily satisfied while also obtaining a relatively high voltage gain from the high μ , low R_p type triodes.

Step 3 - Select a suitable DC operating point for the tube. In order to obtain high voltage gain at the low plate load resistance levels dictated by amplifier instability considerations, it is desirable to minimize the plate resistance of the tube. The low-frequency plate resistance of the tube appears to be a useful guide in doing this, an operating point that minimizes the low frequency R_p resulting in a correspondingly low R_p at high frequencies.

The tube DC operating conditions are therefore selected by examining the low-frequency characteristic curves for a bias point giving a low plate resistance. This invariably entails low grid bias voltage and high plate current conditions. The operating point should, of course, be within the dissipation rating of the tube, and this frequently necessitates a low DC plate voltage.

Step 4 - Calculate the component values for the test amplifier circuit. The circuit will be of the form shown in Figure 6-11. The plate circuit inductor should resonate with from 10 to 20 PF, and it is desirable that the plate circuit Q should be sufficiently high that its effective parallel resistance is large compared to the highest value of plate load resistor R_T that will be used during the test. At 60 MC, the largest likely value of R_T will probably be of the order of 15 K, decreasing to perhaps 10 K at 200 MC. Inductor Q's of 200 to 400 are therefore needed to fulfill this requirement, and this tends to rule out the use of all but air-spaced coils. A large variety of handbooks give formulae for the inductance of such coils and one in particular which has been found useful, because it also gives formulae for estimating the Q of the coil as a function of its dimensions, is "The Radio Designer's Handbook" edited by F. Langford Smith.

The cathode and heater chokes should be chosen to be self-resonant at the design frequency. The effective parallel resistance of the former should preferably be over 1 K at the design frequency so that the amplifier input resistance contribution of this component will be small. It may be beneficial from the viewpoint of signal radiation via the heater leads to bifilar-wind the heater chokes.

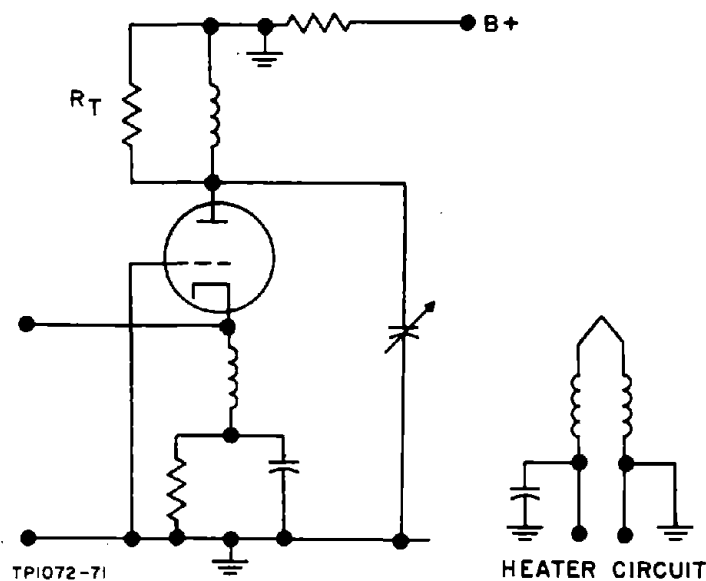


Figure 6-11. Amplifier Test Circuit

The cathode, heater, and supply voltage decoupling capacitors should be chosen to be self-resonant at the design frequency when measured with minimum lead length. A grid-dip meter is useful for determining this condition and the self-resonance frequency of the chokes.

Step 5 - Construct the amplifier test circuit. The circuit layout should follow good engineering practice with regard to minimizing lead lengths and the decoupling of supply lines. To decrease the possibility of feedback within the amplifier, the grid and cathode circuits should be spaced as far as possible from the plate circuit consistent with maintaining minimum lead lengths. The plate-to-grid and the grid-to-cathode ground return signal paths should not be common to each other. The layout should allow access to the plate and cathode for voltage measuring probes, and the impedance bridge connections should be situated immediately adjacent to the cathode. With the object of converting this breadboard to the prototype oscillator, provision should be made for installing the feedback circuit components at a later stage.

Figure 5-3 shows a circuit layout constructed on a brass chassis designed to mount directly on the ground terminal of the RX meter. This layout was for a tube with a top-cap plate connection. This is a very suitable tube configuration since it allows the plate and input circuits to be completely separated by the shield on which the tube mounts. Most tubes do not have this physical form, and it is more difficult to obtain a satisfactory circuit layout.

When the tube plate connection is brought out at the tube base, possibly the best solution is to erect a shield across the middle of the tube socket with the plate circuit on one side and the cathode and heater circuits on the other side. The plate inductor and tuning capacitor should not be installed at this stage.

Step 6 - Determine the amplifier characteristics. For the oscillator designs subsequently to be introduced, the method employed an impedance measuring bridge as the amplifier input signal source. In this instance, the bridge was a Boonton RX Meter, but other types should be equally applicable provided that the signal voltage at the bridge terminals is sufficiently low. The object is to measure the small signal amplifier characteristics, and too large a signal may modify the results obtained, particularly if signal limiting occurs. In view of the voltage gain levels expected, a bridge output signal level of 50 to 100 MV is considered most suitable. The signal output of the RX Meter may be larger than this, and the particular instrument used in these tests was modified to make the bridge output signal adjustable. This modification is described in detail in the instruction manual and consists of connecting a variable resistor in series with the bridge oscillator DC supply voltage line. The modification requires approximately one hour to introduce and is in any case a desirable improvement of the instrument, greatly enhancing its usefulness, particularly for semiconductor circuit measurements.

When using the RX Meter at signal levels of 50 to 100 MV at high frequencies, adjusting the output signal level will often cause a sufficient change of the bridge oscillator frequency to desensitize the null detector circuit unless a corresponding adjustment of the heterodyne oscillator is made. (This oscillator is required to operate at a frequency 100 KC removed from the bridge oscillator frequency to produce a 100-KC difference frequency which is then fed to the null detector circuit.)

The measurement procedure is as follows: Adjust the RX Meter to operating conditions at the design frequency. Measure and note the input impedance of the RF voltmeters that will be used to measure the amplifier input and output signal voltages. Measure the resistance of a number of carbon resistors, and select several having actual resistance values in the range of 1 to 15 K for use as amplifier loads. Values of approximately 1, 1.6, 2.5, 4, 6, 10, and 15 K are suitable. The graphs of Figure 5-2 may be useful when making a preliminary selection of resistors, although a wide variation of the ratio of AC to DC resistance can be expected for resistors of different manufacture.

Measure the effective parallel resistance of the plate inductor and tuning capacitor when tuned to resonance. Calculate the actual total amplifier load resistance for each load resistor. This consists of the parallel combination of the measured resistance of the loading resistor, the plate circuit RF voltmeter parallel resistance, and the effective parallel resistance of the plate circuit inductor and tuning capacitor.

Install the plate tuned circuit. Connect the amplifier to the RX Meter terminals, with the "live" terminal connecting to the tube cathode via a capacitor of low impedance. Short circuit the plate tuned circuit to the decoupled DC plate supply point, null the bridge while setting the bridge output voltage in the range of 50 to 100 MV, retuning the detector oscillator if necessary. Note the amplifier parallel input impedance components. Measure the signal appearing at the decoupled DC supply point and at the cathode decoupling point to ascertain that the decoupling is adequate.

Replace the short circuit with one of the load resistors and tune the plate circuit for maximum plate voltage. Null the RX Meter and retune the plate circuit for maximum signal. Null the RX Meter again if necessary. Note the amplifier parallel input impedance components and the amplifier input and output voltages. Repeat this process for the remaining load resistors.

Using a signal generator and a calibrated attenuator, measure the relative accuracies of the RF voltmeters at the scale settings employed in the test. Correct the relative readings accordingly and calculate the amplifier voltage gain for each load resistor value. Plot the voltage gain and the amplifier input resistance as a function of the total amplifier load resistance.

The amplifier will also have a parallel reactive component which will normally lie in the range of ± 5 PF. It is usually capacitive at low amplifier load levels, becoming inductive as the plate load is increased due to the feedback via the stray capacitance between the plate and cathode. Normally this reactance is large compared to the resistive component and can be neglected. At the highest frequencies, however, it may be comparable with the resistance and then appears to be a potential source of loop phase and gain errors. In practice this does not appear to be the case, however; the introduction of a resonating capacitor to cancel this component producing no significant change in oscillator performance. Based on these experimental findings, it appears justifiable to neglect the parallel reactive component of the amplifier input impedance.

A possible alternative method of amplifier characterization, but one which has not been experimentally tested, would appear to be to drive the amplifier from a signal generator via a resistance equal to $R_r \text{ max}$ or $R_l \text{ max}$, whichever is appropriate. Voltage measurements at the input to the resistor simulating $R_r \text{ max}$ or $R_l \text{ max}$ and at the cathode would then give the value of A_{V_C} , enabling R_{in} to be estimated. This would give an indication of whether or not the terminating level was suitable. Measurement of the plate voltage would then enable estimation of the net voltage gain, corresponding to $G_V \cdot A_{V_C}$, from the input of the resistor simulating the crystal unit resistance to the plate.

Step 7 - Select an amplifier operating condition for the oscillator design. The problem is one of choosing an amplifier total plate load resistance that is suitably small relative to R_{FB} and tuned circuit losses, and is also sufficiently small that the amplifier is stable, while giving an adequate loop voltage gain. Numerous alternatives exist, and it is a matter of choice on the part of the designer as to where to operate the amplifier. Perhaps the best method is to determine several suitable oscillator loop relationships and then make a selection of one of these on the basis of the amplifier voltage gain required.

The procedure is as follows: Select a value of total amplifier plate load resistance and tabulate this together with the amplifier input resistance R_{in} and voltage gain G_V . Adjust R_{in} if necessary to be not more than $3 R_{r \max}$. Calculate:

$$A_{VC} = \frac{R_{in}}{R_{r \max} + R_{in}}$$

A loop voltage gain of 1.4 is usually adequate for a worst-case design where R_r is equal to $R_{r \max}$. The required value of T_{V_0} is then:

$$T_{V_0} = \frac{1.4}{A_{VC} \cdot G_V}$$

Calculate the feedback network input resistance, neglecting losses, from:

$$R_{FB} = \frac{R_{r \max} + R_{in}}{T_{V_0}^2}$$

Calculate the resistance of the parallel combination of R_{FB} and the previously measured effective parallel resistance of the plate circuit and the voltmeter used in the plate circuit. Designating this resistance as R_n , calculate the actual oscillator load resistance from:

$$R_L = \frac{R_n \cdot R_T}{R_n - R_T}$$

If R_n is smaller than R_T the design is, of course, not feasible.

If the amplifier input resistance R_{in} is less than $R_{r \max}$, maximum crystal unit dissipation will occur for a crystal unit having a resonance resistance equal to R_{in} , assuming the plate signal voltage is reasonably constant. The allowable plate signal voltage is then:

$$V_{o \max} = \frac{2 \sqrt{P_{C \max} \cdot R_{in}}}{T_{V_0}}$$

This is the permissible voltage when the crystal unit in circuit has a resonance resistance equal to R_{in} . When a worst-case crystal unit having a resonance resistance equal to $R_{r \max}$ is in circuit, the loop gain and hence the plate signal voltage will be smaller.

If the amplifier input resistance is larger than $R_{r \max}$, maximum crystal unit dissipation will occur for a crystal unit having a resonance resistance equal to $R_{r \max}$, assuming the plate signal voltage does not increase too greatly as the loop gain increases. The allowable plate signal voltage is then:

$$V_o \max = \left(1 + \frac{R_{in}}{R_{r \max}} \right) \frac{\sqrt{P_{C \max} \cdot R_{r \max}}}{T_{V_o}}$$

The relationship between the allowable plate signal voltage and the limiting diode reverse-bias DC voltage does not appear to be simple. Judging by experimental results, the required diode DC bias voltage will be somewhere in the range between the RMS and the peak plate signal amplitudes. Selecting a diode DC bias voltage equal to the RMS signal amplitude should result in plate signal limiting at a level below the permissible amplitude previously calculated. Experimental adjustments may then be made if necessary.

The parallel impedance components of the diode selected should be measured at the calculated DC reverse-bias voltage at the design frequency. The circuit of Figure 6-12 is suitable for this measurement, provided that the resistor R does not introduce appreciable loading. This can be ascertained by measuring the circuit impedance without the diode. At the higher frequencies due to the low resistance of even high-value carbon resistors at these frequencies, it may be necessary to calculate the diode resistance from the measurements obtained with the diode in and out of circuit. If the diode parallel resistance value obtained is not negligibly large compared to the previously derived value of oscillator load, R_L will need to be increased accordingly to ensure adequate loop gain.

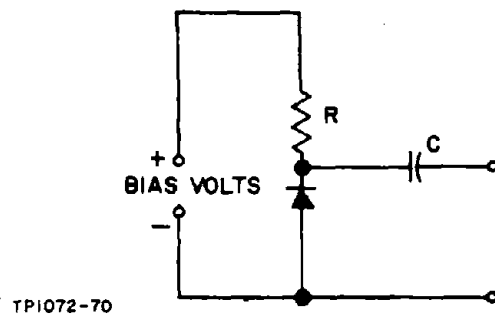


Figure 6-12. Limiter Diode Test Circuit

Step 8 - Calculate the impedance transformer component values for the value of T_{V_0} obtained. The capacitive divider appears to be the most suitable network to use for this purpose. The design relationships for this network are:

$$T_{V_0} = \frac{C_1}{C_1 + C_2}$$

and

$$X_{(C_1 + C_2)} \leq \frac{1}{3} (R_{r \text{ max}} + R_{in})$$

This latter condition is imposed by phase angle considerations as discussed in Section 4. Convert the amplifier circuit to the oscillator circuit, introducing the amplifier input loading resistor if applicable. Various preliminary experimental tests of the oscillator circuit similar to those described in Paragraph 6-8, Step 6 may be found useful.

The prevention of excessive regeneration within the amplifier is one of the major design factors at the higher frequencies. In its mildest form amplifier regeneration can be detected as a peculiarity of the oscillator tuning. As the plate circuit is tuned through the region where the maximum plate signal voltage occurs, a dissymmetry of the signal voltage as a function of tuning will be noted. In severe cases the action is quite abrupt, oscillation ceasing immediately after tuning through peak output. Furthermore, when retuning to restart oscillation, it is necessary to tune past the point of peak output before oscillation recommences.

The severity of this effect is an indication of the relative stability of the amplifier, and in a satisfactory oscillator it should be possible to tune smoothly through the region of peak plate signal voltage. If this is not the case, the circuit should be redesigned using a lower value of amplifier total resistance. Another possibility, which has not been tried with tube amplifiers but appeared to work satisfactorily with transistor amplifiers, is to introduce partial neutralizing in the circuit by means of an inductor across the crystal socket. The regenerative effect appears to be mostly due to feedback via the stray capacitance between the plate and the cathode. An inductor across the crystal socket will cause a signal current to flow from the plate to the cathode approximately in phase opposition to that due to the stray capacitance, reducing the regeneration. Above 100 MC where an inductor is normally used to cancel the crystal unit parallel capacitance, this simply entails decreasing the value of this inductor below that required for C_0 cancellation.

6-18. DESIGN EXAMPLES AND EVALUATION DATA, 60 TO 200 MC

Four designs and evaluations were carried out in this frequency range. Two of these, however, were not very satisfactory because of the amount of

experimental adjustment required to obtain a satisfactory oscillator. The unsatisfactory designs employed the type 5718A subminiature tube which has a typical low-frequency amplification factor of 25 and a plate resistance of 4 K. The design frequencies were 100 and 200 MC.

The major problem encountered in these designs was that of suppressing uncontrolled oscillation which tended to occur when the plate circuit was mistuned. Numerous adjustments of the plate and grid circuits were required before these effects were finally eradicated. In the 200 MC design this entailed operating at a low amplifier voltage gain and with a 200-ohm loading resistor at the amplifier input before adequate amplifier stability was obtained. In the 100 MC design a higher amplifier voltage gain was used and the effect was more severe.

It appears that, although the electrode structure of the 5718A tube is physically small, the connecting lead lengths within the tube and the close proximity of these leads are sufficient to make the tube unsuitable for crystal oscillator design at high frequencies. These designs are included for completeness and to indicate the problems that may be met when designing at these frequencies and are not recommended for duplication.

The other two designs used the 8058 nuvistor triode. This tube is similar in characteristics to the 6CW4 but has a completely different physical form, having a top cap plate connection and a grid grounding connection encircling the tube body. The results obtained using this tube were excellent, perhaps because of the good shielding between input and output circuits possible with a tube of this physical form. This is a relatively costly tube and it may be possible to achieve similar results with the 6CW4, although since this latter tube is single-ended, the shielding between input and output circuits will not be as good.

6-19. 100-MC, 5718A Series Oscillator

Crystal Unit Characteristics (CR-56A/U)

$$P_{\text{CMAX}} = 2 \text{ MW}, R_r \text{ max} = 60 \text{ ohms}$$

The tube DC operating point was selected at

$$E_p = 100 \text{ VDC}, I_p = 10 \text{ MA}, V_G = -1 \text{ VDC}.$$

The amplifier test circuit was similar to that shown in Figure 6-13, excluding the feedback components and the physical layout as shown in Figure 6-14, the chassis mounting directly on the RX Meter ground terminals with the line terminal protruding through the chassis adjacent to the cathode connection.

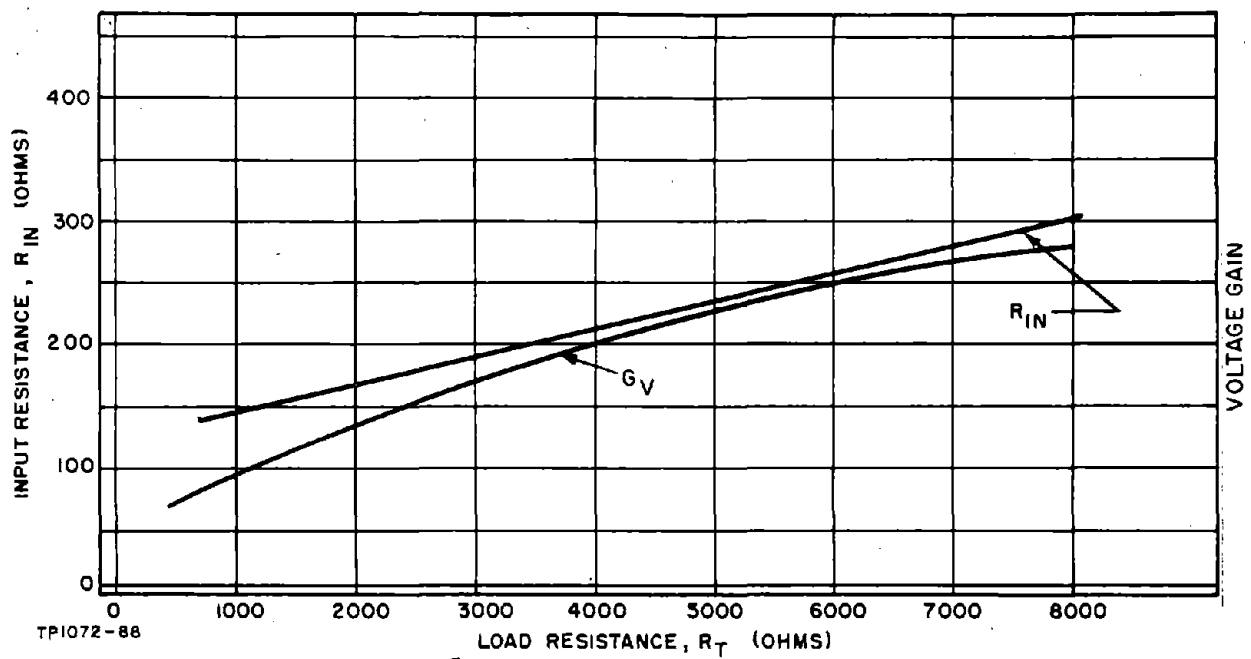


Figure 6-15. Input Resistance and Power Gain Versus Load Resistance, 5718A Tube at 100 MC

The voltage measuring probe and tuned circuit parallel resistances were 50 K and 25 K, giving $R_L = 4.9$ K. Using a capacitive divider feedback network, the relationships are:

$$\frac{C_1}{C_1 + C_2} = 0.13 \quad X_{(C_1 + C_2)} \leq 83 \text{ ohms}$$

If C_2 is 20 PF, $C_1 = 3$ PF, then $X_{(C_1 + C_2)} = 70$ ohms. The allowable plate signal voltage is 11 VRMS. The evaluation data for this oscillator are presented in Figure 6-16 and Table 6-3.

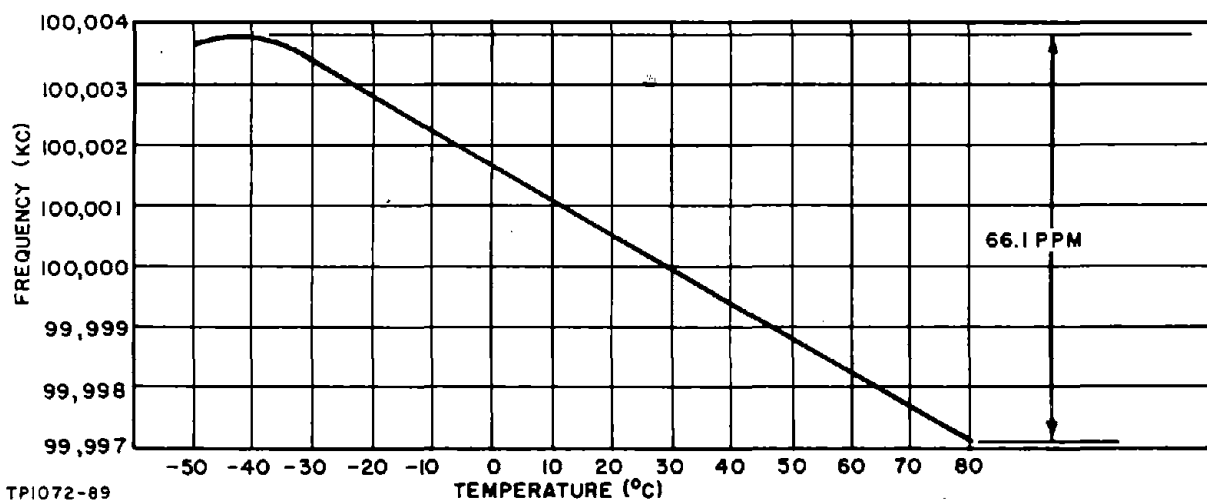


Figure 6-16. Frequency Versus Temperature Characteristics, 100-MC Tube Oscillator

TABLE 6-3. DESIGN EVALUATION DATA, 100-MC TUBE OSCILLATOR

Nominal $V_0 = 8$ V; Nominal Oscillator Frequency = 100.0000 MCCrystal Unit: CR-56A/U, $f_r = 99.9998$ MC, $R_r = 29$ ohms

EFFECT OF	CHANGE	TEST CONDITIONS
$\pm 10\%$ Change in B+ on Oscillator Frequency	± 1.4 PPM	$E_f = 6.3V$, $R_L = 15K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in B+ on Output Voltage	$\Delta V_0 = \pm 12\%$	$E_f = 6.3V$, $R_L = 15K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Oscillator Frequency	± 3.2 PPM	$E_{bb} = 120V$, $R_L = 15K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_0 = \pm 1\%$	$E_{bb} = 120V$, $R_L = 15K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in Filament Supply Voltage on Oscillator Frequency	± 1.2 PPM	$E_{bb} = 120V$, $R_L = 15K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in Filament Supply Voltage on Output Voltage	$\Delta V_0 = \pm 4\%$	$E_{bb} = 120V$, $R_L = 15K$, $T_A \approx 25^\circ C$
$-50^\circ C$ to $+80^\circ C$ Variation of T_A on Oscillator Frequency	± 33 PPM	$E_{bb} = 120V$, $E_f = 6.3V$, $R_L = 15K$
$-50^\circ C$ to $+80^\circ C$ Variation of T_A on Output Voltage	$\Delta V_0 = \pm 6\%$	$E_{bb} = 120V$, $E_f = 6.3V$, $R_L = 15K$

6-20. 150-MC, 8058 Series Oscillator

Crystal Unit Characteristics
Similar to CR-56A/U

$$\text{Assumed } R_{r \max} = 100 \text{ ohms, } P_{C \max} = 2 \text{ MW}$$

The tube DC operating point was selected at

$$E_p = 80 \text{ VDC, } I_p = 10 \text{ MA, } V_G = 0.$$

The amplifier test circuit was similar to that shown in Figure 6-17 excluding the feedback network, and the measured data are plotted in Figure 6-18.

A working point was selected at $R_T = 2.7 \text{ K}$,

$$G_V = 36, R_{in} = 85 \text{ ohms.}$$

Then

$$A_{V_C} = 0.46 \text{ and } T_{V_O} = 0.085,$$

giving $R_{FB} = 25 \text{ K}$. The voltage measuring probe parallel resistance was 50 K and the tuned circuit parallel resistance was 23 K , giving $R_L = 3.7 \text{ K}$.

Using a capacitive divider feedback network, the relationships are:

$$\frac{C_1}{C_1 + C_2} = 0.085 \text{ and } X_{(C_1 + C_2)} \leq 62 \text{ ohms}$$

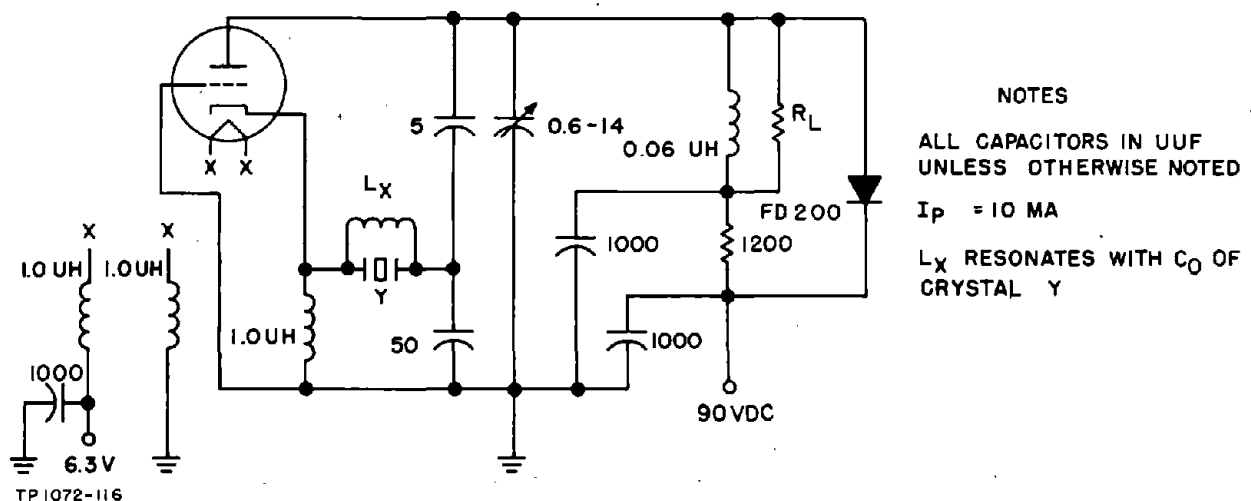


Figure 6-17. 150-MC Series Oscillator Circuit

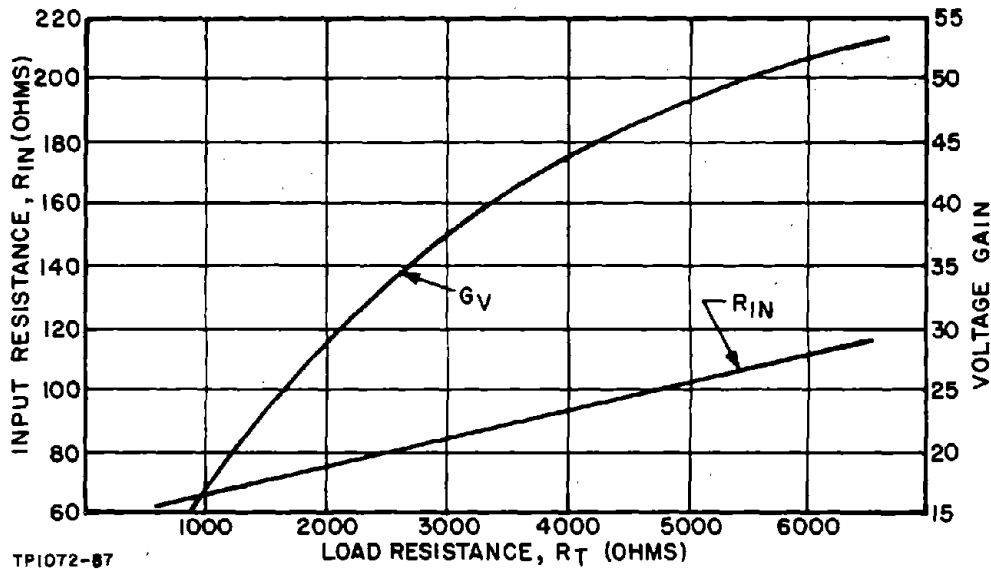


Figure 6-18. Input Resistance and Voltage Gain Vs. Load Resistance, 8058 Nuvistor at 150 MC

If C_2 is 50 PF, $C_1 = 4$ PF, then $X_{(C_1 + C_2)} = 20$ ohms. The allowable plate signal voltage is 9 VRMS. A limiter diode reverse bias of 12 V was found to give a suitable signal limiting action.

The only other experimental adjustment required to obtain satisfactory oscillation under all test conditions was to increase C_1 to 5 PF. The evaluation data for this oscillator are presented in Figure 6-19 and Table 6-4.

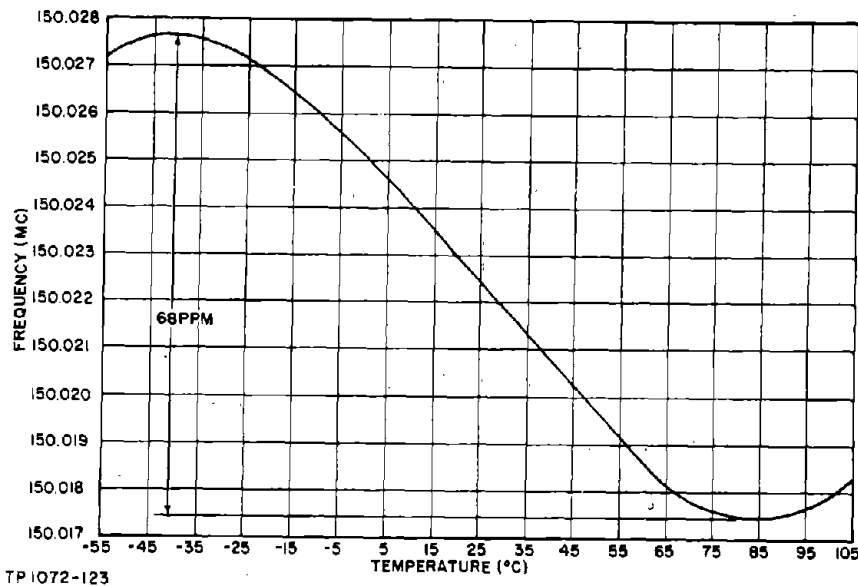


Figure 6-19. Frequency Vs. Temperature, 150-MC Tube Oscillator (8058)

TABLE 6-4. DESIGN EVALUATION DATA, 150-MC TUBE OSCILLATOR

Nominal $V_o = 9$ V; Nominal Oscillator Frequency = 150.0211 MCCrystal Unit: $f_r = 150.0220$ MC, $R_r = 47$ ohms

EFFECT OF	CHANGE	TEST CONDITIONS
+15%, -20% Change in B+ on Oscillator Frequency	± 2 PPM	$R_L = 5.1K$, $E_f = 6.3V$, $T_A \approx 25^\circ C$
+15%, -20% Change in B+ on Output Voltage	$\Delta V_o = \pm 22\%$	$R_L = 5.1K$, $E_f = 6.3V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Oscillator Frequency	± 1.4 PPM	$E_{bb} = 90V$, $E_f = 6.3V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_o = \pm 1\%$	$E_{bb} = 90V$, $E_f = 6.3V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in Filament Voltage on Oscillator Frequency	± 2.6 PPM	$E_{bb} = 90V$, $R_L = 5.1K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in Filament Voltage on Output Voltage	$\Delta V_o = \pm 26\%$ (16% for 5% ΔE_f)	$E_{bb} = 90V$, $R_L = 5.1K$, $T_A \approx 25^\circ C$
-50°C to +80°C Change in T_A on Oscillator Frequency	± 36 PPM	$E_{bb} = 90V$, $R_L = 5.1K$, $E_f = 6.3V$
-50°C to +80°C Change in T_A on Output Voltage	$\Delta V_o = \pm 2\%$	$E_{bb} = 90V$, $R_L = 5.1K$, $E_f = 6.3V$

6-21. 200-MC, 8058 Series Oscillator

Crystal Unit Characteristics Similar to CR-56A/U

Assumed $R_{r\max} = 100$ ohms, $P_{C\max} = 2$ MW

The tube DC operating point was selected at:

$$E_p = 80 \text{ VDC}, I_p = 10 \text{ MA}, V_G = 0.$$

The amplifier test circuit was similar to that shown in Figure 6-20, excluding the feedback circuit, and the measured data are plotted in Figure 6-21.

A working point was selected at $R'_T = 2.5$ K, $G_V = 45$, and $R_{in} = 75$ ohms, where R'_T includes the plate circuit losses. Then,

$$A_{VC} = 0.43 \text{ and } T_{V_0} = 0.073,$$

giving

$$R_{FB} = 33 \text{ K}.$$

The voltmeter probe resistance was 8 K and, since the tuned circuit losses are already accounted for in R'_T , the oscillator load is 4.1 K. Using a capacitive divider feedback network, the relationships are:

$$\frac{C_1}{C_1 + C_2} = 0.073 \quad X_{(C_1 + C_2)} \leq 58 \text{ ohms}$$

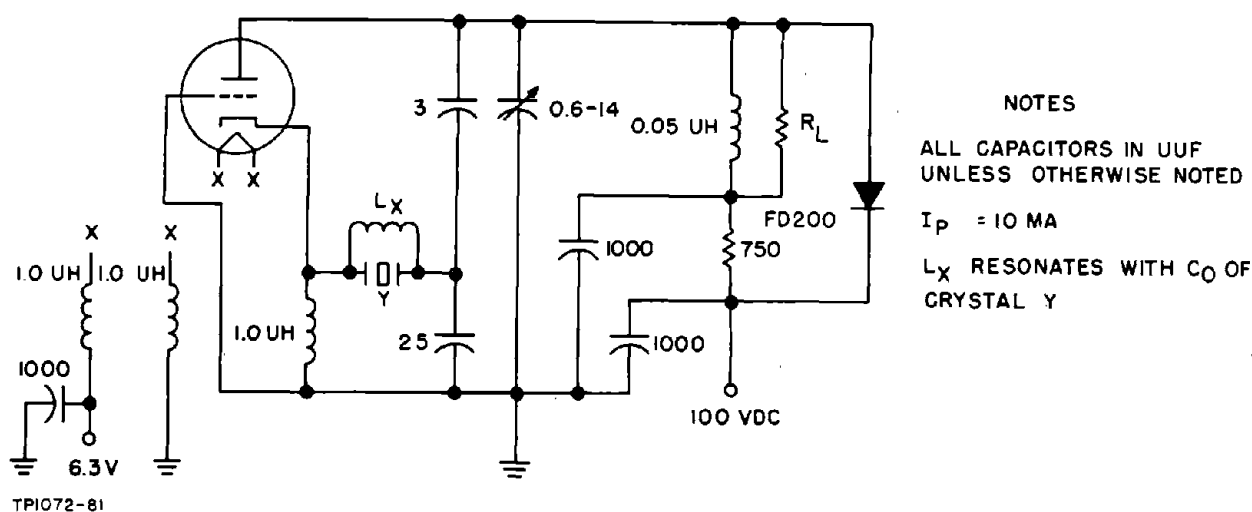


Figure 6-20. 200-MC Series Oscillator Circuit

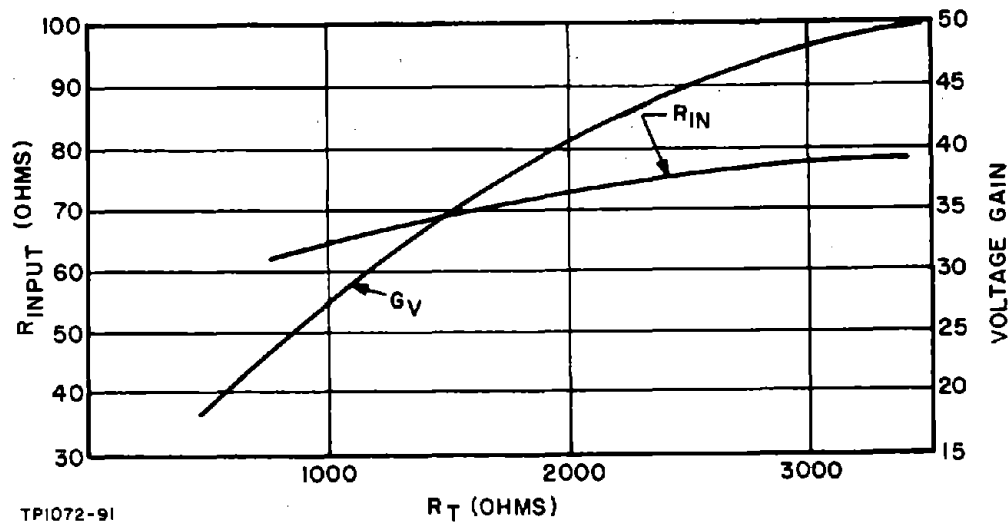


Figure 6-21. Input Resistance and Voltage Gain Versus Total Load Resistance (minus coil losses), 8058 Nuvistor at 200 MC

If C_2 is 25 PF, $C_1 = 1.8$ PF, then $X(C_1 + C_2) = 30$ ohms. The allowable plate signal voltage is then 10 VRMS. Using a limiter diode reverse bias of 7.5 VDC, limiting was obtained at a plate signal voltage of 6 VRMS.

To obtain satisfactory oscillation under all test conditions, it was necessary to increase C_1 to 3 PF. The evaluation data for this oscillator are presented in Figure 6-22 and Table 6-5.

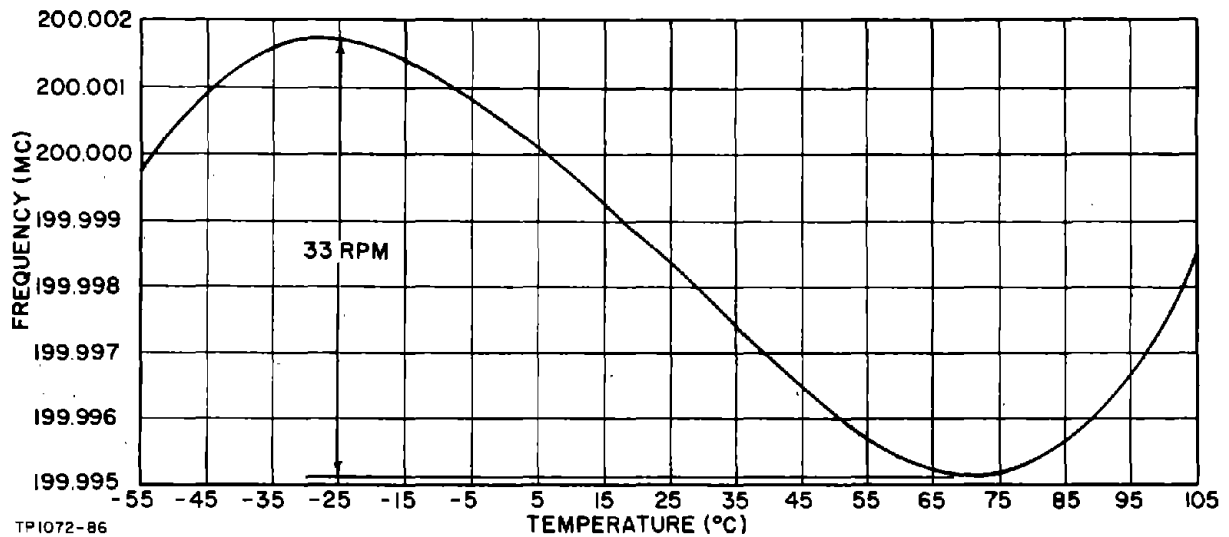


Figure 6-22. Frequency Vs. Temperature, 200 MC Tube Oscillator (8058)

TABLE 6-5. DESIGN EVALUATION DATA, 200-MC TUBE OSCILLATOR (8058)

Nominal $V_0 = 5.8$ V; Oscillator Frequency = 199.9985 MC

Crystal Unit: $f_r = 199.9990$ MC, $R_r = 88$ ohms

EFFECT OF	CHANGE	TEST CONDITIONS
+15%, -20% Change of $B+$ on Oscillator Frequency	± 2 PPM	$E_f = 6.3$ V, $R_L = 10$ K, $T_A \approx 25^\circ\text{C}$
+15%, -20% Change of $B+$ on Output Voltage	$\Delta V_0 = \pm 23\%$	$E_f = 6.3$ V, $R_L = 10$ K, $T_A \approx 25^\circ\text{C}$
$\pm 10\%$ Change of R_L on Oscillator Frequency	± 2.8 PPM	$E_f = 6.3$ V, $E_{bb} = 100$ V, $T_A \approx 25^\circ\text{C}$
$\pm 10\%$ Change of R_L on Output Voltage	$\Delta V_0 < 1\%$	$E_f = 6.3$ V, $E_{bb} = 100$ V, $T_A \approx 25^\circ\text{C}$
$\pm 10\%$ Change of E_f on Oscillator Frequency	± 2.5 PPM	$R_L = 10$ K, $E_{bb} = 100$ V, $T_A \approx 25^\circ\text{C}$
$\pm 10\%$ Change of E_f on Output Voltage	$\Delta V_0 = \pm 22\%$	$R_L = 10$ K, $E_{bb} = 100$ V, $T_A \approx 25^\circ\text{C}$
-50°C to +70°C Change of T_A on Oscillator Frequency	± 18 PPM	$R_L = 10$ K, $E_{bb} = 100$ V, $E_f = 6.3$ V
-50°C to +70°C Change of T_A on Output Voltage	$\Delta V_0 = \pm 6\%$	$R_L = 10$ K, $E_{bb} = 100$ V, $E_f = 6.3$ V

6-22. 200-MC, 5718A Series Oscillator

Crystal Unit Characteristics

Similar to CR-56A/U

$$\text{Assumed } R_{r \max} = 100 \text{ ohms}$$

$$P_{\text{CMAX}} = 2 \text{ MW}$$

The tube DC operating point was selected at

$$E_p = 100 \text{ VDC}, I_p = 7.5 \text{ MA}, V_G = 1.5 \text{ VDC}$$

The amplifier test circuit was similar to that shown in Figure 6-23, excluding the feedback network, and the measured data are plotted in Figure 6-24.

A working point was selected at

$$R_T = 1.6 \text{ K}, G_V = 11, R_{in} = 120 \text{ ohms}$$

Then:

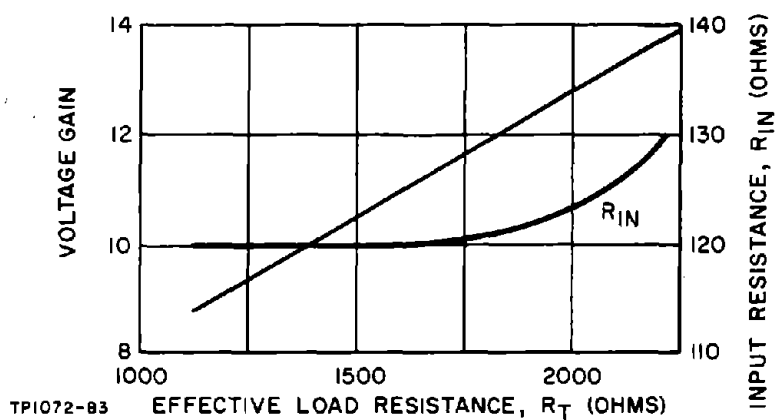
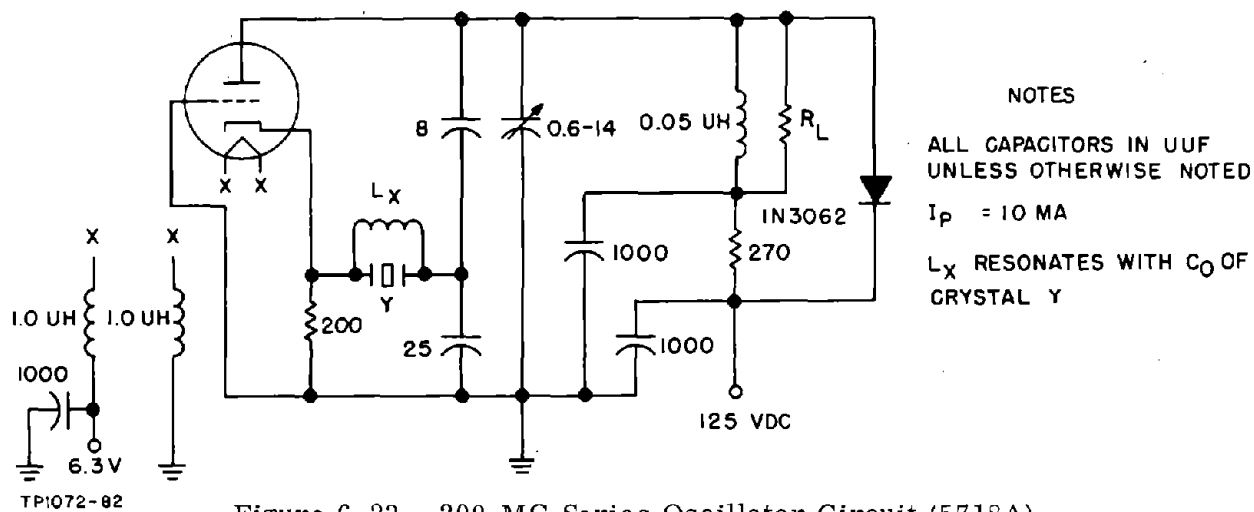
$$A_{V_C} = 0.55 \text{ and } T_{V_0} = 0.25,$$

giving

$$R_{FB} = 3.5 \text{ K.}$$

The voltage measuring probe parallel resistance was 8 K, and the tuned circuit effective parallel resistance was 40 K, giving:

$$R_L = 5.3 \text{ K.}$$



Using a capacitive divider feedback network, the relationships are:

If $C_2 = 25 \text{ PF}$, $C_1 = 8.2 \text{ PF}$, then

The allowable plate signal voltage is 4 VRMS. Using a limiter diode reverse bias of 2 V, limiting was obtained at a plate signal voltage of 2.7 VRMS. The evaluation data for this oscillator are presented in Figure 6-25 and Table 6-6.

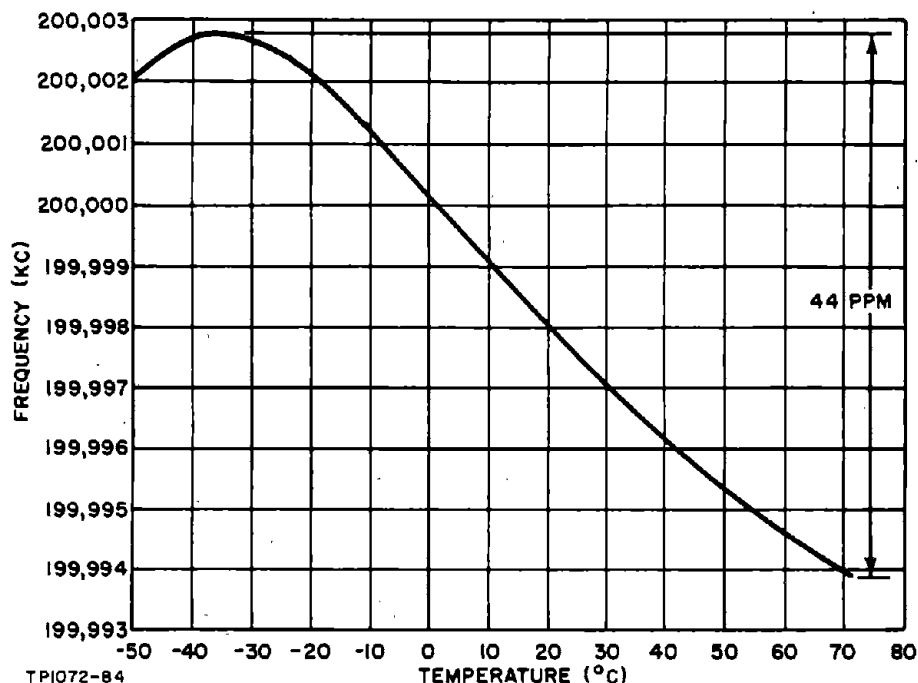


Figure 6-25. Frequency Versus Temperature, 5718A Tube at 200 MC

6-23. DESIGN OF SERIES OSCILLATORS, 1 KC TO 100 KC

Below 90 KC the resonance resistance of crystal units is so large that the grounded grid amplifier circuit is no longer suitable because of the excessive attenuation that would occur between the crystal unit input and the amplifier input terminals. A more suitable oscillator configuration then consists of a grounded-cathode amplifier and a phase-inverting feedback network as shown in Figure 6-26. In this circuit the grid leak resistor R_g is usually the major part of the crystal unit output terminating resistance and can be selected to provide a suitable terminating level without incurring an excessive attenuation.

The major disadvantage of this circuit is the large tuned circuit component values required at the lower frequencies which may make the alternative circuits presented later more desirable. This does not apply at the higher frequencies, and this circuit may perhaps be used advantageously up to 500 KC.

TABLE 6-6. DESIGN EVALUATION DATA, 200-MC TUBE OSCILLATOR (5718A)

Nominal $V_o = 2.7$ V; Operating Frequency = 199.998 MC

Crystal Unit: $f_r = 199.9990$ MC, $R_r = 88$ ohms

EFFECT OF	CHANGE	TEST CONDITIONS
±10% Change in B+ on Oscillator Frequency	±1 PPM	$E_f = 6.3V$, $R_L = 13K$, $T_A \approx 25^\circ C$
±10% Change in B+ on Output Voltage	$\Delta V_o = \pm 11\%$	$E_f = 6.3V$, $R_L = 13K$, $T_A \approx 25^\circ C$
±10% Change in R_L on Oscillator Frequency	±2.5 PPM	$E_f = 6.3V$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
±10% Change in R_L on Output Voltage	$\Delta V_o = \pm 2\%$	$E_f = 6.3V$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
±10% Change in Filament Voltage on Oscillator Frequency	±2.5 PPM	$E_{bb} = 125V$, $R_L = 13K$, $T_A \approx 25^\circ C$
±10% Change in Filament Voltage on Output Voltage	$\Delta V_o = \pm 2\%$	$E_{bb} = 125V$, $R_L = 13K$, $T_A \approx 25^\circ C$
-50°C to +70°C Change in T_A on Oscillator Frequency	±22 PPM	$E_{bb} = 125V$, $R_L = 13K$, $E_f = 6.3V$
-50°C to +70°C Change in T_A on Output Voltage	$\Delta V_o = \pm 11\%$	$E_{bb} = 125V$, $R_L = 13K$, $E_f = 6.3V$

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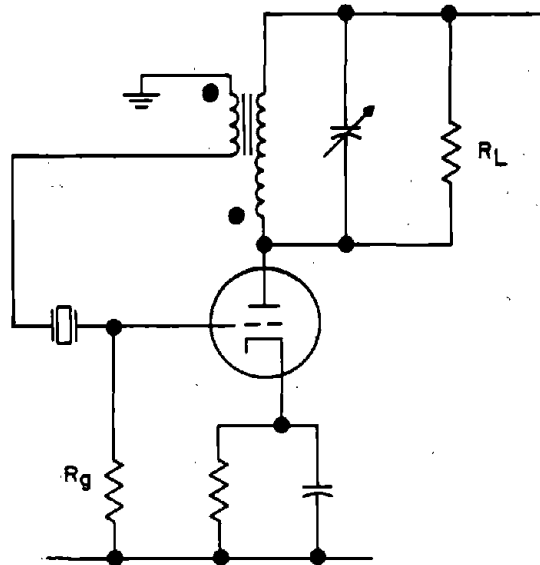


Figure 6-26. Oscillator Circuit For Use Below 90 KC

6-24. Crystal Unit Characteristics

The only military type series resonance crystal unit applicable in this frequency range is the CR-50A/U covering the range from 16 to 100 KC. The major characteristics of this crystal unit are:

Frequency Range: 16 to 100 KC, inclusive

Overall Frequency Tolerance: ± 0.012 percent

Operating Temperature Range: -40 to $+70^{\circ}\text{C}$

Rated Dissipation: 0.1 MW

Maximum Resonance Resistance:	{	16 to 30 KC:	100 K
		30+ to 50 KC:	90 K
		50+ to 70 KC:	80 K
		70+ to 90 KC:	70 K
		90+ to 100 KC:	60 K

Crystal Holder: HC-13/U

There are no military type crystal units applicable at frequencies below 16 KC, but crystal units are manufactured for operation at frequencies from below 1 KC to 16 KC. Typical manufacturer's data for these give the following major characteristics:

Overall Frequency Tolerance:	±0.015 percent
Operating Temperature Range:	-40 to +70°C
Rated Dissipation:	Values ranging from 10 to 100 UW
Maximum Resonance Resistance:	Values from 100 to 200 K
Physical Configuration:	The resonator in these units is in the form of a relatively long quartz bar, and usually the holder is a cylindrical glass bulb 3 to 4 inches in length mounted on an octal tube base, although at the higher frequencies crystal holders of the HC-13/U type may be available.

As discussed in detail in Paragraph 6-6, the permissible drive voltage V_{\max} applied at the crystal unit input terminal depends on the relative values of the crystal unit resonance resistance R_r and the amplifier input resistance R_{in} . When R_{in} is less than or equal to $R_{r \max}$, the relationship is:

$$V_{\max} = 2 \sqrt{P_{\text{CMAX}} \cdot R_{in}} \quad (6-34)$$

Denoting the relationship between R_{in} and $R_{r \max}$ as

$$R_{in} = k R_{r \max} \quad (6-35)$$

where k is less than 1, enables V_{\max} to be calculated as a function of k . For the given crystal characteristics, these calculations result in the values contained in Table 6-7. The double values of V_{\max} given for the frequency range of 1 to 16 KC take into account the spread in crystal dissipation rating quoted by manufacturers. It is thought probable that 10 UW is the more desirable rating, and this will be subsequently employed.

Relating the values of V_{\max} in Table 6-7 to the plate signal levels at which amplifier self-limiting can be readily obtained shows that the voltage ratio of the feedback transformer need not be very large. Amplifier voltage gain requirements are therefore not too demanding.

TABLE 6-7. CRYSTAL CHARACTERISTICS, 1 TO 100 KC

Frequency (KC)	R_r max (Kilohms)	$P_{C\text{MAX}}$ (UW)	V_{max} (RMS)		
			$k = 0.33$	$k = 0.5$	$k = 1$
1 to 16 KC	200	100	5.2	6.4	9
		10	1.6	2	2.8
16 to 30 KC	100	100	3.6	4.5	6.3
30+ to 50 KC	90	100	3.5	4.3	6
50+ to 70 KC	80	100	3.2	4.0	5.6
70+ to 90 KC	70	100	3.0	3.8	5.3
90+ to 100 KC	60	100	2.8	3.5	4.9

6-25. Amplifier Characteristics

The voltage gain of a grounded-cathode triode amplifier, when the plate circuit is tuned to resonance or when the plate circuit reactance is negligibly large compared to the plate load resistance, is:

$$G_V = \frac{\mu R_T}{R_T + R_p} \quad (6-36)$$

The amplifier input resistance consists of the grid-leak resistor R_g and the grid-cathode capacitance C_{gk} in parallel with two impedance components due to feedback via the grid-plate capacitance C_{pg} . This subject is discussed in detail in Section 9 where it is shown that, provided the phase shift between the grid and plate is small, these components are:

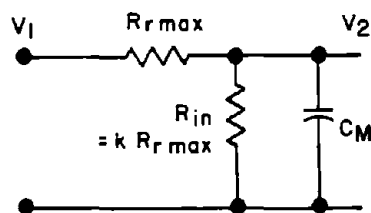
$$C_M = (G_V + 1) C_{pg} \quad (6-37)$$

$$R_M = X_{C_M} / \phi \quad (6-38)$$

where ϕ is the phase angle of the plate signal relative to the grid signal in radians. The amplifier input impedance therefore consists of R_g , R_M , C_M , and C_{gk} all in parallel.

Frequently, the reactance of C_M and R_M are negligibly large compared to R_g and have little influence on the amplifier input impedance. In some cases, however, an appreciable phase shift can occur due to C_M . Figure 6-27 illustrates the effect at the crystal unit resonance frequency. The phase angle of V_2 relative to V_1 is:

$$\phi = -\tan^{-1} \frac{k}{1+k} \cdot \frac{R_{r \max}}{X_{C_M}} \quad (6-39)$$



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Figure 6-27. Effect of C_M on Loop Phase Angle

It is apparent that for the likely range of k values an undesirably large phase lag of V_2 relative to V_1 can occur if the reactance of C_M approaches $R_{r \max}$ in value. A phase lag of up to 10 degrees will not upset the circuit performance unduly, and this is considered a suitable maximum allowable value. Substituting 10 degrees into Equation (6-39) then gives as a limiting condition:

$$\frac{k}{1+k} \cdot \frac{R_{r \max}}{X_{C_M}} \leq 0.18 \quad (6-40)$$

If this relationship is satisfied, the effects of X_{C_M} can be neglected. If not, it will be necessary to provide a correction. This can be conveniently introduced using a neutralizing capacitor. The object is to provide a current flowing to the grid point equal in magnitude and opposite in phase to that flowing through C_{pg} . Since the output signal of the impedance transformer is in phase opposition to the plate signal voltage, a capacitor connected from this point to the grid will provide a current of the required phase. To provide the correct current magnitude requires the capacitance to be related to C_{pg} and the voltage ratio of the impedance transformer T_{V_0} by the expression:

$$C_n = C_{pg} / T_{V_0} \quad (6-41)$$

It is not necessary to achieve complete neutralization, and the value of C_n is not critical. The nearest 5 percent standard value to that calculated should suffice.

Provided that the plate phase lag is not more than 10 degrees, values of X_{CM} satisfying Equation (6-40) will result in values of R_M sufficiently large that its effect on the amplifier input resistance can be neglected. And when X_{CM} does not satisfy Equation (6-40) and neutralizing is required, R_M will not, of course, be present. Under normal circumstances R_M can therefore be neglected and R_{in} is then equal to R_g .

The amplifier output impedance insofar as the feedback network is concerned consists of the parallel combination of R_p , the oscillator load R_L , and the capacitance from the plate to all other electrodes.

6-26. Loop Gain Relationships

For the oscillator circuit of Figure 6-26, the loop gain relationships can be conveniently divided into three factors. These are:

- (a) The amplifier voltage gain G_V from the grid to the plate circuit
- (b) The attenuation A_{VC} from the crystal unit input terminal to the tube grid
- (c) The voltage ratio T_{V_0} of the impedance transforming network between the tube plate and the crystal unit input terminal.

The oscillator loop voltage gain is then:

$$G_{VL} = G_V \cdot A_{VC} \cdot T_{V_0} \quad (6-41)$$

where:

$$A_{VC} = \frac{R_{in}}{R_{r \max} + R_{in}} \quad (R_{in} = R_g) \quad (6-42)$$

T_{V_0} is a design variable which must be large enough to provide adequate loop gain but must also be sufficiently small as to prevent crystal unit overdrive. That portion of the feedback network input resistance due to the transformation of the series combination of the amplifier input resistance and the crystal resonance resistance is related to T_{V_0} as:

$$R_{FB} = \frac{R_{r \max} + R_{in}}{T_{V_0}^2} \quad (6-43)$$

A loop voltage gain of 1.4 is usually adequate for a worst-case design and substituting this value into Equation (6-41) gives:

$$T_{V_0} = \frac{1.4}{G_V \cdot A_{V_C}} \quad (6-43)$$

The permissible plate signal voltage $V_0 \text{ max}$ is related to V_{max} as:

$$V_0 \text{ max} = V_{\text{max}} / T_{V_0} \quad (6-44)$$

The oscillator plate load resistance R_L is related to R_T and R_{FB} as:

$$R_L = \frac{R_T \cdot R_{FB}}{R_{FB} - R_T} \quad (6-45)$$

The terminating resistance level at the input side of the crystal unit is $T_{V_0}^2 \cdot R_0$, where R_0 is equal to R_p and R_L in parallel.

6-27. Impedance Transforming Network

The impedance transforming network is required to give a 180-degree phase shift, and either the π network or a phase inverting inductive transformer is suitable, although of the two, the inductive transformer is perhaps to be preferred since it can also be used as a parallel feed path for the tube plate current. This is particularly advantageous if the available plate supply voltage is low.

The secondary load impedance of the transformer consists of $R_r \text{ max}$ and R_{in} in series and therefore has values of from not less than 60 K to more than 200 K. In view of the high level of the secondary load, the most suitable inductive transformer operating condition is that obtained when the secondary winding inductance is small compared to the secondary load resistance. The design equations for this type of operation are:

$$T_{V_0} = \frac{V_2}{V_1} = -k \sqrt{\frac{L_2}{L_1}} \angle 90^\circ - \tan^{-1} \frac{\omega L_2}{r_s} - \tan^{-1} \frac{r_s}{k^2 \omega L_2} \quad (6-46)$$

$$\frac{\omega L_2}{r_s} \leq \frac{1}{3}, \text{ where } r_s = R_r \text{ max} + R_g. \quad (6-47)$$

The inductance of the primary winding is determined from consideration of the plate circuit loaded Q . The plate circuit Q should not be too high, otherwise temperature changes may cause large variations in the plate tuned circuit

phase angle, in turn increasing the oscillator frequency tolerance. Because of this, a plate circuit loaded Q of less than 15 is considered desirable. This determines the minimum value that the primary inductance may have relative to the amplifier output resistance. The plate circuit loaded Q , assuming the coil Q is large, is:

$$Q_L = \frac{R_T \cdot R_p}{(R_T + R_p)} \cdot \frac{1}{\omega L_1} \quad (6-48)$$

For Q_L equal to or less than 15, this gives:

$$\omega L_1 \geq \frac{R_T \cdot R_p}{15 (R_T + R_p)} \quad (6-49)$$

The effective parallel resistance R_{LP} of the transformer reflected into the plate circuit forms part of the calculated oscillator load R_L . The relationship is:

$$R_L = \frac{R'_L \cdot R_{LP}}{R'_L + R_{LP}} \quad (6-50)$$

where R'_L is the actual oscillator load reflected into the plate circuit. Depending on the external oscillator load relative to the calculated R_L and the Q of the transformer windings, the transformer loss resistance may necessitate a larger value of primary inductance than that given by Equation (6-48).

Plate circuit tuning may present a difficulty at the lowest frequencies because of the large value of tuning capacitance required. One possibility is to adjust the transformer to resonance at the design frequency before installation in the circuit. Another alternative is to wind the transformer on a tunable pot core.

6-28. DESIGN EXAMPLES

The design process consists of obtaining a suitable loop gain while satisfying the limiting condition on TV_O and k . The design procedure closely follows that given previously for design in the 90 KC to 60 MC range. The following examples illustrate the approach.

6-29. 16 to 100 KC Series Oscillator

This example is presented for the two extreme frequencies of the range. The circuit value changes required for intermediate frequencies should be evident.

Crystal characteristics:

	<u>16 KC</u>	<u>100 KC</u>
$R_r \text{ max}$	100 K	60 K
$P_{C\text{MAX}}$	100 UW	100 UW

For $k = 0.5$ ($R_{in} = 0.5 R_r \text{ max}$), $A_{V_C} = \frac{1}{3}$.

Then:

	<u>16 KC</u>	<u>100 KC</u>
$V_{\text{max}} \text{ (RMS)}$	4.5	3.5
$R_g = R_{in} = k R_r \text{ max}$	50 K	30 K
$R_r \text{ max} + R_{in} = (1 + k) R_r \text{ max}$	150 K	90 K
$R_r \text{ max}$ in parallel with R_{in}	33 K	20 K

Using a 12AT7 triode and selecting an operating point at $E_p = 100 \text{ VDC}$, $I_p = 4 \text{ MA}$, $V_G = -0.9 \text{ VDC}$, the tube characteristics are $R_p = 14 \text{ K}$, $\mu = 62$ and $C_{pg} = 1.5 \text{ PF}$. Then for $R_T = 14 \text{ K}$, the voltage gain G_V is 31 and C_M is 48 PF. The feedback network impedance transforming network voltage ratio is:

$$T_{V_o} = \frac{1.4}{G_V \cdot A_{V_C}} = 0.135$$

$$T_{V_o}^2 = 0.018$$

Then:

	<u>16 KC</u>	<u>100 KC</u>
$R_{FB} = \left(\frac{R_r \text{ max} + R_{in}}{T_{V_o}^2} \right)$	8.2 MEGO	4.9 MEGO

R_L	$\approx R_T$	$\approx R_T$
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$V_o \text{ max}$	33 VRMS	26 VRMS
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The oscillator external load R_L	14 K	14 K
------------------------------------	------	------

	<u>16 KC</u>	<u>100 KC</u>
The crystal unit input terminating resistance, $\left(T_{V_0}^2 \left[\frac{R_L \cdot R_p}{R_L + R_p} \right] \right)$	130 ohms	130 ohms
X_{C_M}	210 K	33 K
$\left(\frac{k}{1+k} \right) \frac{R_{r \max}}{X_{C_M}}$	0.16	0.6

Neutralizing is therefore necessary at 100 KC. The required neutralizing capacitor is approximately $1.5/0.135 = 11$ PF. The phase angle at 16 KC is acceptable, and no neutralizing is required.

A suitable transformer primary reactance is 700 ohms. Assuming a primary winding Q of 100, $R_{LP} = 70$ K. This is 5 times R_L , increasing the oscillator load to 17.5 K.

	<u>16 KC</u>	<u>100 KC</u>
The primary winding inductance L_1 is	7 MH	1.1 MH
Assuming a coupling coefficient of 0.9, the secondary winding inductance L_2 is	158 UH	25 UH
and ωL_2	16 ohms	16 ohms
The tuning capacitance is approximately	0.143 UF	2300 PF

If desired, the winding inductances could be increased appreciably to ease the tuning problem.

6-30. 1 to 16 KC Series Oscillator

Crystal characteristics:

$R_{r \max}$ and $P_{C_{MAX}}$ are assumed to be 200 K and 10 UW, respectively.

For $k = 0.5$, $A_{VC} = \frac{1}{3}$.

Then:

$$V_{\max} \text{ (RMS)} = 2 \text{ V}$$

$$R_{\text{in}} = k R_{\text{r max}} = 100 \text{ K}$$

$$R_{\text{r max}} + R_{\text{in}} = 1 + k R_{\text{r max}} = 300 \text{ K}$$

$$R_{\text{r max}} \text{ in parallel with } R_{\text{in}} = 67 \text{ K}$$

Using a 12AX7 at an operating point of $E_p = 100 \text{ VDC}$, $I_p = 0.5 \text{ MA}$, $V_G = -1 \text{ VDC}$, the tube characteristics are $\mu = 100$, $R_p = 85 \text{ K}$, and $C_{pg} = 1.7 \text{ PF}$.

For $R_T = 85 \text{ K}$, $G_V = 50$ and $C_M = 87 \text{ PF}$. The feedback impedance transforming network voltage ratio is:

$$T_{V_O} = 0.084$$

$$T_{V_O}^2 = 0.007$$

Then

$$R_{\text{FB}} = \left(\frac{R_{\text{r max}} + R_{\text{in}}}{T_{V_O}^2} \right) = 43 \text{ megohms}$$

$$R_L = R_T$$

$$V_{O \text{ max}} = 24 \text{ VRMS}$$

The crystal unit input terminating resistance $\left(T_{V_O}^2 \left[\frac{R_L \cdot R_p}{R_L + R_p} \right] \right)$ is 300 ohms.

	<u>16 KC</u>	<u>1 KC</u>
$X_{C_M} :$	115 K	1.84 MEGO
$\left(\frac{k}{1+k} \right) \frac{R_{\text{r max}}}{X_{C_M}} :$	0.58	0.036

Neutralizing is therefore necessary at 16 KC. The required neutralizing capacitor is approximately $1.5/0.084 = 18 \text{ PF}$. No neutralizing is required at 1 KC.

A suitable transformer primary reactance is 4.3 K. Assuming a primary winding Q of 100, R_{LP} is 430 K. This is 5 times R_L , requiring an increase in the oscillator load to 110 K.

	<u>1 KC</u>	<u>16 KC</u>
The primary winding inductance L_1 is	690 MH	43 MH
Assuming a coupling coefficient of 1, the secondary winding inductance is	4.8 MH	0.3 MH
ωL_2	3 ohms	3 ohms
The tuning capacitance is approximately	0.037 UF	2300 PF

6-31. Untuned Low Frequency Oscillators

At the lower frequencies it may not be desirable to employ a tuned circuit in the oscillator because of the problem of tuning. One suitable alternative circuit which may be used below 16 KC employs the crystal unit as a four-terminal network. In this frequency range if requested from the manufacturer, the crystal unit can be supplied having four electrical connections which can then either be paired for operation as a conventional two-terminal crystal unit or can be used as a four-terminal network.

When used in this latter manner, the crystal operates similarly to a filter network giving maximum signal transmission with either a 0 or a 180 degree phase shift at the crystal unit resonance frequency. Using the crystal unit as a phase-inverting network in conjunction with a grounded-cathode amplifier then results in a very simple circuit. Due to the limited experience with this circuit, a worst-case design procedure has not been developed, and it will be necessary for the designer to draw conclusions in this respect.

The design method used consisted of experimentally determining the characteristics of a particular crystal unit as a phase-inverting network and then relating this to the amplifier characteristics. In this particular instance the design frequency was 1 KC, and it was found possible, using a stable audio signal generator, to measure the voltage ratio of the crystal unit input and output signals for various values of output load resistance with the test circuit of Figure 6-28. Including a resistor in the signal input line also enables the crystal unit input resistance to be estimated. The crystal unit test data are given in Table 6-8.

The tabulated data show:

- (a) The input resistance at the crystal unit resonance frequency is approximately equal to the output load resistance R in series with R_p , the crystal unit input resistance when a signal is applied to the two input terminals with the two output terminals shorted.

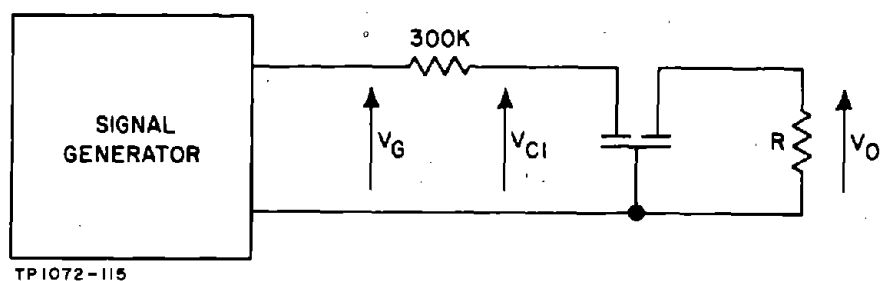


Figure 6-28. Crystal Unit Test Circuit

TABLE 6-8. CRYSTAL UNIT TEST DATA

R	$\frac{V_O}{V_{C1}}$	$\frac{V_{C1}}{V_G}$	Crystal Unit Input Resistance $R_{in} \approx R'_r + R$	$\frac{R}{R'_r + R}$
20 K	0.063	0.50	300 K	0.067
200 K	0.42	0.63	510 K	0.39
510 K	0.54	0.75	900 K	0.57
750 K	0.61	0.78	1.1 MEGO	0.68
1 MEGO	0.69	0.81	1.3 MEGO	0.77

- (b) The voltage transmission ratio is approximately equal to $R/R'_r + R$.
- (c) R'_r is approximately 5.5 times the resonance resistance of the crystal unit as a two-terminal network, which was 55 K in this instance.

It appears, therefore, on the basis of this test that, at the crystal unit resonance frequency, the crystal unit and load resistor act similarly to the network shown in Figure 6-29.

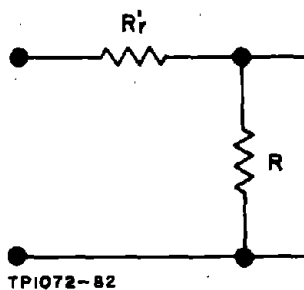


Figure 6-29. Equivalent Circuit of Crystal Unit and Output Load at f_r

The relationship between R_T and R_T' is not known, but if the relationship is linear, the maximum value of R_T' would be approximately 1 megohm. Because of this uncertainty a worst-case design was not attempted, and the following design was calculated for the particular crystal tested. The effect of the crystal output load was not known either, and the design calculation was made for a 200-K load, although the design was subsequently evaluated for loads of 200 K, 510 K, 750 K, and 1 megohm without, however, adjusting the loop gain. The difference in performance was found to be negligible.

Design Calculation (Using analogous notation to that previously employed) - Using a 12AT7 tube at $I_p = 0.75$ MA, $E_p = 60$ V, and $V_G = -1.5$ V, then $\mu = 35$ and $R_p = 35$ K. For $R_T = 17$ K, the voltage gain is then 12. For $R = 200$ K, the voltage attenuation between the filter input and output terminals (A_{V_C}) is 0.42. Therefore, the permissible attenuation between the tube plate and the crystal input (T_{V_O}), allowing for a loop voltage gain of 1.4 is:

$$T_{V_O} = \frac{1.4}{G_V \cdot A_{V_C}} = 0.28$$

Using a resistive feedback network and assuming the loading due to the crystal to be negligible, the resistor ratio is then:

$$\frac{R_2}{R_1 + R_2} = T_{V_O} = 0.28 \text{ or } \frac{R_2}{R_1} = 0.39$$

where R_1 and R_2 are designated in Figure 6-31. For $R_1 = 100$ K, then $R_2 = 36$ K, satisfying the assumption that R_2 is much less than the crystal input resistance.

The amplifier total load resistance consists of the oscillator resistance, the plate feed resistance, and the feedback network resistance in parallel. The latter are 51 K and 130 K, respectively, and the external oscillator load resistance is therefore 33 K. The allowable crystal unit input voltage, assuming a permissible crystal unit dissipation of 10 UW, is 2.2 VRMS, and the allowable plate signal voltage is then 8 VRMS. The evaluation data for this design is presented in Table 6-9 and Figure 6-30.

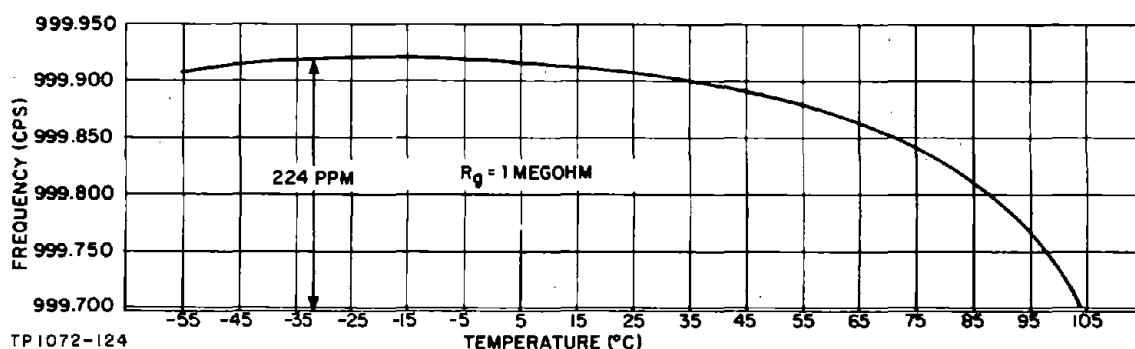


Figure 6-30. Frequency Vs. Temperature, 1-KC Tube Oscillator

TABLE 6-9. DESIGN EVALUATION DATA, 1-KC VACUUM TUBE OSCILLATOR (FOUR-TERMINAL CRYSTAL)

Crystal Unit: T-9J, $f_r = 999.930$ CPS, $R_r = 55$ K

	Value of R_g			
	200K	510K	750K	1 MEG
Oscillator Frequency (CPS)	999.910	999.905	999.910	999.905
Nominal V_o	5.2	5.9	5.9	5.8
Influence of $\pm 10\%$ Change in $B+$ on Oscillator Frequency	$< \pm 10$ PPM	$< \pm 10$ PPM	$< \pm 10$ PPM	$< \pm 10$ PPM
Influence of $\pm 10\%$ Change in $B+$ on Output Voltage	$\Delta V_o = \pm 22\%$	$\Delta V_o = \pm 20\%$	$\Delta V_o = \pm 20\%$	$\Delta V_o = \pm 14\%$
Influence of $\pm 10\%$ Change in R_L on Oscillator Frequency	$< \pm 4$ PPM	$< \pm 4$ PPM	$< \pm 4$ PPM	$< \pm 4$ PPM
Influence of $\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_o = \pm 6\%$	$\Delta V_o = \pm 5\%$	$\Delta V_o = \pm 5\%$	$\Delta V_o = \pm 4\%$
Influence of $\pm 10\%$ Change in E_f on Oscillator Frequency	$< \pm 3$ PPM	$< \pm 3$ PPM	$< \pm 3$ PPM	$< \pm 3$ PPM
Influence of $\pm 10\%$ Change in E_f on Output Voltage	$\Delta V_o = \pm 3\%$	$\Delta V_o = \pm 2\%$	$\Delta V_o = \pm 2\%$	$\Delta V_o = \pm 2\%$
Influence of -50°C to $+80^\circ\text{C}$ Change in T_A on Oscillator Frequency	± 60 PPM	± 50 PPM	± 55 PPM	± 50 PPM
Influence of -50°C to $+80^\circ\text{C}$ Change in T_A on Output Voltage	$\Delta V_o = \pm 6\%$	$\Delta V_o = \pm 2\%$	$\Delta V_o = \pm 2\%$	$\Delta V_o = \pm 2\%$

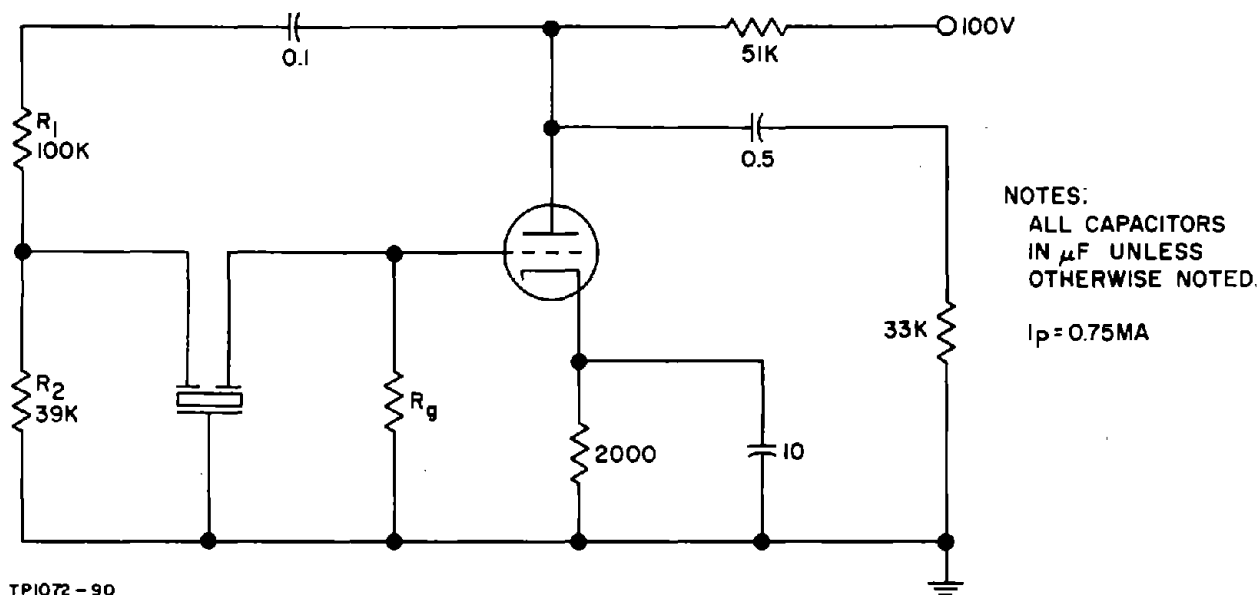


Figure 6-31. 1-KC Crystal Phase-Inverting Oscillator

6-32. Two-Stage Oscillator

The alternative to using the crystal unit as a phase-inverting filter is a two-stage amplifier configuration where the increased voltage gain allows an inefficient feedback network to be used. Tuning is not entirely eliminated, however, because of the possibility of uncontrolled oscillation at high frequencies; the crystal unit parallel capacitance completing the feedback path.

One method of doing this is to include a Wien bridge network tuned to the design frequency in the feedback network. But this is not entirely satisfactory because of the resulting circuit complexity. Another possibility (not tried) would be to arrange the time constants of the grid and plate circuits so that their net phase angle is zero at the design frequency but which introduces a substantial phase lag and gain reduction at higher frequencies. The techniques used in analog computer circuits may be helpful in this respect. The design procedure employed is similar to that described previously for use at higher frequencies.

The oscillator configuration for this design example is as shown in Figure 6-32, and the design calculation using analogous notation to that employed previously is as follows, using a 12AX7 triode operating at $E_p = 100$ VDC, $I_p = 0.5$ MA, $V_G = -1$ VDC, $R_p = 85$ K, $\mu = 100$. For $R_{T1} = 50$ K and $R_{T2} = 30$ K, the total voltage gain from V_1 grid to V_2 plate is 970. For a loop voltage gain of 1.4 in a worst-case design, the voltage attenuation A from the plate of V_2 to the grid of V_1 is then $\frac{1}{690}$. This is satisfied by the feedback network

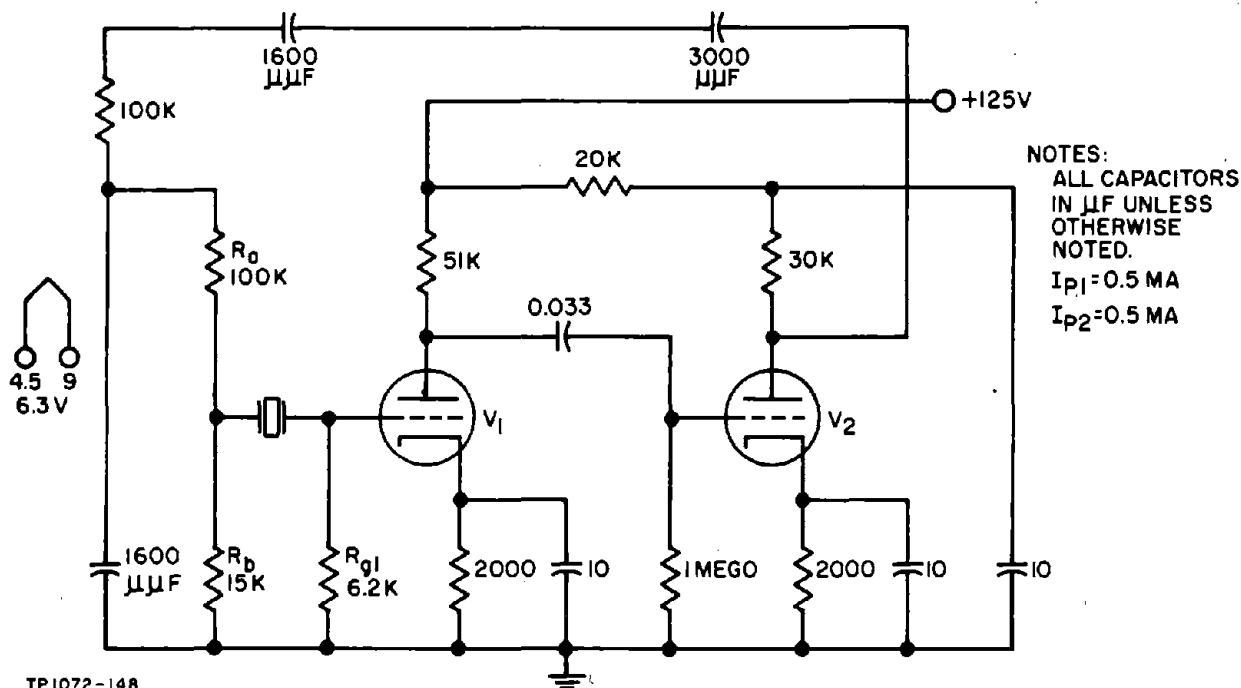


Figure 6-32. 1-KC Two-Stage Wien Bridge Oscillator

shown in Figure 6-32, where:

$$A = \frac{1}{3} \times \frac{R_b}{R_a + R_b} \times \frac{R_{g1}}{R_{g1} + 200 \text{ K}} = \frac{1}{690}$$

Referring to the Wien bridge analysis of Section 4, the requirement for zero phase shift in the Wien bridge network is:

$$C_1 R_1 C_2 R_2 = \frac{1}{(\omega')^2}$$

where the loading due to the crystal unit is included in R_2 and the amplifier output resistance forms a part of R_1 . R_2 is therefore 113 K and R_1 is 122 K. For $C_1 = 1150 \text{ PF}$ and $C_2 = 1600 \text{ PF}$, $\omega' = 6280$ and $f' = 1000 \text{ CPS}$. The nominal value of C_1 required was 1040 PF.

The permissible output voltage before crystal overdrive occurs is obtained by considering the case when R_r is equal to $R_r \text{ min}$, which is assumed to be $1/9 R_r \text{ max}$; that is, 22 K. The crystal input voltage causing a crystal dissipation of 10 UW is 0.6 VRMS. The attenuation between the plate of V_2 and the crystal input terminal is approximately 0.043. Therefore, the allowable plate signal voltage when a very good crystal unit is in circuit is 14 VRMS.

The evaluation data are presented in Figure 6-33 and Table 6-10, followed by the data for a 3-KC oscillator of the same design in Figures 6-34 and 6-35 and Table 6-11.

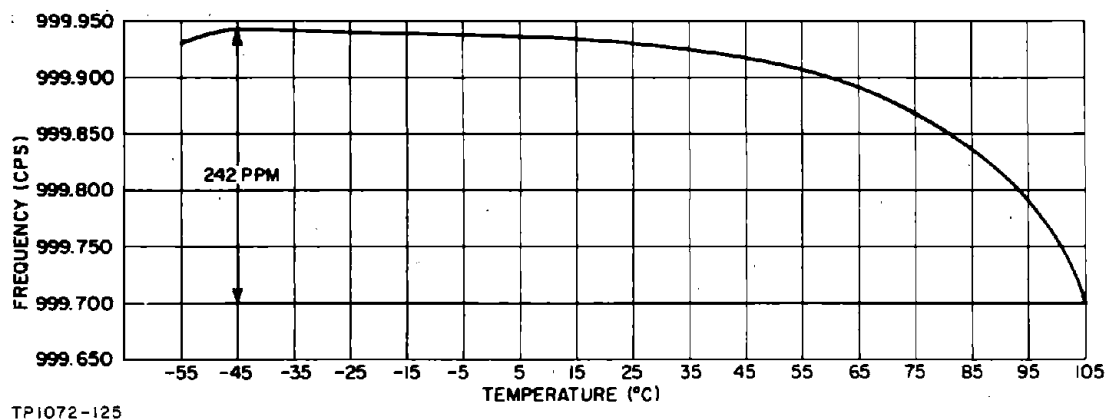


Figure 6-33. Frequency Vs. Temperature for the 1-KC Two-Stage Tube Oscillator (Wien Bridge)

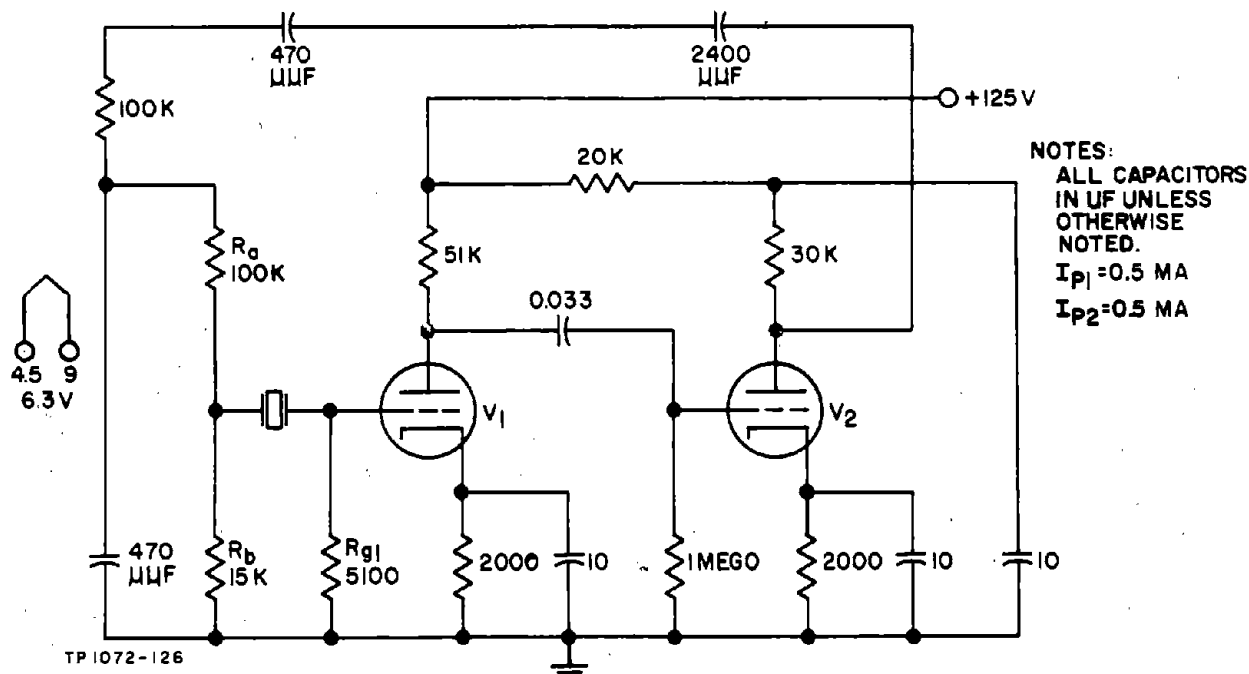
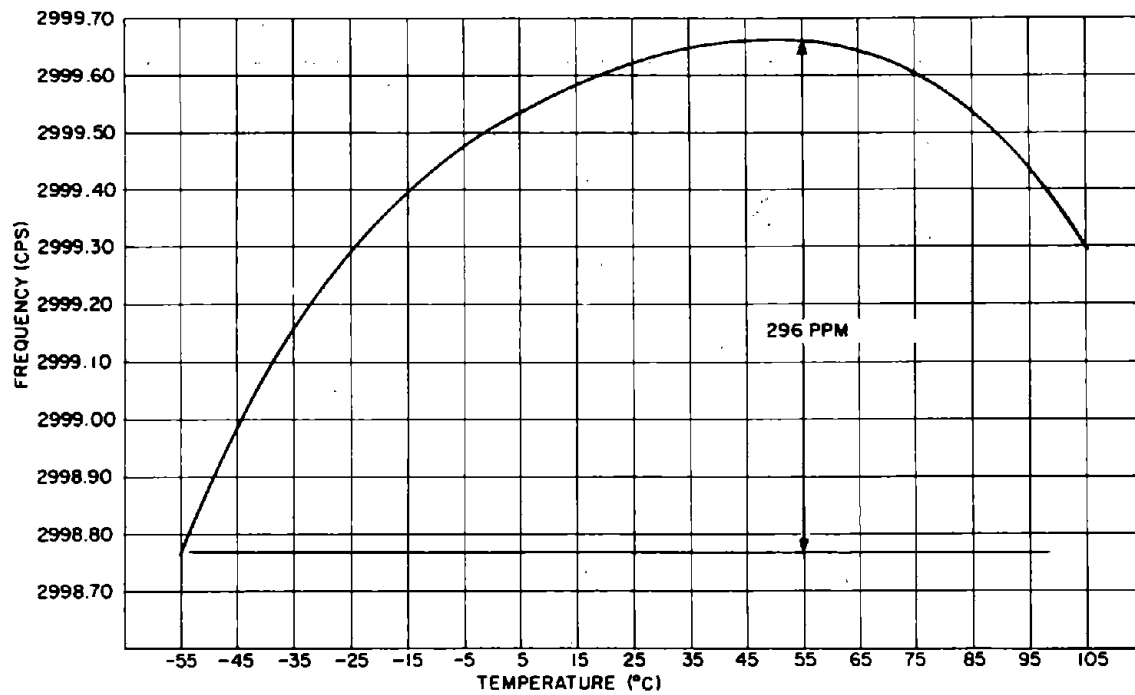


Figure 6-34. 3-KC Wien Bridge Oscillator

TABLE 6-10. DESIGN EVALUATION DATA, 1-KC TWO-STAGE TUBE OSCILLATOR

Crystal Unit: T-9J, $f_r = 999.93$ CPS, $R_r = 55$ K

EFFECT OF	CHANGE	TEST CONDITIONS
$\pm 10\%$ Change in B+ on Oscillator Frequency	$\leq \pm 3$ PPM	$E_f = 6.3V$, $R_L = 30K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in B+ on Output Voltage	$\Delta V_o = \pm 13\%$	$E_f = 6.3V$, $R_L = 30K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Oscillator Frequency	$\leq \pm 3$ PPM	$E_f = 6.3V$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_o = \pm 7\%$	$E_f = 6.3V$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in E_f on Oscillator Frequency	$\leq \pm 3$ PPM	$R_L = 30K$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in E_f on Output Voltage	$\Delta V_o = \pm 2\%$	$R_L = 30K$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
$-50^\circ C$ to $+80^\circ C$ Change in T_A on Oscillator Frequency	± 47 PPM	$R_L = 30K$, $E_{bb} = 125V$, $E_f = 6.3V$
$-50^\circ C$ to $+80^\circ C$ Change in T_A on Output Voltage	$\Delta V_o = \pm 1\%$	$R_L = 30K$, $E_{bb} = 125V$, $E_f = 6.3V$



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Figure 6-35. Frequency Vs. Temperature, 3-KC Tube Oscillator
(Wien Bridge)

TABLE 6-11. DESIGN EVALUATION DATA, 3-KC TWO-STAGE TUBE OSCILLATOR
Crystal Unit: T-9A $f_r = 2999.6$ CPS, $R_r = 50$ KC

EFFECT OF	CHANGE	TEST CONDITIONS
$\pm 10\%$ Change in $B+$ on Oscillator Frequency	$\leq \pm 3$ PPM	$E_f = 6.3V$, $R_L = 30K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in $B+$ on Output Voltage	$\Delta V_o = \pm 13\%$	$E_f = 6.3V$, $R_L = 30K$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Oscillator Frequency	$\leq \pm 3$ PPM	$E_f = 6.3V$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_o = \pm 7\%$	$E_f = 6.3V$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in E_f on Oscillator Frequency	$\leq \pm 3$ PPM	$R_L = 30K$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in E_f on Output Voltage	$\Delta V_o < \pm 2\%$	$R_L = 30K$, $E_{bb} = 125V$, $T_A \approx 25^\circ C$
$-55^\circ C$ to $+80^\circ C$ Change in T_A on Oscillator Frequency	± 150 PPM	$R_L = 30K$, $E_{bb} = 125V$, $E_f = 6.3V$
$-55^\circ C$ to $+80^\circ C$ Change in T_A on Output Voltage	$\Delta V_o < \pm 2\%$	$R_L = 30K$, $E_{bb} = 125V$, $E_f = 6.3V$

SECTION 7 TRANSISTOR SERIES RESONANCE OSCILLATOR DESIGN

7-1. GENERAL

Because of the variations of crystal unit and transistor amplifier characteristics as functions of frequency, no single design technique is applicable throughout the entire available frequency range from below 1 KC to 200 MC. The resonance resistance of the crystal unit is the major variable, the maximum values ranging from possibly 200 K at 1 KC to 15 ohms at 20 MC. This variation as a function of frequency occurs mainly as a relatively smooth transition between adjacent frequencies.

There are, however, certain frequencies at which an abrupt change of maximum resonance resistance level of an order of magnitude or more occurs. It is found that a different design approach is required for the frequency ranges lying between each of these discontinuities, and the following discussion is arranged accordingly in four parts as follows:

- (a) Design between 1 KC and 100 KC
- (b) Design between 90 KC and 500 KC
- (c) Design between 800 KC and 30 MC
- (d) Design between 30 MC and 200 MC

The first three of these range sub-divisions are determined as described by the discontinuous behavior of the crystal unit resonance resistance. An overlap of ranges occurs between 90 and 100 KC because in this region crystal units with radically different values of resonance resistance are available, and a discontinuity occurs between 500 KC and 800 KC because no military standard crystal units are available in this region. The fourth range sub-division, however, is dictated by the complex behavior of transistor amplifiers at frequencies above 30 MC.

It is convenient to first discuss the design of oscillators in the 800-KC to 30-MC range, which then serves as a basis for the discussion of the 30 to 200 MC and the 90 to 500 KC ranges. The latter then serves as a starting point for the 1-KC to 100-KC range. The order of presentation is therefore 800 KC to 30 MC, 30 to 200 MC, 90 to 500 KC, and 1 KC to 100 KC.

7-2. SERIES RESONANCE CRYSTAL UNIT CHARACTERISTICS, 800 KC TO 30 MC

Table 7-1 gives the major characteristics of the military standard series resonance crystal units applicable in the 800-KC to 30-MC frequency range. The multiplicity of crystal units is due largely to the various crystal holder types available, and the number is further increased by there being usually two and sometimes three frequency tolerances available for selection in any frequency band.

TABLE 7-1. MILITARY STANDARD SERIES RESONANCE CRYSTAL UNITS, 800 KC TO 30 MC

Frequency Range in MC	Operating Temperature Range (Centigrade)	Frequency Tolerance (\pm Percent)	Rated Drive (MW)	Maximum Resonance Resistance (ohms)	Crystal Unit Type	Holder Type
WIDE TEMPERATURE RANGE CRYSTAL UNITS						
0.8 to 20	-55 to +105	0.005	10 and 5	520 to 15	CR-19A/U	HC-6/U
0.8 to 20	-55 to +105	0.0025	10 and 5	520 to 15	CR-85/U	HC-6/U
5 to 20	-55 to +105	0.005	5	50 to 20	CR-60A/U	HC-18/U
*10 to 61	-55 to +105	0.005	20	40	CR-51A/U	HC-6/U
10 to 61	-55 to +105	0.005	2 and 4	40	CR-52A/U	HC-6/U
*15 to 50	-55 to +105	0.005	2	50 and 75	CR-24/U	HC-18/U
17 to 61	-55 to +105	0.005	2	40	CR-55/U	HC-18/U
17 to 61	-55 to +105	0.0025	2	40	CR-67/U	HC-18/U
17 to 61	-55 to +105	0.005	2	40	CR-72/U	HC-18/U
17 to 61	-55 to +105	0.0025	2	40	CR-76/U	HC-18/U
17 to 62	-55 to +105	0.002	2	40	CR-77/U	HC-25/U
17 to 61	-55 to +105	0.005	2	40	CR-81/U	HC-25/U
TEMPERATURE CONTROLLED CRYSTAL UNITS						
0.8 to 20	70 to 80	0.002	5 and 2.5	520 to 15	CR-28A/U	HC-6/U
0.8 to 20	80 to 90	0.002	5 and 2.5	520 to 15	CR-35A/U	HC-6/U
10 to 61	70 to 80	0.001	2 and 1	60 and 40	CR-65/U	HC-6/U
10 to 75	70 to 80	0.002	2 and 1	60 and 40	CR-32A/U	HC-6/U
17 to 61	80 to 90	0.002	2 and 1	40	CR-61/U	HC-18/U
17 to 61	80 to 90	0.002	2 and 1	40	CR-84/U	HC-25/U

*Special Application

The maximum resonance resistance of crystal units varies appreciably with operating frequency over the 800-KC to 30-MC range, particularly at frequencies below 20 MC. This is shown in Figure 7-1, which is a plot of the specified maximum crystal unit resonance resistance values as a function of frequency. The actual range of values likely to be encountered for any crystal type at a given nominal frequency will be from $R_{r \text{ max}}$ to $\frac{1}{9} R_{r \text{ max}}$ at frequencies below 20 MC, and $R_{r \text{ max}}$ to $\frac{1}{4} R_{r \text{ max}}$ from 20 to 30 MC.

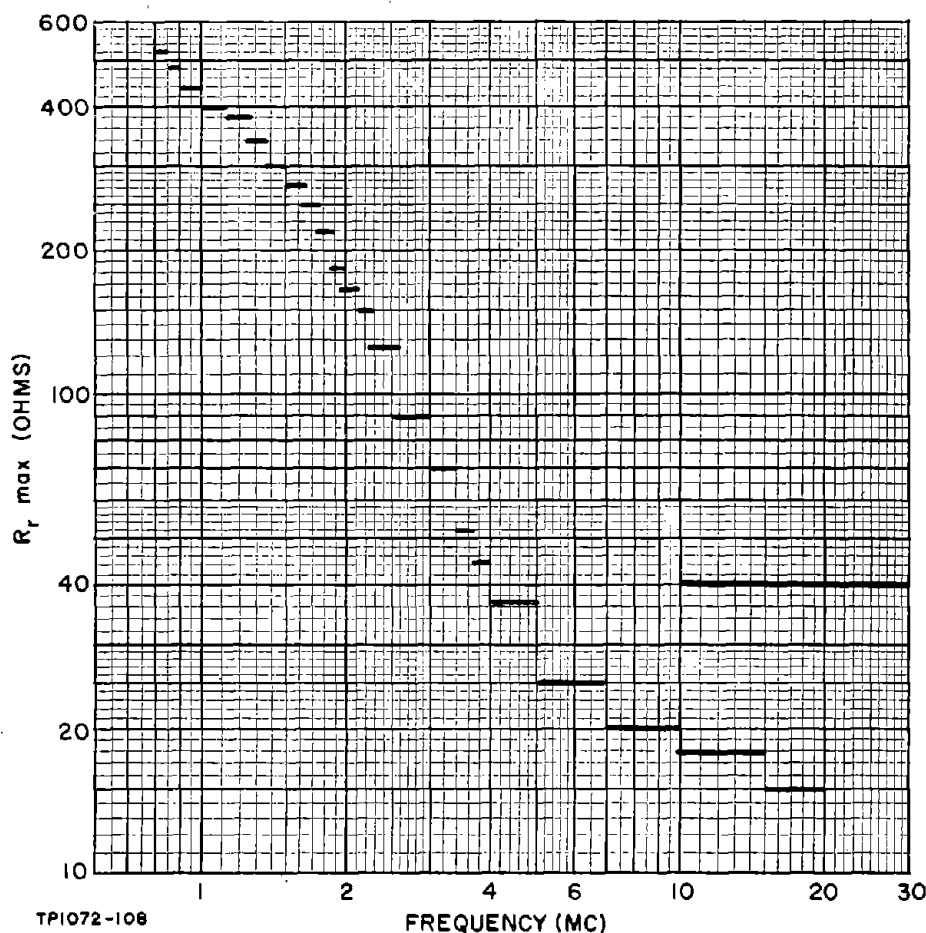


Figure 7-1. Variation of Crystal Unit Resonance Resistance With Frequency

7-3. TRANSISTOR SERIES OSCILLATORS, 800 KC TO 30 MC

In this frequency range, the input resistance of a grounded base amplifier can provide an almost ideal terminating level for series resonance crystal units. The discussion of grounded base amplifier input resistance given in Section 3 shows that, with the possible exception of the region where the complex internal feedback causes an input resistance peak, the series input resistance $R_{in(s)}$ of an

amplifier can, by a suitable choice of bias levels, be made small relative to the values of $R_r \text{ max}$ given in Figure 7-1, thereby providing a suitable crystal unit terminating resistance level. Further, in the region where the peak of amplifier series input resistance occurs, $R_r \text{ max}$ has a value of 40 ohms or greater, and, by selecting a suitable value of emitter current, $R_{in(s)}$ can also be made sufficiently small in this frequency region to give a good crystal unit terminating resistance value. It is therefore unnecessary to use an impedance transforming network between the crystal unit and the amplifier input, and, provided an adequate loop gain can be obtained, it is then possible to use the simple oscillator configuration shown in Figure 7-2(a).

At the crystal unit series resonance frequency, this circuit appears as shown in Figure 7-2(b), from which it can be seen that R_r acts as an emitter degeneration resistor. As discussed in Section 3, the effect of an emitter degeneration resistor is to extend the frequency range over which the amplifier voltage gain is frequency independent, and to reduce the phase shift of the amplifier. For the amplifier total load levels likely to be met with in practice, and with the maximum values of crystal resonance resistance encountered, this means that the voltage gain from point X in Figure 7-2(b) to the collector is essentially frequency independent below 30 MC when a transistor with a typical f_T of 300 MC is used, and possibly 50 MC when the typical transistor f_T is 700 MC or greater.

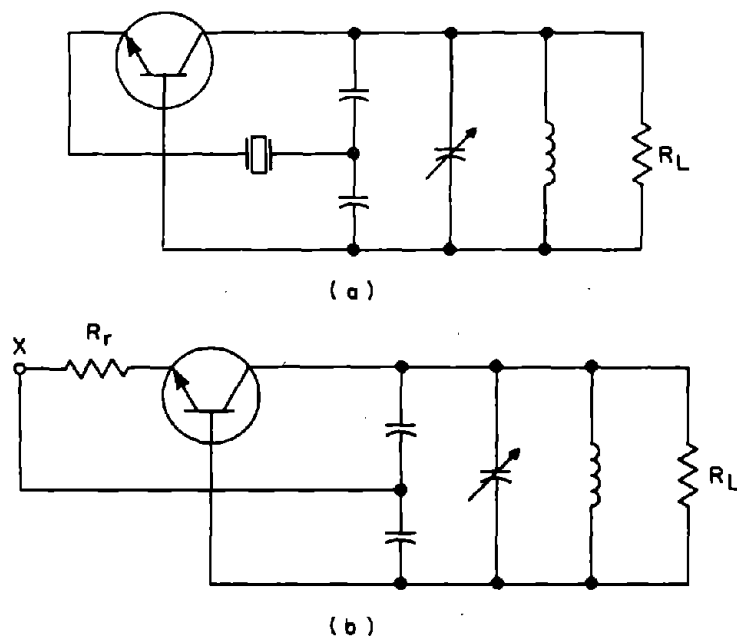


Figure 7-2. Series-Resonance Common-Base Oscillator

Inspection of the common-base amplifier input resistance plots given in Section 3 also shows that $R_{in(s)}$ is almost independent of frequency up to 20 MC and that an estimate of its value sufficiently accurate for the estimation of crystal loading can be obtained to beyond 30 MC. For design frequencies below 30 MC and provided a suitable transistor is used, it is therefore possible to determine the oscillator component values by simple calculation.

7-4. Loop Voltage Gain Determination

The loop voltage gain of the circuit of Figure 7-2(b) is the product of the amplifier voltage gain and the feedback network attenuation. The latter consists of two parts: that occurring in the impedance transforming network between the amplifier output (transistor collector) and the crystal unit, and that resulting from the connection of the crystal unit to the amplifier input. Over the frequency range considered, the latter can be accounted for in the amplifier gain calculation by replacing r_e by $r_e + R_r$. That is, the net amplifier voltage gain G_{VR} , including the effect of R_r is:

$$G_{VR} = \frac{\alpha_o \cdot R_T}{r_e + R_r + r_{bb'}(1 - \alpha_o) + \frac{R_T}{R_D}(r_{bb'} + r_e + R_r)} \quad (7-1)$$

The net voltage gain of the amplifier and crystal unit combination will be smallest when the crystal unit resonance resistance has its maximum value $R_{r \max}$, and this is the value to be used in a worst-case design. Further, for the values of R_T likely to be used, the term $\frac{R_T}{R_D}(r_{bb'} + r_e + R_r)$ will be small compared to $R_{r \max}$, and Equation (7-1) can be approximated as:

$$G_{VR} \approx \frac{R_T}{r_e + R_{r \max} + r_{bb'}(1 - \alpha_o)} \quad (7-2)$$

The worst-case loop voltage gain G_{VL} is then:

$$G_{VL} = G_{VR} \cdot A_{Vt} \quad (7-3)$$

where A_{Vt} is the voltage attenuation ratio of the impedance transforming network between the amplifier output and the crystal.

7-5. Crystal Unit Loading

At frequencies up to 20 MC, the series input resistance of a common-base amplifier has a value approximately equal to:

$$R_{in(s)} = r_e + r_{bb'}(1 - \alpha_o) \quad (7-4)$$

Crystal unit loading considerations dictate that $R_{in(s)}$ should be small compared to R_r . If $R_{in(s)}$ is equal to or less than $1/3 R_r \text{ max}$, this will result in a minimum loaded $\frac{d\phi}{df}$ of 75 percent of that of the crystal unit alone when a worst-case crystal unit ($R_r = R_r \text{ max}$) is considered. This represents a reasonable compromise between crystal loading and loop voltage gain considerations, and with this assumption the net voltage gain of the amplifier and crystal unit combination can be restated as:

$$G_{VR} \approx \frac{R_T}{K \cdot R_r \text{ max}} \quad (7-5)$$

where K is a constant depending on the relative values of $R_{in(s)}$ and $R_r \text{ max}$ and has a value of:

$$\begin{aligned} K &= 1 + \frac{R_{in(s)}}{R_r \text{ max}} \\ &= 1 + \frac{r_e + r_{bb'}(1 - \alpha_o)}{R_r \text{ max}} \end{aligned} \quad (7-6)$$

For the assumed crystal loading conditions, K will have a value in the range of 1 to 1.33. The lower value applies when $R_{in(s)}$ is much smaller than $R_r \text{ max}$, and the latter value when $R_{in(s)}$ equals $1/3 R_r \text{ max}$.

7-6. Loop Gain as a Function of R_L

Equation (7-5) shows that, for the assumed crystal unit loading conditions, the net voltage gain from the crystal unit input to the collector is almost entirely determined by the ratio of the collector total load resistance to the crystal unit resonance resistance, since the effect of $R_{in(s)}$ is small.

R_T is the parallel combination of the oscillator external load R_L and the impedance transforming network parallel input resistance R_{FB} . Neglecting losses in the impedance transforming network, R_{FB} is related to the secondary load resistance r_s by the equation:

$$R_{FB} = \frac{r_s}{A^2 V_t} \quad (7-7)$$

In this case r_s is the series combination of $R_{in(s)}$ and $R_r \text{ max}$, and substituting for r_s in terms of $R_{in(s)}$ and $R_r \text{ max}$ gives:

$$R_{FB} = \frac{K \cdot R_{r \max}}{A_{V_t}^2} \quad (7-8)$$

Then, since R_T is equal to R_L and R_{FB} in parallel:

$$R_T = \frac{K \cdot R_{r \max} \cdot R_L}{K \cdot R_{r \max} + A_{V_t}^2 \cdot R_L} \quad (7-9)$$

Substituting into Equation (7-5) for R_T then gives:

$$G_{VR} = \frac{R_L}{K \cdot R_{r \max} + A_{V_t}^2 \cdot R_L} \quad (7-10)$$

and from Equation (7-3):

$$G_{VL} = \frac{R_L \cdot A_{V_t}}{K \cdot R_{r \max} + A_{V_t}^2 \cdot R_L} \quad (7-11)$$

or transposing Equation (7-11):

$$\frac{R_L}{R_{r \max}} = \frac{K \cdot G_{VL}}{A_{V_t} (1 - G_{VL} \cdot A_{V_t})} \quad (7-12)$$

A loop voltage gain of 1.4 for a worst-case design is adequate in protecting against loop gain variations with temperature, etc., particularly in view of the large amount of degeneration introduced by $R_{r \max}$. Substituting this value of loop voltage gain and the limit values of K into Equation (7-12) gives:

For $K = 1.33$

$$\frac{R_L}{R_{r \max}} = \frac{1.86}{A_{V_t} (1 - 1.4 \cdot A_{V_t})} \quad (7-13)$$

For $K = 1$

$$\frac{R_L}{R_{r \max}} = \frac{1.4}{A_{V_t} (1 - 1.4 \cdot A_{V_t})} \quad (7-14)$$

Figure 7-3 gives plots of Equations (7-13) and (7-14). These show that the minimum usable value of R_L determined by loop voltage gain and crystal loading considerations occurs for a feedback transforming network attenuation A_{V_t} of approximately 0.36 and lies in the range of 8 to 10 $R_{r \max}$, depending on the relative values of $R_{in(s)}$ and $R_{r \max}$. However, this does not take into

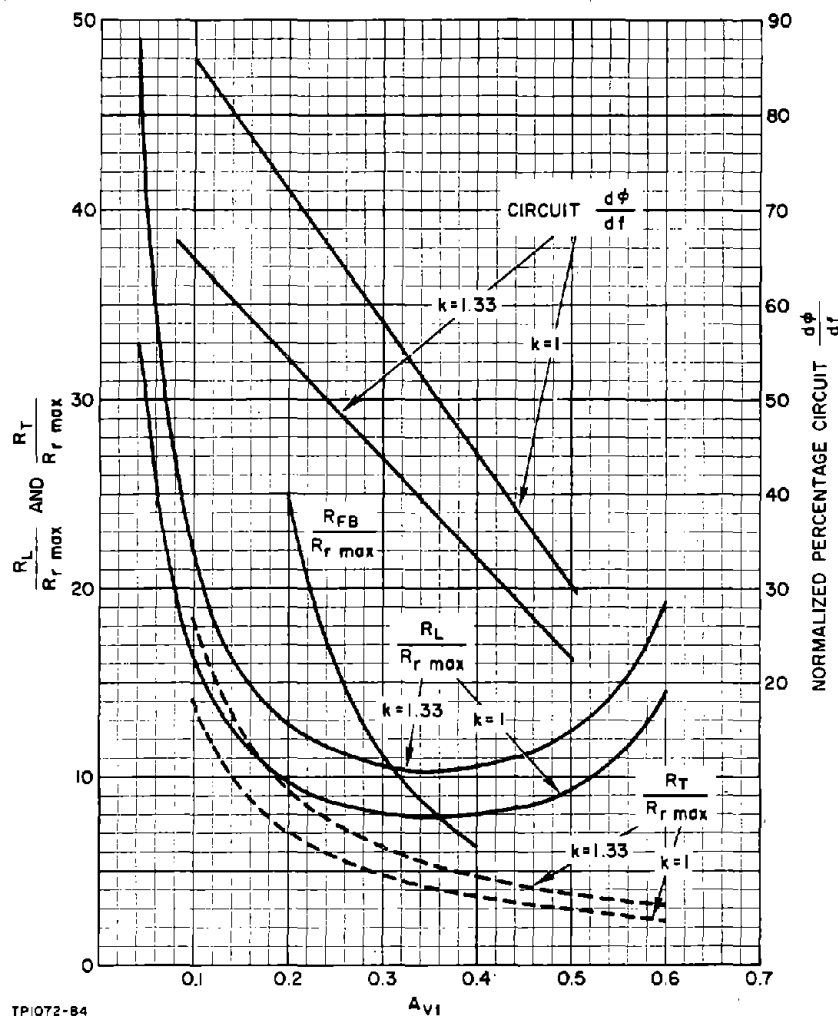


Figure 7-3. $\frac{R_L}{R_{r \max}}$, $\frac{R_T}{R_{r \max}}$, and $\frac{d\phi}{df}$ as Functions of A_{vt} and K

account the crystal unit loading due to the terminating resistance appearing at the driving source side of the crystal unit, which will also influence the desirable value of R_L . This resistance consists of the oscillator load resistance R_L and the amplifier output resistance $R_{o(p)}$ in parallel reflected to the secondary side of the impedance transforming network. $R_{o(p)}$ will normally be much larger than R_L and, therefore, the terminating resistance r_t seen by the crystal unit at the driving source side is approximately:

$$r_t \approx A_{vt}^2 \cdot R_L \quad (7-15)$$

The total crystal unit terminating resistance is then r_t when $K = 1$ and $r_t + 1/3 R_{r \max}$ when $K = 1.33$. From Section 2 the circuit $\frac{d\phi}{df}$ is then:

For $K = 1$

$$\text{Circuit } \frac{d\phi}{df} = \text{Crystal unit } \frac{d\phi}{df} \cdot \frac{R_{r \max}}{r_t + R_{r \max}} \quad (7-16)$$

For $K = 1.33$

$$\text{Circuit } \frac{d\phi}{df} = \text{Crystal unit } \frac{d\phi}{df} \cdot \frac{R_{r \max}}{r_t + 1.33 R_{r \max}} \quad (7-17)$$

Substituting values of r_t calculated from Equation (7-15) into Equations (7-16) and (7-17) gives the circuit $\frac{d\phi}{df}$ values normalized to the crystal unit $\frac{d\phi}{df}$ plotted in Figure 7-3. These plots show that the circuit $\frac{d\phi}{df}$ is 50 percent of that of the crystal unit alone when AV_t equals 0.36 and 0.24 for K values of 1 and 1.33, respectively. These values represent a reasonable compromise condition for total crystal unit loading and will subsequently be used as design limits, operation with AV_t values larger than those quoted being considered undesirable.

7-7. Crystal Unit Dissipation

The driving source voltage applied to the crystal unit is limited by the crystal unit dissipation rating. When $R_{in(s)}$ is linear and much smaller than $1/9 R_{r \max}$, the allowable drive voltage must be less than:

$$V_{\max} = K\sqrt{P_{C\max}} \cdot \frac{R_{r \max}}{9} \quad (7-18)$$

where K is a constant allowing for drive source voltage increase with loop gain and $B+$ increases. And when $R_{in(s)}$ is intermediate between $1/9 R_{r \max}$ and $R_{r \max}$, the permissible drive voltage is:

$$V_{\max} = 2K_1\sqrt{P_{C\max}} \cdot R_{in(s)} \quad (7-19)$$

Equations (7-18) and (7-19) are derived on the assumption that $R_{in(s)}$ remains constant as the loop gain increases. This is not the case in transistor amplifiers where, as the loop voltage gain increases, the signal appearing between the emitter and base exceeds the linear operating range of the emitter-base junction, and for some portion of the cycle the emitter-base junction is wholly or partially reverse-biased. The effect is illustrated in Figure 7-4 which shows the emitter and crystal unit input voltage waveforms of a 1-MC oscillator

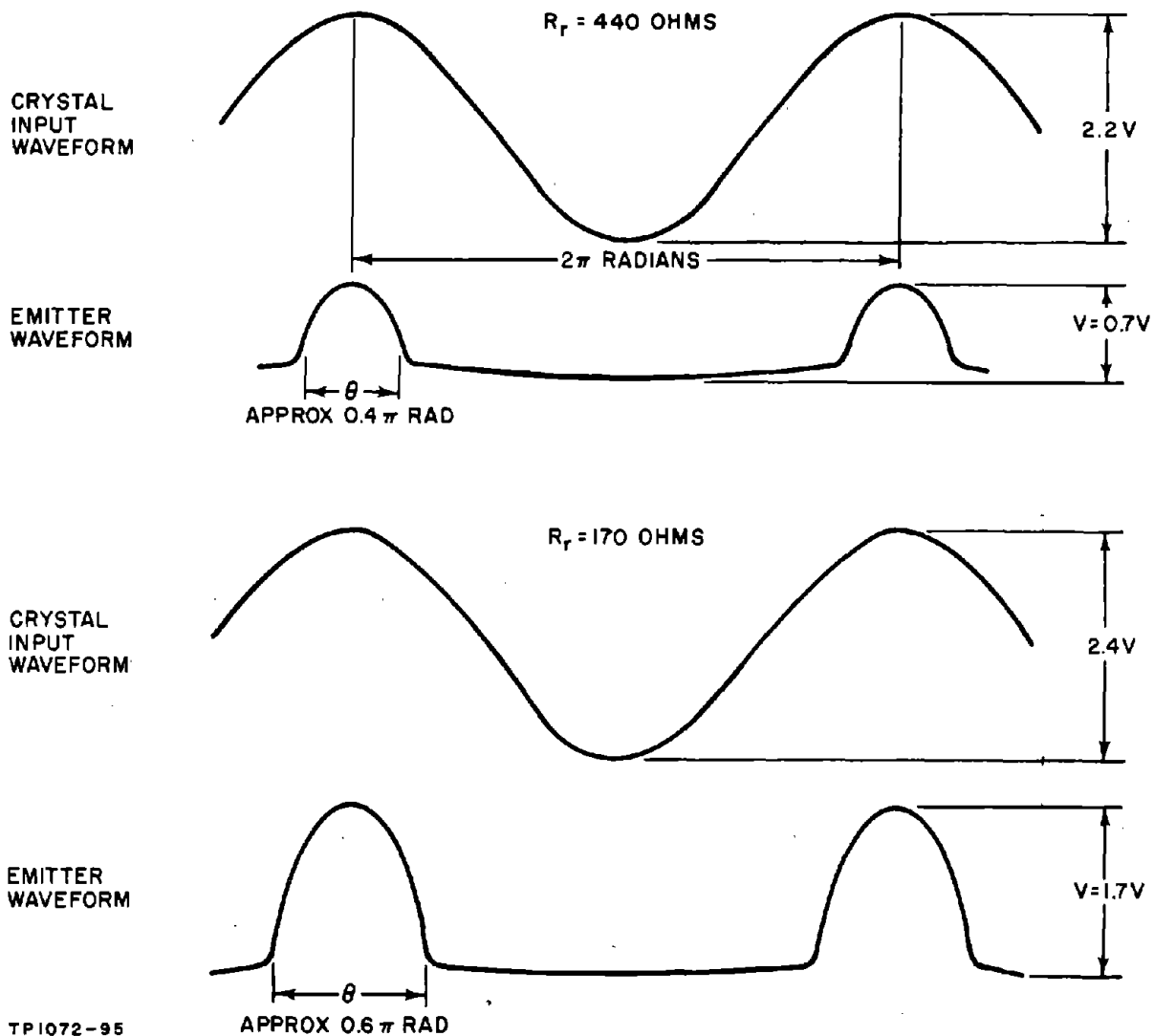


Figure 7-4. Crystal Unit and Emitter Waveforms of a 1 MC Series Oscillator

of this type for R_T values of 440 and 170 ohms. The loop voltage gain for $R_T = 440$ ohms was approximately 1.4. If the emitter waveforms of Figure 7-4 are assumed to have the form of a horizontal section of a sine wave, the fundamental frequency component peak-to-peak amplitude E of the emitter waveforms is given by the formula*:

$$E = \frac{2V}{\pi (1 \cos \frac{\theta}{2})} \left[\left(\sin \frac{\theta}{2} - \frac{\theta}{2} \cos \frac{\theta}{2} \right) + \left(\frac{\theta}{2} - \sin \frac{\theta}{2} \cos \frac{\theta}{2} \right) \right] \quad (7-20)$$

where θ and V are defined in Figure 7-4.

* Terman: Radio Engineers Handbook

Substituting the values of θ and V given in Figure 7-4 into Equation (7-20) gives emitter waveform fundamental frequency component amplitudes of 0.54 and 1.9 V peak-to-peak for R_r equals 440 and 170 ohms, respectively. Subtracting these values from the crystal unit input voltages gives the fundamental frequency voltages across the crystal units as 1.7 and 0.5 V peak-to-peak for R_r equals 440 and 170 ohms, respectively. The oscillator was operating at the crystal resonance frequency, and therefore the fundamental frequency power component is equal to the fundamental component of crystal unit voltage squared divided by the resonance resistance of the crystal unit, giving 0.82 and 0.18 MW for the 440- and 170-ohm crystal units, respectively.

The overtone resonance modes of the crystal unit are not harmonically related to the fundamental resonance mode, and hence the crystal unit is essentially reactive at the harmonic frequencies of the emitter waveform. Consequently, the power dissipated in the crystal unit due to these signal components will be negligible, and the total crystal unit dissipation is approximately equal to that due to the fundamental frequency component.

In this particular example, therefore, it appears that the crystal dissipation decreases rather than increases with the loop gain. The extent to which this effect will occur in any particular design depends on the collector signal voltage, the impedance transforming network voltage attenuation ratio, the emitter DC current, and the crystal unit signal current. The crystal unit dissipation is therefore difficult to estimate, and it has not been found possible to develop a simple formula which adequately describes the crystal unit dissipation. It is evident, however, that it will be much less than that given by Equations (7-18) and (7-19).

Based on the preceding example and on similar results for a 5-MC oscillator, it appears that it will be quite conservative to design on the basis of a crystal unit dissipation of one-half the dissipation rating for a worst-case design. It is then unlikely that the crystal unit dissipation will ever exceed its rating for any value of resonance resistance. For want of a more accurate estimate, this will be used subsequently as a design condition. Ignoring the presence of $R_{in}(s)$ in series with the crystal unit, this condition gives:

$$V_{max} = \sqrt{\frac{P_{C_{MAX}}}{2}} \cdot R_{r \max} \quad (7-21)$$

The non-linear behavior of the amplifier input resistance creates doubts concerning the validity of the crystal unit loading conditions previously derived. In the example given of non-linear operation, the transistor was biased at an emitter current of 1.4 MA, giving an amplifier small-signal input resistance of approximately 20 ohms. The actual input resistance is increased substantially above this value by the non-linear operation. Calculating on the basis of the

fundamental frequency voltages and the relative emitter and crystal unit voltages, the actual amplifier input resistance is 140 and 520 ohms for the 440 and 170 ohm crystal units, respectively. This does not, however, appear to be a valid approach to estimating the loading conditions. During the period when the large emitter signal voltage excursions occur, the circuit is "freewheeling," the amplifier is cutoff and the loop is open-circuited, and signals within the circuit are solely due to the release of energy by the amplifier tank circuit and the crystal unit. The crystal unit is therefore incapable of controlling the oscillator frequency during this part of the oscillation period. During the remainder of the cycle, the loop is closed, and over the greater part of this period the instantaneous amplifier input resistance will be smaller than that indicated by Equation (7-4). Therefore, during the period when the loop is closed and the crystal unit can control the operation of the oscillator, the crystal unit is adequately terminated.

The effect of the pulsating crystal unit drive is not clear, but it is very possible that it degrades the performance of the crystal unit relative to when it is linearly loaded. However, this condition is almost inevitable in a series resonance transistor oscillator designed to accept a wide range of crystal equivalent resistance. One way of linearizing the amplifier input resistance would be to connect a physical resistor in parallel with the amplifier input. If its value was sufficiently small, the variation in total input resistance could then be appreciably reduced. This would result in the crystal unit operating under more linear conditions, but the loop would still open-circuit during each cycle of oscillation in essentially the same way, and the control period would remain practically constant. This approach has not been evaluated and it has been assumed that an adequate crystal unit termination during the time the loop is closed is sufficient. With this assumption the discussion of Paragraph 7-5 is valid.

7-8. Relative Values of Crystal Unit Dissipation and Oscillator Power Output

The voltage applied to the input of the crystal unit is also applied across r_t , the load reflected from the collector side of the impedance transforming network. r_t is representative of the oscillator load R_L and therefore has the same power dissipation. The oscillator output power is therefore:

$$P_L = \frac{V_{\max}^2}{r_t} \quad (7-22)$$

Substituting for V_{\max} from Equation (7-21) gives:

$$\frac{P_L}{P_{\text{CMAX}}} = \frac{R_r \max}{2 r_t} \quad (7-23)$$

Or, substituting for r_t from Equation (7-15):

$$\frac{P_L}{P_{C\text{MAX}}} = \frac{R_{r\text{ max}}}{2 A_{V_t}^2 \cdot R_L} \quad (7-24)$$

Figure 7-5 is a plot of Equation (7-24) for $K = 1$ and $K = 1.33$ as a function of A_{V_t} . These curves show the relative values of crystal unit maximum dissipation and the worst-case design oscillator output power, and indicate that the oscillator power output can only be appreciably greater than the crystal unit dissipation rating when A_{V_t} is less than 0.1. Reference to Figure 7-3 shows that the oscillator load R_L must then be greater than 14 to 20 $R_{r\text{ max}}$.

At the lower frequencies of this range where $R_{r\text{ max}}$ is relatively large, the oscillator load required to give an output power of more than 3 $P_{C\text{MAX}}$ will be of the order of 5 K or greater. This, in turn, will require a high breakdown voltage transistor because of the large collector voltage swing that will be encountered. For example, for a 30 MW power output at 800 KC, Figures 7-5 and 7-3 show that $A_{V_t} = 0.1$ and $R_L = 14$ ($K = 1$). At 800 KC, $R_{r\text{ max}} = 520$ ohms giving $R_L = 7.3$ K. To dissipate 30 MW in a 7.3 K load requires a collector signal voltage of 14.8 VRMS or 42 V peak-to-peak. Allowing for an increase in collector signal voltage due to loop gain change and power supply variation, the transistor breakdown voltage rating must be at least 50 volts and preferably 60 V. If a single supply voltage is used the applicable voltage rating will be BV_{CER} , the collector-to-emitter breakdown voltage rating with a total resistance R between base and emitter. Transistor types with BV_{CER} ratings of more than 60 V together with suitable high-frequency characteristics are costly at the present time, and this example probably approaches the economically feasible limit, particularly when higher power output can be obtained with less expensive transistors using the Pierce oscillator at these frequencies. At higher frequencies, the power output limitations are less severe due to the much lower values of $R_{r\text{ max}}$.

Quite often high oscillator output power is not required, and the values of A_{V_t} and R_L can then be selected from considerations of transistor type, desirable biasing levels, etc.

7-9. DESIGN PROCEDURE FOR SERIES RESONANCE TRANSISTOR OSCILLATORS, 800 KC TO 30 MC

7-10. Step 1, Selection of Crystal Unit Type

In this frequency range, crystal units with frequency tolerances of ± 0.005 and ± 0.0025 percent are available with dissipation ratings of 10 MW up to 10 MC and 5 MW above 10 MC. There is also an overlap in the 17- to 20-MC range

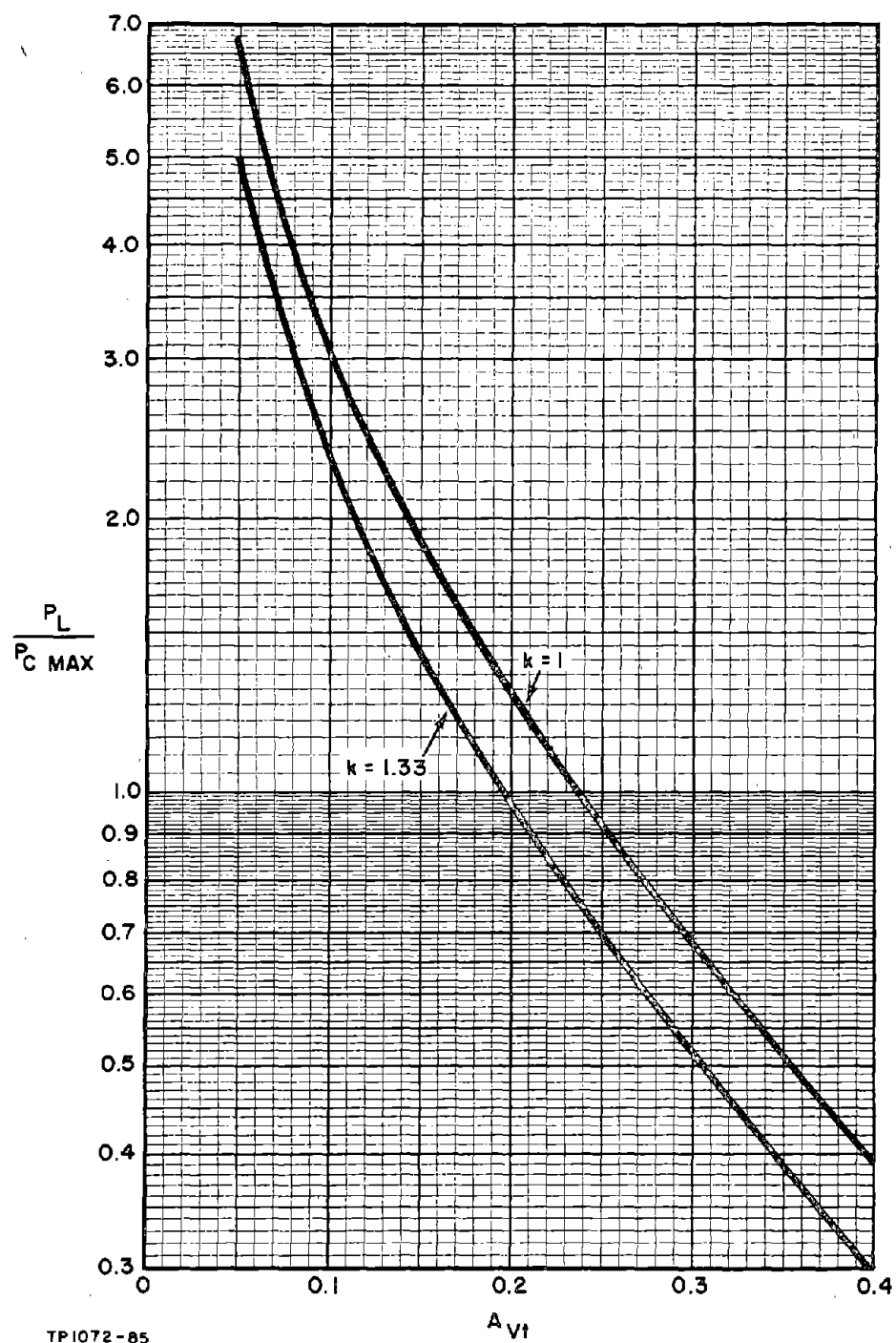


Figure 7-5. Oscillator Power Output Relative to Crystal Unit Dissipation Rating

where overtone crystal units with frequency tolerances of 0.005 to 0.002 percent are available with dissipation ratings of 2 MW. The latter types complete the coverage to 30 MC.

The selection of a crystal unit type will be governed by the overall oscillator frequency tolerance desired. If a large number of oscillators are to be constructed, the in-service overall oscillator tolerance can be expected to be at least ± 5 PPM wider than that of the crystal unit unless special precautions are taken. In the overlap region where a choice of crystal unit dissipation rating is available, this may also form a basis for selection, depending on the oscillator output power desired.

7-11. Step 2, Design Feasibility

The feasibility of the design using the selected crystal unit at the desired oscillator output power level can be determined from Figures 7-3 and 7-5. The maximum value of Av_t allowed by crystal unit dissipation considerations is determined from Figure 7-5 for the known values of desired output power and crystal dissipation rating. This value of Av_t is then found on the curves of Figure 7-3 to find R_L .

There may be some uncertainty at this stage as to which K value applies, and values of R_L should be determined for each value of K. The collector signal voltage required to give the desired power output is:

$$V_C = \sqrt{P_L \cdot R_L} \quad (7-25)$$

and the collector-emitter bias voltage is then:

$$V_{CE} \approx 1.4 V_C \quad (7-26)$$

The required collector bias current is approximately given by:

$$I_C = \frac{V_{CE}}{R_T} \quad (7-27)$$

where R_T is given in Figure 7-3 for the particular value of Av_t . Some allowance should be made for the collector circuit tuning coil losses which will decrease R_T and increase the required collector bias current. The value of I_C calculated from Equation (7-27) is the minimum value and may be increased if necessary to decrease the amplifier input resistance. This may be desirable in the 10- to 20-MC region where $R_{r \max}$ is small for certain crystal units.

It is now necessary to tentatively select a transistor type on the basis of the preceding discussion or, alternatively to assume a minimum value of transistor h_{FE} . The input resistance is then calculated as follows:

$$I_E \approx I_C \quad (7-28)$$

$$r_e = \frac{25}{I_E} + r' \quad (7-29)$$

(In the absence of specific information regarding the value of the emitter ohmic resistance r' , assume a value of 1 ohm.)

Then:

$$R_{in(s)} = r_e + r_{bb'} (1 - \alpha_o) \quad (7-30)$$

and:

$$K = 1 + \frac{R_{in(s)}}{R_{r\max}} \quad (7-31)$$

If K is not less than or approximately equal to 1.33, a larger value of collector bias current must be assumed and $R_{in(s)}$ recalculated until this condition is satisfied. The K value arrived at will determine which set of R_L , A_{Vt} , V_{CE} , and I_C values obtained in the parallel calculation apply.

The values of V_{CE} and I_C finally obtained determine the feasibility of the design. The power supply voltage available must be higher than V_{CE} , preferably by at least 2 volts to allow for adequate transistor biasing, and the transistor power dissipation and breakdown voltage ratings must be larger than $V_{CE} \cdot I_C$ and $2 V_{CE}$, respectively. The design may be practically feasible in the sense that suitable transistors are obtainable but economically unfeasible because of the high transistor cost.

7-12. Step 3, Selection of Transistor Type

The transistor type is selected as follows:

- (a) The transistor power dissipation rating required at the highest working temperature is calculated from:

$$P_{D\max} > V_{CE} \cdot I_C \quad (7-32)$$

Variations in power supply voltage will increase both V_{CE} and I_C , and an appropriate allowance should be made taking into account the stability of the supply.

- (b) The transistor gain-bandwidth product at the calculated bias levels should be ten times the design frequency and preferably larger to maintain the validity of the assumption that the amplifier voltage gain is independent of frequency. The discussion of transistor amplifier voltage gain behavior given in Paragraphs 3-14 to 3-18 should be helpful in this respect.
- (c) The transistor breakdown voltage rating must be at least twice the highest collector voltage peak-to-peak swing. For single voltage supply biasing, the applicable transistor breakdown voltage rating is BVC_{ER} , the rating with a total resistance of R between emitter and base.
- (d) The transistor minimum h_{FE} will normally only be important in the 6- to 20-MC range where $R_r \text{ max}$ is 20 ohms or less. A low value of minimum h_{FE} may then require the emitter current to be higher than that necessary to supply the output power in order to decrease r_e sufficiently to meet the maximum resistance condition on $R_{in(s)}$. The amplifier input resistance component due to $r_{bb}' (1 - \alpha_o)$ may then be appreciable if $h_{FE \text{ min}}$ is small.

7-13. Step 4, Calculation of Remaining Oscillator Circuit Components

- (a) Impedance transforming network

The impedance transformer secondary load is:

$$r_s = R_{in(s)} + R_r \text{ max} \quad (7-33)$$

The required voltage attenuation ratio is A_{V_t} . Section 4 details the design procedure to be employed for various impedance transforming networks.

The collector tank circuit is designed for the calculated impedance transforming network effective parallel primary reactance. The total amplifier load R_T consists of the external load R_L , the feedback circuit load R_{FB} , and the effective parallel resistance of the collector tank circuit inductance R_{LP} . R_{LP} has not yet been accounted for and may be sufficiently small to reduce R_T and hence the loop gain by an appreciable amount. This can be determined by measuring R_{LP} or by assuming a coil Q and using the formula:

$$R_{LP} = Q \cdot X_L \quad (7-34)$$

If R_{LP} is not negligibly large compared to R_T , then R_L must be increased to offset the additional amplifier loading. The actual R_L is then:

$$\text{Actual } R_L = \frac{R'_L \cdot R_{LP}}{R_{LP} - R'_L} \quad (7-35)$$

where R'_L is the value of R_L calculated in Step 2.

(b) Transistor Biasing

It is desirable if possible that the emitter-to-ground voltage should be at least 3 VDC to provide wide temperature range transistor bias stability. The base-biasing network current should preferably be greater than 5 times the 25-degree Centigrade base current of a transistor with the minimum h_{FE} . If minimum biasing current is desired, the base biasing network can be calculated as detailed in Paragraph 3-26.

The reactance of the base decoupling capacitor C_B should be small compared to the base parallel input resistance. At the crystal resonance frequency, the base parallel input-resistance is that of a common-emitter amplifier with emitter degeneration. This subject is discussed in Paragraphs 3-20 and 3-24. For the values of crystal resonance resistance likely to be encountered, the base input resistance may vary from several kilohms at frequencies below 3 or 4 MC to 100 ohms at 20 MC. It is not considered worthwhile to attempt to calculate C_B accurately, since it can readily be experimentally adjusted during the breadboard stage. A preliminary estimate can be obtained using the formula:

$$R_{in(p)} = (r_e + \frac{R_{r \max}}{9}) h_{FE \min} \quad (7-36)$$

X_{C_B} should be less than one-tenth of $R_{in(p)}$ to provide adequate decoupling.

7-14. DESIGN EXAMPLES

7-15. 1 MC, 2N706A Series Resonance Oscillator

Oscillator Requirements:

Overall Frequency Tolerance: ± 70 PPM

Output Power: 4 MW

For a CR-19A/U Crystal Unit:

$$P_{C\text{MAX}} = 10 \text{ MW}$$

$$R_{r \text{ max}} = 440 \text{ ohms}$$

Because of the large value of $R_{r \text{ max}}$, K will be approximately 1.

From Figure 7-5 for $K = 1$, $A_{V_t} \leq 0.4$.

Selecting a value of:

$$A_{V_t} = 0.1$$

From Figure 7-3:

$$R_L = 7.2 \text{ K}$$

$$R_T = 6.2 \text{ K}$$

$$V_C = 5.4 \text{ VRMS}$$

$$V_{CE} = 7.5 \text{ V}$$

$$I_C = 1.2 \text{ MA}$$

A 2N706A transistor is selected for this design.

Its characteristics are:

$$\text{Power dissipation at } 105^\circ\text{C} = 140 \text{ MW}$$

$$BV_{CEO} = 15 \text{ VDC}$$

$$h_{FE\text{min}} (\text{at } 1 \text{ MA}) \approx 10$$

$$\text{Typical } f_T \approx 150 \text{ MC}$$

$$I_E \approx 1.4 \text{ MA}$$

$$r_e \approx 19 \text{ ohms}$$

$$R_{in(s)} \approx 25 \text{ ohms}$$

$$K \approx 1.06$$

Using a capacitive divider impedance transformer:

$$\frac{C_1 + C_2}{C_1} = \frac{1}{A_{V_t}}$$

or

$$\frac{C_2}{C_1} = 9$$

$$r_s = 465 \text{ ohms}$$

$$\text{Let } X_{C2} \approx \frac{r_s}{5} \approx 89 \text{ ohms}$$

Then:

$$C_2 = 1800 \text{ PF}$$

$$C_1 = 200 \text{ PF}$$

$$X_C = 890 \text{ ohms}$$

The tuning inductance required is then:

$$L = \frac{X_C}{\omega} = 140 \text{ UH}$$

$R_{LP} \approx 90 \text{ K}$ for a Q of 100 and can be ignored.

For a 10 VDC supply, the emitter-to-ground voltage is approximately 2.5 VDC. The emitter resistor is then 1.8 K. The maximum base current is approximately 0.15 MA, and suitable base-biasing resistor values are 2.4 K and 6.2 K.

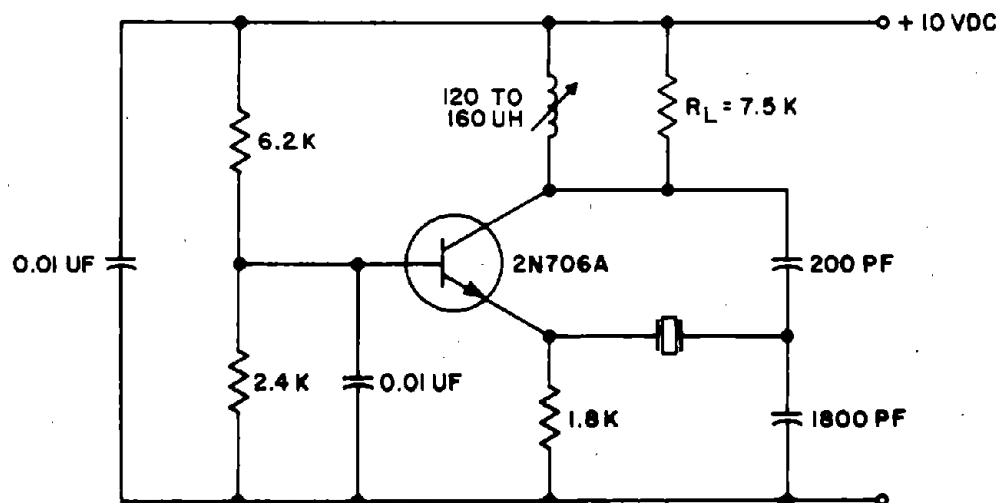
The base input resistance is approximately 4.7 K, and X_{CB} should be 470 ohms or less. A C_B of 0.01 UF is adequate.

DESIGN EVALUATION DATA
1 MC, 2N706A SERIES RESONANCE OSCILLATOR

Crystal Units CR-19A/U	Resonance Frequency (MC)	R_r (ohms)
1	0.999990	180
2	0.999987	150
3	0.999993	170
4	0.999993	440
(Number 3 + 270 ohms)		

DESIGN EVALUATION DATA FOR 1 MC, 2N706A SERIES RESONANCE
OSCILLATOR (ALL RESULTS OBTAINED USING LIMIT CRYSTAL)

Effect of		Change
+15% B+ Change on Oscillator	Frequency V_O	<1 PPM +16%
-20% B+ Change on Oscillator	Frequency V_O	<1 PPM -20%
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_O	<1 PPM $\pm 3\%$
-55°C to +105°C Change in T_a on Oscillator	Frequency V_O	± 20 PPM $\pm 7\%$
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		± 3 PPM
Transistor Interchange (8 units, retuning to maximum output)	Frequency V_O	<1 PPM < $\pm 2\%$
Crystal Unit Interchange	Frequency Miscorrelation V_O	± 2 PPM $\pm 4\%$



TP1072-132

Figure 7-6. 1-MC, 2N706A Series Resonance Oscillator,
Schematic Diagram

7-16. 5 MC, 2N706A Series Resonance Oscillator

Oscillator Requirements:

Overall Frequency Tolerance: ± 70 PPM

Output Power: 25 MW

For a CR-19A/U crystal unit:

$$P_{\text{CMAX}} = 10 \text{ MW}$$

$$R_{\text{r max}} = 37 \text{ ohms}$$

From Figure 7-5 for:

$$\underline{K = 1}$$

$$A_{Vt} \leq 0.12$$

$$\underline{K = 1.33}$$

$$A_{Vt} \leq 0.09$$

From Figure 7-3 for:

$$\underline{K = 1}$$

$$R_L \geq 520 \text{ ohms}$$

$$R_T \geq 430 \text{ ohms}$$

$$\underline{K = 1.33}$$

$$R_L \geq 890 \text{ ohms}$$

$$R_T \geq 780 \text{ ohms}$$

The collector signal voltage is:

$$\underline{K = 1}$$

$$V_C = 3.6 \text{ VRMS}$$

$$\underline{K = 1.33}$$

$$V_C = 4.7 \text{ VRMS}$$

Collector-emitter bias voltage and current:

$$\underline{K = 1}$$

$$V_{\text{CE}} = 5.1 \text{ VDC}$$

$$I_C = 12 \text{ MADC}$$

$$\underline{K = 1.33}$$

$$V_{\text{CE}} = 6.7 \text{ VDC}$$

$$I_C = 9 \text{ MA}$$

A 2N706A transistor will be suitable for this design. Its characteristics are:

$$\text{Power Dissipation at } 105^\circ\text{C} = 140 \text{ MW}$$

$$BV_{CEO} = 15 \text{ VDC}$$

$$h_{FEmin} \text{ (at 5 MA)} \approx 20$$

$$\text{Typical } f_T \approx 300 \text{ MC}$$

Then:

$$r_e \approx 3 \text{ ohms}$$

$$R_{in(s)} \approx 6 \text{ ohms}$$

$$K = 1.2$$

$$\text{Use } K = 1.33 \text{ values}$$

Using a capacitive divider impedance transformer:

$$\frac{C_1 + C_2}{C_1} = \frac{1}{A_{V_t}}$$

or

$$\frac{C_2}{C_1} = 10$$

$$r_s = 43 \text{ ohms}$$

$$\text{Let } X_{C2} \approx \frac{r_s}{5} \approx 9 \text{ ohms}$$

then

$$C_2 = 3600 \text{ PF}$$

$$C_1 = 360 \text{ PF}$$

$$X_C = 100 \text{ ohms}$$

The tuning inductance required is then:

$$L = \frac{X_C}{\omega} = 3.2 \text{ UH}$$

$$R_{LP} \approx 10 \text{ K for a } Q \text{ of } 100 \text{ and can be ignored.}$$

$$\text{Maximum } I_b \approx 0.5 \text{ MA}$$

For a 10 VDC supply, the emitter-to-ground voltage is approximately 3 VDC. The emitter resistor is then 330 ohms. Suitable base-biasing resistor values are then 2.7 K and 1.8 K.

The base input resistance is approximately 200 ohms minimum, and X_{CB} should be 20 or less. A C_B of 0.01 UF is adequate.

DESIGN EVALUATION DATA
5 MC, 2N706A SERIES RESONANCE OSCILLATOR

Crystal Units CR-19A/U	Resonance Frequency (MC)	R_r (ohms)
1	4.999941	12
2	4.999931	11
3	4.999932	23
4	4.999967	20
5 (Number 4 + 15 ohms)	4.999963	37

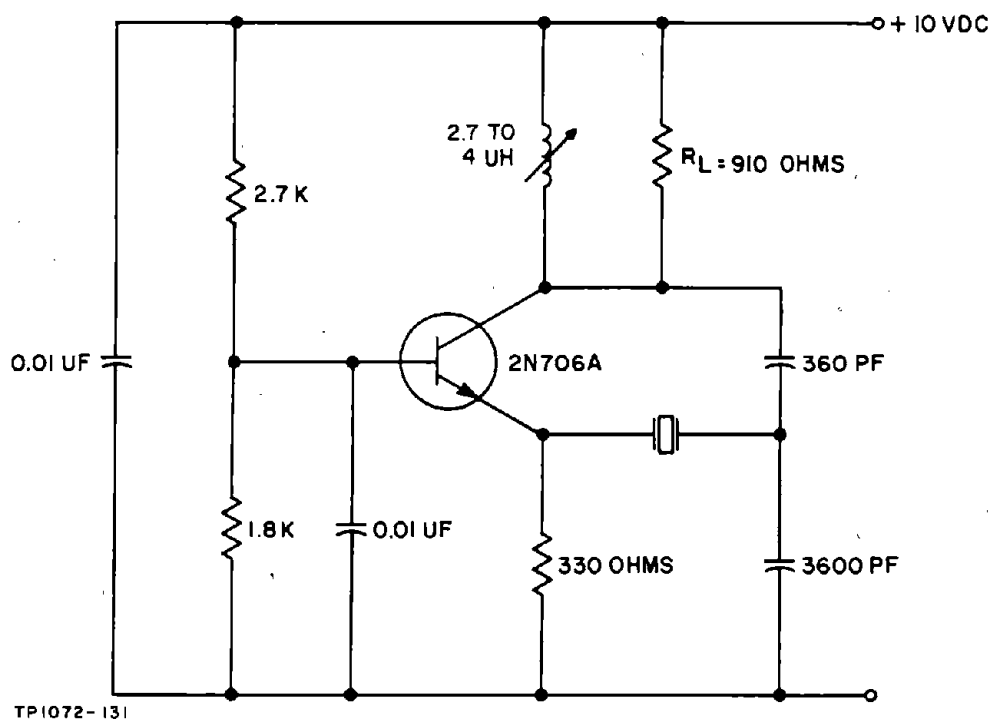


Figure 7-7. 5-MC, 2N706A Series Resonance Oscillator,
Schematic Diagram

DESIGN EVALUATION DATA FOR 5 MC, 2N706A SERIES RESONANCE
OSCILLATOR (All Results Obtained Using Limit Crystal)

Effect of		Change
+15% B+ Change on Oscillator	Frequency V_o	<1 PPM +18%
-20% B+ Change on Oscillator	Frequency V_o	<1 PPM -23%
±10% Change in R_L on Oscillator	Frequency V_o	<1 PPM ± 5%
-55°C to +105°C Change in T_a on Oscillator	Frequency V_o	±23 PPM ±10%
Contribution of Oscillator Circuit to Frequency Deviations in Tem- perature Test		<±3%
Transistor Interchange (8 units, retuning to maximum output)	Frequency V_o	<1 PPM <±2%
Crystal Unit Interchange	Frequency Miscorrelation V_o	±4 PPM ±5%

7-17. 20 MC, 2N706A Series Resonance Oscillator

Oscillator Requirements:

Overall Frequency Tolerance: ±70 PPM

Output Power: 20 MW

For a CR-19A/U crystal unit:

$P_{C\text{MAX}} = 5 \text{ MW}$

$R_r \text{ max} = 15 \text{ ohms}$

From Figure 7-5 for:

$$\underline{K = 1}$$

$$AV_t \leq 0.08$$

$$\underline{K = 1.33}$$

$$AV_t \leq 0.06$$

From Figure 7-3 for:

$$\underline{K = 1}$$

$$R_L = 300 \text{ ohms}$$

$$R_T = 270 \text{ ohms}$$

$$V_C = 2.5 \text{ VRMS}$$

$$V_{CE} = 3.5 \text{ VDC}$$

$$I_C = 13 \text{ MA}$$

$$\underline{K = 1.33}$$

$$R_L = 510 \text{ ohms}$$

$$R_T = 470 \text{ ohms}$$

$$V_C = 3.2 \text{ VRMS}$$

$$V_{CE} = 4.5$$

$$I_C = 10 \text{ MA}$$

A 2N706A transistor is selected for this design. Its characteristics are:

$$\text{Power dissipation at } 105^\circ\text{C} = 140 \text{ MW}$$

$$BV_{CEO} = 15 \text{ VDC}$$

$$h_{FE\min} \approx 20$$

$$\text{Typical } f_T \approx 300 \text{ MC}$$

For

$$\underline{K = 1}$$

$$I_E \approx 14 \text{ MA}$$

$$r_e \approx 2.5 \text{ ohms}$$

$$R_{in(s)} \approx 5.5 \text{ ohms}$$

$$\underline{K = 1.33}$$

$$I_E \approx 11 \text{ MA}$$

$$r_e \approx 3 \text{ ohms}$$

$$R_{in(s)} \approx 6 \text{ ohms}$$

K is approximately 1.4, and the values calculated for K = 1.33 must be used.

Using a capacitive divider impedance transformer:

$$\frac{C_2}{C_1} = \frac{1}{AV_t} - 1 = 15.5$$

$$r_s = 21 \text{ ohms}$$

$$\text{Let } X_{C2} \approx \frac{r_s}{5} = 4 \text{ ohms}$$

Then

$$C_2 = 2000 \text{ PF}$$

$$C_1 = 130 \text{ PF}$$

$$X_C = 66 \text{ ohms}$$

$$L = 0.5 \text{ UH}$$

$R_{LP} \approx 6.6 \text{ K}$ for a Q of 100 and can be ignored.

For a 10 VDC supply, the emitter-to-ground voltage is approximately 5.5 VDC. The emitter resistor is then 510 ohms. The maximum base current is approximately 0.5 MA, and suitable biasing resistor values are 3 K and 1.6 K.

The base input resistance is approximately 400 ohms, and X_{CB} should be 40 ohms or less. A C_B of 1000 PF is adequate.

DESIGN EVALUATION DATA
20 MC, 2N706A SERIES RESONANCE OSCILLATOR

Crystal Units CR-19A/U	Resonance Frequency (MC)	R (ohms)
1	20.00060	4.5
2	20.00031	5
3	20.00068	5.5
4	20.00027	5
5	20.00009	15
(Number 4 + 10 ohms)		

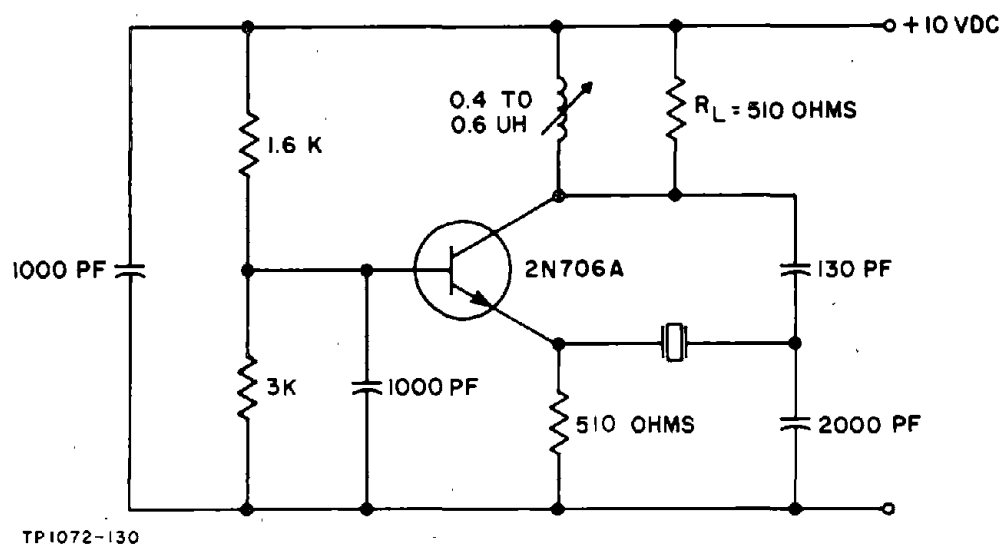


Figure 7-8. 20 MC, 2N706A Series Resonance Oscillator, Schematic Diagram

DESIGN EVALUATION DATA FOR 20 MC, 2N706A SERIES RESONANCE OSCILLATOR (All Results Obtained Using Limit Crystal)

Effect of		Change
+15% B+ Change on Oscillator	Frequency V_o	<1 PPM +13%
-20% B+ Change on Oscillator	Frequency V_o	1 PPM -20%
±10% Change in R_L on Oscillator	Frequency V_o	<1 PPM ± 7%
-55°C to +105°C Change in T_a on Oscillator	Frequency V_o	±25 PPM ± 5%
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		± 3 PPM
Transistor Interchange (5 units, retuning to maximum output)	Frequency V_o	± 2 PPM ± 3%
Crystal Unit Interchange	Frequency Miscorrelation V_o	± 4 PPM ±10%

7-18. TRANSISTOR SERIES OSCILLATORS ABOVE 30 MC

The same oscillator configuration used below 30 MC is still valid above 30 MC. However, a change of design approach is required above 30 to 50 MC, depending on the type of transistor to be used, due to the complex behavior of the amplifier characteristics at these higher frequencies. Using transistors with typical current gain-bandwidth products of 700 or larger, it should be practicable to apply the design procedure described for use below 30 MC at frequencies up to 50 or perhaps 60 MC with a fair degree of design accuracy. But for transistor types having current gain-bandwidth products of 300 or less, 30 MC will probably be the highest frequency at which those methods can be profitably employed.

The major problem is that of estimating with sufficient accuracy the voltage gain and input impedance of the amplifier. For most types of transistors, little or no information is contained in the data sheets which is of any help in this respect. However, for several of the very high frequency types, graphs of the transistor admittance parameters are presented. These, though, are normally given for the common emitter configuration, and a time consuming calculation is required before a transformation to the required common base admittance parameters is obtained. A further calculation is then required before an amplifier characterization for one operating condition is achieved.

An alternative to confining attention to only those transistor types for which detailed data of this kind are available is to measure the amplifier characteristics. This method is presumably as accurate as the process described above, is also probably less time consuming, and has the great advantage of increasing the number of transistor types which can be considered for use.

This is the method of amplifier characterization selected for use in this frequency range. It entails using an impedance measuring bridge as an amplifier signal source so that the amplifier input impedance can be measured for various load conditions. At the same time amplifier input and output voltage measurements are made from which the voltage gain can be calculated.

In all other respects the oscillator design process is similar to that described for use below 30 MC.

7-19. Crystal Unit Characteristics

Table 7-2 gives the major characteristics of the military standard series resonance crystal units in the frequency range from below 30 MC to 125 MC. More detailed specifications are given in MIL-C-3098, Supplement 1. There are no military standard crystal units for the frequency range from 125 MC to 200 MC,

TABLE 7-2. MILITARY STANDARD SERIES RESONANCE CRYSTAL UNITS, 10 MC TO 200 MC

Frequency Range (MC)	Operating Temperature Range (°C)	Frequency Tolerance (± Percent)	Rated Drive (MW)	Maximum Resonance Resistance (ohms)	Crystal Unit Type	Holder Type
WIDE TEMPERATURE RANGE CRYSTAL UNITS						
35 to 50	-55 to +105	0.005	20	60	CR-73/U	HC-6/U
* 50 to 87		0.005	2	50 and 60	CR-53A/U	HC-6/U
50 to 125		0.005	2	50 and 60	CR-54A/U	HC-18/U
50 to 125		0.002	2	50 and 60	CR-56A/U	HC-18/U
50 to 125		0.005	2	50 and 60	CR-80/U	HC-25/U
50 to 125		0.002	2	50 and 60	CR-82/U	HC-25/U
125 to 200	-55 to +105	0.005	2	80 to 100	CR-83/U Similar to CR-54A/U, CR-56A/U, CR-80/U, CR-82/U, or CR-83/U	HC-25/U
TEMPERATURE CONTROLLED CRYSTAL UNITS						
10 to 61	70 to 80	0.001	2 and 1	60 and 40	CR-65/U	HC-6/U
10 to 75	70 to 80	0.002	2 and 1	60 and 40	CR-32A/U	HC-6/U
17 to 61	80 to 90	0.002	2 and 1	40	CR-61/U	HC-18/U
17 to 61	80 to 90	0.002	2 and 1	40	CR-84/U	HC-25/U
50 to 125	80 to 90	0.002	1	50 and 60	CR-59A/U	HC-18/U
50 to 125	70 to 80	0.001	1	40	CR-75/U	HC-6/U

* Special Application

NOTE: Refer to Table 7-1 for other crystal units applicable from 30 to 61 MC.

but crystal units can be purchased in this range that meet the specifications of the CR-54A/U, CR-56A/U, CR-80/U, CR-82/U, or CR-85/U types, except that the maximum series resonance resistance may increase to 80 or 100 ohms.

The maximum resonance resistance of crystal units therefore lies in the range of 40 to 100 ohms in the 30 to 200 MC frequency range. The actual range of resonance resistance which will be encountered for large groups of crystals of the same type and frequency will probably be $R_{r \text{ max}}$ to $1/4 R_{r \text{ max}}$ below 60 MC and $R_{r \text{ max}}$ to $1/3 R_{r \text{ max}}$ above 60 MC.

For these crystal unit types, the crystal unit shunt capacitance C_0 is below 7 PF and is of little importance insofar as oscillator design is concerned below 100 MC. Above 100 MC, however, this capacitance can degrade the crystal unit phase-shifting capability since the ratio of X_{C_0} to R_1 is then small. The reactance of a 7 PF capacitance varies from 230 ohms at 100 MC to 114 ohms at 200 MC, while the crystal series arm resistance may, in the worst case, be 60 ohms at 100 MC and 100 ohms at 200 MC.

The ratio of X_{C_0} to R_1 , therefore, lies in the range of 1 to 5. The analysis of Paragraph 1-4 shows that the crystal unit phase-shifting capability is severely degraded when this ratio is less than 3. At frequencies above 100 MC, therefore, this condition is either being approached or exceeded, and to prevent excessive degradation of the crystal unit phase-shifting capability, it is necessary to neutralize C_0 . This is achieved by connecting an inductor, which resonates with C_0 at the crystal unit frequency, in parallel with the crystal unit. The value of C_0 at the operating frequency can vary appreciably from the value measured at low frequencies, and to obtain maximum effect C_0 should be determined at a frequency close to the operating frequency, but sufficiently lower that the motional arm of the crystal unit has a negligible effect on the measurement. A frequency 5 to 10 percent below the operating frequency is usually satisfactory.

Complete cancellation of C_0 is not essential since the object is simply to increase the parallel capacitive reactance to a value such that $\frac{X_{C_0}}{R_1}$ for a worst-case crystal will be larger than, say, 5. Therefore, an inductance which resonates with the typical value of C_0 at the operating frequency will suffice for all crystal units of the particular type.

The Q of the inductor should be sufficiently large that its effective parallel resistance is at least 10 times the crystal unit series resonance resistance to avoid a degradation of the crystal unit phase shifting capability due to this cause. This is not a demanding requirement considering the low value of R_1 at these frequencies, and frequently the inductor is constructed in the form of a closely

spaced single-layer coil wound on a 1/2 watt carbon resistor of 3 to 10 K nominal value. At all frequencies below 100 MC the ratio of X_{C_0} to R_1 is sufficiently large that it is unnecessary to neutralize the crystal unit shunt capacitance.

Since the shunt capacitance is neutralized above 100 MC, the crystal operates at the motional arm resonance frequency f_s and the resistance of the crystal at this frequency is the motional arm resistance R_1 . To avoid having to refer to both R_T and R_1 and f_T and f_s in the following discussion, these distinctions will be ignored and the discussion will in general be presented in terms of R_T and f_T . It should be understood, however, that when applied to designs above 100 MC, R_1 and f_s are the appropriate crystal characteristics.

7-20. Amplifier Characteristics

The behavior of the voltage gain and emitter input impedance of a grounded base transistor amplifier in this frequency range is discussed in Paragraph 3-14. Briefly reviewing, it is shown there that above 30 MC for any particular value of load resistance, the voltage gain of a tuned amplifier is frequency dependent, decreasing at a rate of from 12 to 16 DB per decade, depending on transistor type and load level. Increasing the load resistance tends to cause a more rapid decrease of voltage gain, with the result that the voltage gain is no longer linearly related to the load resistance. However, at the low levels of load resistance suitable for oscillator service, this effect is not excessive. To illustrate this, Table 7-3 gives values of voltage gain at 100 MC relative to amplifier load resistance for various types of transistors, roughly indicating the pattern of gain fall-off.

TABLE 7-3. TUNED VOLTAGE GAIN VERSUS R_T

R_T (ohms)	Voltage Gain ($I_E = 10$ MA)		
	2N706A	2N2219	2N2708/2N917
50	3.2	3.2	3.2
200	10	10	11
500	20	16	25
1000	27	20	35

Above 30 MC, the amplifier input impedance behavior as a function of frequency is quite complex. The series resistive component is approaching the region where a peak value occurs, which is then followed by a rapid decrease, finally approaching zero in the frequency range of 60 to 200 MC, depending on

transistor type, bias level, and load resistance. The series input inductive reactance as a function of frequency appears to increase almost coincidentally with the series resistive component up to the region of the resistance peak. And above the peak it increases rapidly relative to the resistive component. From immediately above the frequency of peak series resistance, the amplifier input impedance is essentially inductive.

Above 20 MC the amplifier develops a large phase lag which reaches a value of 45 to 70 degrees in the region of 60 MC, but which does not, judging by oscillator performance, exceed a value of 90 degrees below 200 MC.

7-21. Attenuation of Feedback Signal Between Crystal Unit Input and Amplifier Input Points

When the behavior of the amplifier input resistance is considered in relation to the crystal unit, the equivalent circuit at the crystal unit frequency is of the form shown in Figure 7-9 (b), or transforming to parallel components, as in Figure 7-9 (c). Designating the amplifier input impedance as Z_{in} , the relationship between V_1 and V_2 is then:

$$A_{VC} = \frac{V_2}{V_1} = \frac{Z_{in}}{Z_{in} + R_{r \max}} \quad (7-37)$$

where

$$Z_{in} = r_{in(s)} + j\omega L(s) = \frac{j\omega L(p)}{1 + j\omega L(p)/R_{in}} \quad (7-38)$$

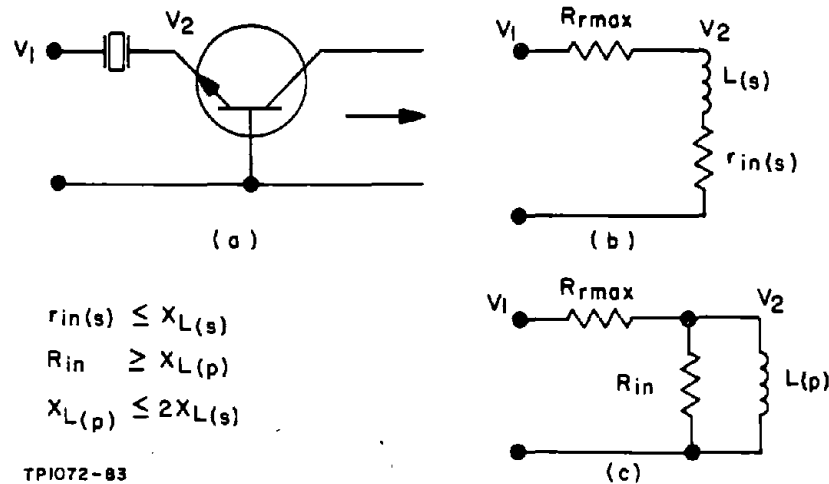


Figure 7-9. Equivalent Circuit of Crystal Unit and Amplifier Input

Considering the case of parallel input components, the attenuation is then:

$$A_{VC} = \frac{j\omega L(p)}{R_{r \max} + j\omega L(p) \left[1 + R_{r \max}/R_{in} \right]} \quad (7-39)$$

and:

$$\left| A_{VC} \right| = \frac{\omega L(p)}{R_{r \max} \sqrt{1 + \left[\frac{\omega L(p)}{R_{r \max}} \left(1 + \frac{R_{r \max}}{R_{in}} \right) \right]^2}} \quad (7-40)$$

In many cases, $\omega L(p) \ll R_{r \max}$ and $R_{in} \gg R_{r \max}$, and then:

$$\left| A_{VC} \right| \approx \frac{\omega L(p)}{R_{r \max}} \quad (7-41)$$

In practice, this does not appear to give a good estimate of the attenuation. It was found that the actual attenuation occurring between the crystal unit input and the amplifier input lies somewhere between the value given by Equation (7-40) and that which would be obtained if the inductive component in Figure 7-9 (c) was absent. That is:

$$A_{VC} \approx \frac{R_{in}}{R_{in} + R_{r \max}} \quad (7-42)$$

No satisfactory explanation has been found for this effect. One possible explanation is that the increase in effective emitter resistance due to the addition of $R_{r \max}$ in series with the emitter causes a change in the distribution of the feedback currents between the base and emitter paths, thereby increasing $L(p)$.

Oscillation can usually be obtained when calculating the loop gain on the basis of the attenuation given by Equation (7-42), but it will then usually be necessary to increase the loop gain to obtain satisfactory oscillator performance when subjected to external variables. A value of voltage attenuation mid-way between the two values given by Equations (7-40) and (7-42) seems to be a suitable choice.

7-22. Loop Voltage Gain Relationships

The loop voltage gain of the oscillator is conveniently divided into three factors. Referring to Figure 7-10, these are:

- (a) The voltage gain G_V from the emitter to the collector of the transistor.

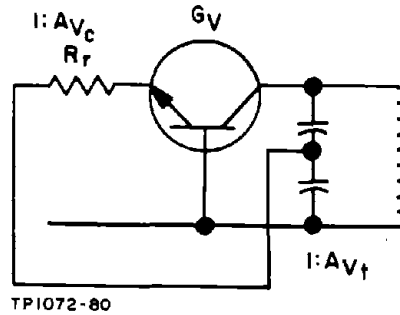


Figure 7-10. Oscillator Loop Voltage Gain Relationships

- (b) The voltage ratio A_{V_t} of the impedance transforming network between the transistor collector and the crystal unit input terminal.
- (c) The voltage attenuation A_{V_c} occurring between the crystal unit input terminal and the transistor emitter.

The loop voltage gain G_{V_L} is then given by:

$$G_{V_L} = G_V \cdot A_{V_t} \cdot A_{V_c} \quad (7-43)$$

A loop voltage gain of 1.4 is usually suitable for a worst-case design giving:

$$A_{V_t} = \frac{1.4}{G_V \cdot A_{V_c}} \quad (7-44)$$

G_V and A_{V_c} are obtained from the amplifier measuring process and the known value of $R_{r \max}$, enabling the impedance transforming network voltage ratio to be calculated.

The amplifier loading due to the feedback circuit, neglecting losses, is then:

$$R_{FB} = \frac{R_{r \max} + R_{in}}{A_{V_t}^2} \quad (7-45)$$

7-23. Crystal Unit Power Dissipation

The signal voltage at the input terminal of the crystal unit V_{\max} has to be limited to a specific value to prevent crystal unit overdrive. This in turn indirectly determines the maximum value of the collector signal voltage $V_{o \max}$. The two are related by the voltage ratio A_{V_t} of the impedance matching transformer

connected between the collector and the crystal unit as:

$$V_{o \max} = \frac{V_{\max}}{A_v} \quad (7-46)$$

V_{\max} is also a function of the load impedance at the output side of the crystal unit which is, in this case, the amplifier input impedance. The complex nature of the amplifier input impedance at small signal levels has already been described, and a further increase in complexity occurs when the amplifier is subjected to a high input signal level of the order of that expected in oscillator service. This will be far larger than the "linear" region of the emitter-base diode characteristic, and a large but apparently unpredictable increase in the amplifier input impedance can be expected. Because of this it is difficult to develop an equation for V_{\max} which will ensure that crystal overdrive does not occur but which is not so stringent as to place needless restraints on the design.

Judging by experimental results, it appears that a suitable limit to apply to the crystal unit input voltage is approximately twice that permitted across a worst-case crystal unit. That is:

$$V_{\max} \approx 2\sqrt{P_{C\max} \cdot R_{r \max}} \quad (7-47)$$

Applying Equation (7-47) for the various values of $R_{r \max}$ gives the values of V_{\max} shown in Table 7-4. These should only be used as a rough guide to the permissible value of V_{\max} , and when finalizing the design measurements of the voltage across the crystal unit, should be made to determine the crystal dissipation. This approach may lead to erroneous results, however, if the voltage across the crystal unit is estimated from the input and output terminal voltages relative to ground because of the large phase difference of these signals.

TABLE 7-4. PERMISSIBLE CRYSTAL UNIT INPUT VOLTAGE

$R_{r \max}$ (ohms)	V_{\max} (RMS)
40	0.56
50	0.64
60	0.7
100	0.9

7-24. Crystal Unit Terminating Resistance Level

To prevent degradation of the crystal unit phase-shifting capabilities, the terminating resistance levels on either side of the crystal unit should be low compared to the maximum crystal unit resonance resistance. One of these terminating resistances is the amplifier series input resistance, and reference to the plots of Figure 3-13(a) to (d) shows that, for the bias conditions indicated, $R_{in(s)}$ is much smaller than the values of $R_{r \max}$ appropriate to the various frequencies except possibly in the frequency region of 30 to 80 MC. In this frequency range $R_{in(s)}$ may be comparable with $R_{r \max}$ due to the peak of $R_{in(s)}$ in this region. While this is not in the worst case a very desirable terminating level, it will not cause a too drastic degradation of the crystal unit phase-shifting capabilities and can be considered satisfactory.

These are, of course, the small signal amplifier input resistance characteristics, and under the large signal conditions that occur in practice, it is difficult to interpret what the terminating level provided by the amplifier will be.

The other crystal unit termination is provided by the amplifier output resistance via the impedance transforming network. The amplifier output resistance is also difficult to estimate, but it is, at the least, smaller than the oscillator load R_L . If R_L is therefore assumed to be the amplifier output resistance, the crystal unit terminating resistance is $A_v^2 \cdot R_L$. This quantity is usually much less than $R_{r \max}$.

Both crystal unit terminating resistance levels therefore appear to be adequate in this oscillator configuration.

7-25. Oscillator Phase Relationships

Since this type of oscillator gives good correlation of crystal unit and oscillator frequencies without major corrective measures despite the large phase lag present in the amplifier, the mechanism by which this occurs is worth consideration. Low miscorrelation of oscillator and crystal unit frequencies implies that the net loop phase angle of the remainder of the circuit is approaching zero and therefore a compensation of the amplifier phase lag must be inherent in the circuit. It appears that this phase correction is obtained due to the action of the crystal unit in conjunction with the amplifier input impedance. Reference to Figure 7-9 (b) shows that, at the crystal unit resonance frequency, the phase angle of the amplifier input signal relative to the signal at the crystal unit input frequency is:

$$\theta = \tan^{-1} \frac{\omega L(s)}{R_{in(s)}} - \tan^{-1} \frac{\omega L(s)}{R_{r \max} + R_{in(s)}} \quad (7-48)$$

$R_{in}(s)$ is always smaller than $R_r \max + R_{in}(s)$ and at the higher frequencies is much smaller. Therefore, θ is a phase lead which is correspondingly small at low frequencies but gradually increases with frequency.

Judging by the small amounts of phase lead which had to be introduced in other ways into the circuit to obtain good frequency correlation, it appears that the compensation is almost complete for the range of resonance resistance values expected at the various frequencies. This leads to the conclusion that it is undesirable to connect a low impedance across the amplifier input, since this will tend to decrease the phase lead obtained at this point. The emitter DC current feedpath should therefore preferably be at least 10 times $X_{L(s)}$, a condition which will normally be automatically satisfied by the conditions imposed by transistor operating point stability with temperature variations. This also precludes the use of resistive loading of the amplifier input to decrease amplifier regeneration, leaving as the two alternatives either increased amplifier output loading or amplifier neutralization.

7-26. Amplifier Stability

The prevention of excessive regeneration within the amplifier is a major design factor at the higher frequencies. In its most severe form it results in uncontrolled oscillation at a frequency spaced some distance from the design frequency. In its mildest form amplifier regeneration can be detected as a peculiarity of the oscillator tuning action. As the collector circuit is tuned through the region of peak output signal, a dissymmetry of the signal voltage as a function of tuning will be noted. In severe cases, the action is quite abrupt, oscillation ceasing immediately when peak output is past. Furthermore, when retuning in the other direction to restart oscillation, it is necessary to tune past the point where peak output was previously obtained before oscillation recommences.

The severity of this effect is an indication of the relative stability of the amplifier, and in a satisfactory oscillator it should be possible to tune smoothly through the region of peak collector signal voltage. If this is not the case, the circuit should be redesigned. If the power output requirement is small, operating the amplifier at a lower collector load resistance level will usually result in a cure, but if high output power is desired this may not always be a suitable remedy since reducing R_T frequently reduces the output power. Another possibility then is to neutralize the amplifier by means of an inductor in parallel with the crystal unit. Above 100 MC where an inductor is normally used in this position to neutralize the crystal unit shunt capacitance, this simply entails decreasing the value of this inductor below that required for C_0 cancellation.

An example of this design approach is given subsequently.

7-27. DESIGN PROCEDURE FOR SERIES RESONANCE TRANSISTOR OSCILLATORS, 30 TO 200 MC

7-28. Step 1, Selection of a Crystal Unit Type

Select a crystal unit type having a suitable frequency tolerance applicable at the design frequency, and determine from the specification sheet the crystal unit dissipation rating $P_{C\text{MAX}}$ and the maximum resonance resistance $R_{r\text{ max}}$ at this frequency. From 100 to 125 MC where neutralization of the crystal unit shunt capacitance is desirable, the specified value of maximum resonance resistance can be regarded as equivalent to the maximum value of the motional arm resistance. Above 125 MC where no military specifications for crystal units exist at this time, $R_{l\text{ max}}$ can be specified to the manufacturer as 100 ohms, and the crystal dissipation rating can be considered to be 2 MW.

Calculate the permissible signal voltage at the crystal input terminal from:

$$V_{\text{max}} = 2 \sqrt{P_{C\text{MAX}} \cdot R_{r\text{ max}}} \quad (7-49)$$

7-29. Step 2, Selection of a Suitable Transistor Type

The characteristics having the greatest influence on the amplifier performance are the current gain-bandwidth product and the collector-base capacitance. A high f_T and low C_{ob} are indicative of good high frequency performance.

Judging by experimental results, satisfactory oscillators can be designed at frequencies up to 120 MC and perhaps 150 MC using transistor types having typical current gain-bandwidth products of 300 to 400. Above 120 MC, transistor types having current gain-bandwidth products of 700 or larger should be satisfactory. It appears doubtful that types having a typical f_T of less than 500 will be suitable at the highest frequencies due to excessive amplifier regeneration at suitable voltage gain levels. To adequately stabilize amplifiers using these types at 200 MC will probably require the voltage gain to be so low that crystal unit overdrive is likely to occur. However, if the amplifier is neutralized, it may be possible to develop a satisfactory design.

7-30. Selection of a Suitable Transistor DC Operating Point

The first consideration is to bias the transistor in a region where the current gain-bandwidth product is optimized and where the emitter base capacitance is minimized. For transistor types suitable for oscillator designs, the current gain-bandwidth product is usually largest in the collector current range

of 3 to 30 MA and for collector-emitter DC voltages of 5 to 20 volts. $C_{cb'}$, which forms a part of C_{ob} and is presumably a major factor in the amplifier regeneration action, is also suitably minimized in this range of DC collector-emitter voltage.

If only low power output is required as would usually be the case when used, for example, as a receiver mixer injection signal source, the lower collector current and collector-emitter voltage will be suitable. If high power output is desired, bias conditions approaching the higher end of the quoted ranges will be necessary. Power outputs approaching 50 percent of the transistor dissipation can be obtained, and calculations similar to those that would be used at low frequencies to determine the bias conditions for a Class A power amplifier may be helpful in determining suitable bias conditions. This assumes, however, that the amplifier will be stable with the calculated collector load resistance, which may be very far from the case.

7-31. Step 4, Calculation of the Component Values for the Test Amplifier

The circuit will be of the form shown in Figure 7-11. The collector circuit tuning inductor should resonate with, say, 50 PF at 30 MC, decreasing to perhaps 10 PF at 200 MC. It is desirable that the collector tuned circuit effective parallel resistance should be large compared to the highest value of collector load resistance R_T that will be used during the test. The highest value of R_T will usually be 1 K or less, making a tuned circuit effective parallel resistance of 8 to 10 K suitable. At the lower frequencies the losses of the

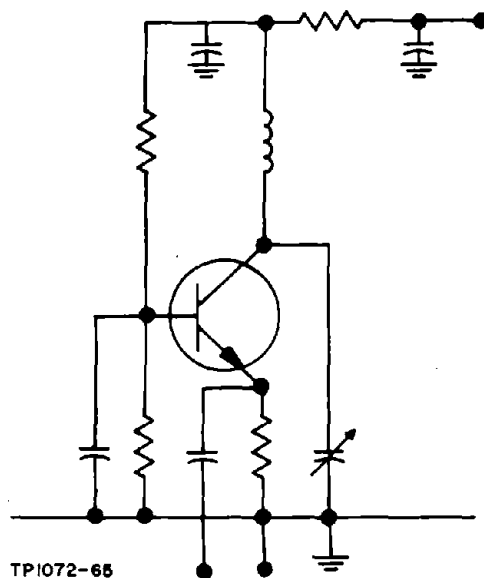


Figure 7-11. Amplifier Test Circuit

collector tuning capacitor will usually be negligible. At the higher frequencies, however, some types of tuning capacitor may have a significant parallel resistance. With the object of converting this amplifier into the prototype oscillator, the biasing resistors should be selected to provide adequate transistor operating point stability over the intended temperature range. The amplifier input loading due to the emitter feed resistor should also be considered which should have a value of, say, 6 to 10 times the expected amplifier parallel input reactance at frequencies above 50 MC. The subsequently presented design examples may be helpful in gauging the reactance levels to be expected. The collector and base circuit decoupling capacitors should be close to self-resonance at the design frequency. A grid-dip meter is useful for determining this condition.

7-32. Step 5, Construction of the Amplifier Test Circuit

The circuit layout should follow good engineering practice with regard to minimizing lead lengths and the decoupling of supply lines. To decrease the possibility of feedback, the emitter and collector circuits should be spaced as far apart as possible consistent with maintaining minimum lead lengths. The layout should allow access to the collector and emitter leads for the voltage measuring probes, and the impedance bridge connections should be immediately adjacent to the emitter connection. With the object of converting this circuit to the prototype oscillator, provision should be made for installing the feedback circuit components at a later stage.

Figure 5-3 shows a circuit layout constructed on a brass chassis designed to mount directly on the ground terminal of the RX Meter. The shield between the emitter and collector circuits is not essential. Unless previously measured and found satisfactory, the collector tuning inductor should not be installed at this stage.

7-33. Step 6, Determination of the Amplifier Characteristics

The procedure to be described applies specifically to the Boonton RX Meter, but should also be adaptable to other high-frequency impedance measuring bridges, provided the signal voltage at the bridge terminals is sufficiently low. The object is to measure the small signal amplifier characteristics, and too large a signal will modify the results, particularly if signal limiting occurs. The linear input signal handling capabilities of a transistor amplifier depends greatly on the transistor bias conditions but generally lies in the range of 10 to 30 MV. Normally the signal output of the RX Meter will be much larger than this, and the instrument used in these tests was modified to make the bridge output signal adjustable.

This modification is described in the instruction manual and consists of connecting a variable resistor in series with the bridge oscillator plate supply

voltage line. It requires about one hour to introduce this modification and is, in any case, a desirable improvement, greatly enhancing the instrument's usefulness for semiconductor circuit measurements.

When using the RX Meter at low output signal levels at high frequencies, there are two effects which should be noted. Adjusting the output signal level will often cause a sufficient change of the bridge oscillator frequency to desensitize the null detector circuit unless a corresponding adjustment is made of the heterodyne oscillator frequency. (This oscillator operates at a frequency 100 KC removed from the bridge oscillator frequency to produce a 100-KC difference frequency which is then fed to the null detector circuit.) At the highest frequencies the heterodyne oscillator signal appears at the bridge terminals at a level of from 5 to 20 MV. This will cause an amplifier output which may mislead the operator into thinking that the amplifier is oscillating.

The measuring procedure is as follows: Adjust the RX Meter to operating condition at the design frequency. Measure and note the input impedance of the RF voltmeters that will be used to measure the amplifier input and output signal voltages. Measure the resistance of a number of carbon resistors and select several having actual resistance values in the range of 200 ohms to 1 K for use as amplifier loads. Values of approximately 200, 300, 500, 700, and 1000 ohms are suitable. The graphs of Figure 5-2 may be useful when making a preliminary selection of resistors. Measure the effective parallel resistance of the collector circuit tuning inductor. Calculate the actual total amplifier load resistance for each load resistor. This consists of the parallel combination of the measured resistance of the loading resistor, the plate circuit RF voltmeter input resistance, and the effective parallel resistance of the collector tuning inductor.

Install the collector tuning inductor in the circuit. Connect the amplifier to the bridge terminals, with the live terminal connecting to the transistor emitter via a capacitor of negligible impedance. Short the collector to the decoupled supply point, null the bridge while setting the bridge output voltage to 10 or 15 MV, retuning the detector oscillator if necessary. Note the amplifier parallel input impedance components. Measure the signal voltage appearing at the decoupling points of the collector and base to ascertain that the decoupling is adequate.

Replace the short circuit with the lowest value loading resistor and tune the collector circuit for maximum collector signal voltage, adjusting the bridge output voltage if necessary. Null the RX Meter and retune the plate circuit for maximum signal. Null the RX Meter again if necessary. Note the amplifier parallel input components. The amplifier input inductance may in some cases be beyond the range of the bridge and it will then be necessary to place a capacitor across the bridge terminals to obtain a null indication. Repeat the measuring process for the remaining load resistors.

Using a signal generator and a calibrated attenuator, measure the relative accuracies of the RF voltmeters at the scale settings employed in the test. Correct the readings accordingly and calculate the amplifier voltage gain for each load condition. Plot the amplifier voltage gain and input resistance as a function of the total amplifier load resistance.

7-34. Step 7, Selection of an Amplifier Operating Condition for the Oscillator Design

The problem is one of selecting from the plotted data an operating point which will provide a high voltage gain and negligible undesirable effects due to amplifier instability. Numerous alternatives exist, but one criterion which appears to be valid at least above 70 MC is that at the operating point selected the amplifier input resistance should not exceed twice the value measured when the collector is shorted. This appears to ensure a satisfactory degree of amplifier stability and may be used as a guide in determining the maximum collector load that may be employed.

When the operating point has been selected, the oscillator design calculation is as follows: Tabulate the corresponding values of amplifier total load R_T , the amplifier parallel input components R_{in} and $X_{L(p)}$, and the amplifier voltage gain G_V . Calculate:

$$A_{V_C} = \frac{R_{in}}{R_{in} + R_{r \max}} \quad (7-50)$$

$$|A_{V_C}| = \frac{\omega L(p)}{R_{r \max} \sqrt{1 + \left[\frac{\omega L(p)}{R_{r \max}} \left(1 + \frac{R_{r \max}}{R_{in}} \right) \right]^2}} \quad (7-51)$$

Select a value half-way between these two and calculate:

$$A_{V_t} = \frac{1.4}{G_V \cdot A_{V_C}} \quad (7-52)$$

$$R_{FB} = \frac{R_{in} + R_{r \max}}{A_{V_t}^2} \quad (7-53)$$

Calculate the resistance of the parallel combination of R_{FB} and the previously measured parallel resistance of the collector tuning inductor and the voltmeter to be used in the collector circuit. Designating this resistance as R_n , calculate the actual oscillator load resistance from:

$$R_L = \frac{R_n \cdot R_T}{R_n + R_T} \quad (7-54)$$

Calculate the impedance transformer component values. The capacitive divider appears to be the most suitable network to use at these frequencies. The design relationships for this network are:

$$A_{V_t} = \frac{C_1}{C_1 + C_2} \quad (7-55)$$

and

$$X(C_1 + C_2) \leq \frac{1}{3} (R_{r \max} + Z_{in}) \approx \frac{1}{3} R_{r \max} \quad (7-56)$$

This latter condition is imposed by phase angle considerations as discussed in Section 4. In order to obtain good frequency correlation, it may be necessary to increase or decrease $X(C_1 + C_2)$ to introduce a small phase angle. Convert the amplifier to the oscillator circuit.

7-35. DESIGN EXAMPLES

7-36. 193-MC Oscillator

The circuit is shown in Figure 7-12 and was designed for true grounded base operation as a precaution against possible difficulties due to AC grounding the base. This is not necessary in practice, and a conventional single voltage supply biasing scheme should be suitable. The calculation is presented for both values of A_{V_C} for comparison purposes.

A 150-MC crystal was used in this evaluation by operating it in the 9th overtone mode. Late in the evaluation period the pins of the crystal holder (HC-18) were damaged and it was necessary to transfer the crystal to another holder

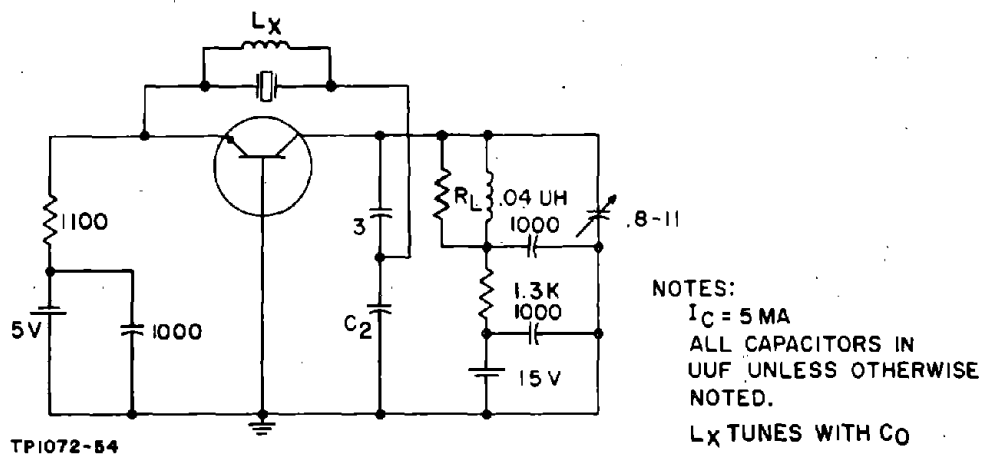


Figure 7-12. 193-MC Oscillator Circuit

(HC-6). The repackaged crystal resistance was approximately 20 percent larger and the series resonance frequency decreased 10 KC. No other ill effects were noted.

The design calculation is presented for both values of A_{V_C} for comparison purposes. The crystal unit used had characteristics similar to those of the CR-56A/U but with $R_1 \text{ max} = 100$ ohms, $P_{C\text{MAX}} = 2$ MW. The measured amplifier data is given in Figure 7-13, and a working point was selected at $R_T = 600$ ohms, $R_{in} = 460$ ohms, $G_V = 12.5$, $X_{L(p)} = 65$ ohms.

$$\begin{aligned} \text{Then: } A_{V_C} &= 0.82 & |A_{V_C}| &= 0.51 \\ A_{V_t} &= 0.136 & A_{V_t} &= 0.22 \\ R_{FB} &= 30 \text{ K} \end{aligned}$$

Therefore: $R_L \approx R_T = 600$ ohms.

$$\frac{C_2}{C_1} = \frac{1}{A_{V_t}} - 1 = 6.3 \quad \frac{C_2}{C_1} = 3.5$$

For $C_2 = 25$ PF, $C_1 = 4$ PF For $C_2 = 15$ PF, $C_1 = 4.3$ PF

This design was evaluated for $C_1 = 3$ PF, $C_2 = 15$ and 25 PF with the results indicated in Figure 7-14 and Table 7-5.

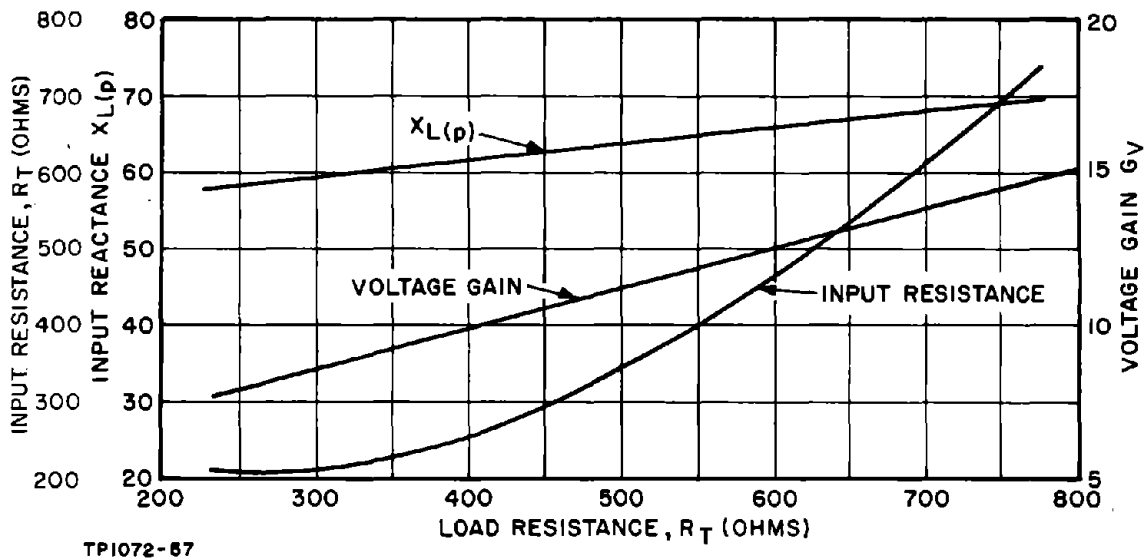


Figure 7-13. 2N917 Common Base Transistor Amplifier at 193-MC

TABLE 7-5. DESIGN EVALUATION DATA, 193-MC TRANSISTOR OSCILLATOR

3.6V (15 UUF)
Nominal $V_o = 3.1V$ (25 UUF), Oscillator Frequency = 192.854 MC

Crystal Unit: $f_s = 192.8560$ MC, $R_1 = 78$ ohms
 $f_s = 192.8463$ MC, $R_1 = 96$ ohms (repackaged)

EFFECT OF	CHANGE	TEST CONDITIONS
$\pm 10\%$ Change in $B+$ on Oscillator Frequency	± 3.2 PPM ± 2.2 PPM	$C_2 = 15$ UUF, $R_L = 640$ ohms, $V_e = -5V$, $T_A \approx 25^\circ C$ $C_2 = 25$ UUF, $R_L = 640$ ohms, $V_e = -5V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in $B+$ on Output Voltage	$\Delta V_o = \pm 4\%$ $\Delta V_o = \pm 10\%$	$C_2 = 15$ UUF, $R_L = 640$ ohms, $V_e = -5V$, $T_A \approx 25^\circ C$ $C_2 = 25$ UUF, $R_L = 640$ ohms, $V_e = -5V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Oscillator Frequency	± 2 PPM ± 1.5 PPM	$C_2 = 15$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $T_A \approx 25^\circ C$ $C_2 = 25$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_o = \pm 13\%$ $\Delta V_o = \pm 15\%$	$C_2 = 15$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $T_A \approx 25^\circ C$ $C_2 = 25$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $T_A \approx 25^\circ C$
$-50^\circ C$ to $+80^\circ C$ Variation of T_A on Oscillator Frequency	± 38 PPM ± 36 PPM	$C_2 = 15$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $R_L = 640$ ohms $C_2 = 25$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $R_L = 640$ ohms
$-50^\circ C$ to $+80^\circ C$ Variation of T_A on Output Voltage	$\Delta V_o = \pm 10\%$ $\Delta V_o = \pm 17\%$	$C_2 = 15$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $R_L = 640$ ohms $C_2 = 25$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $R_L = 640$ ohms

T_A = Oscillator Ambient Temperature

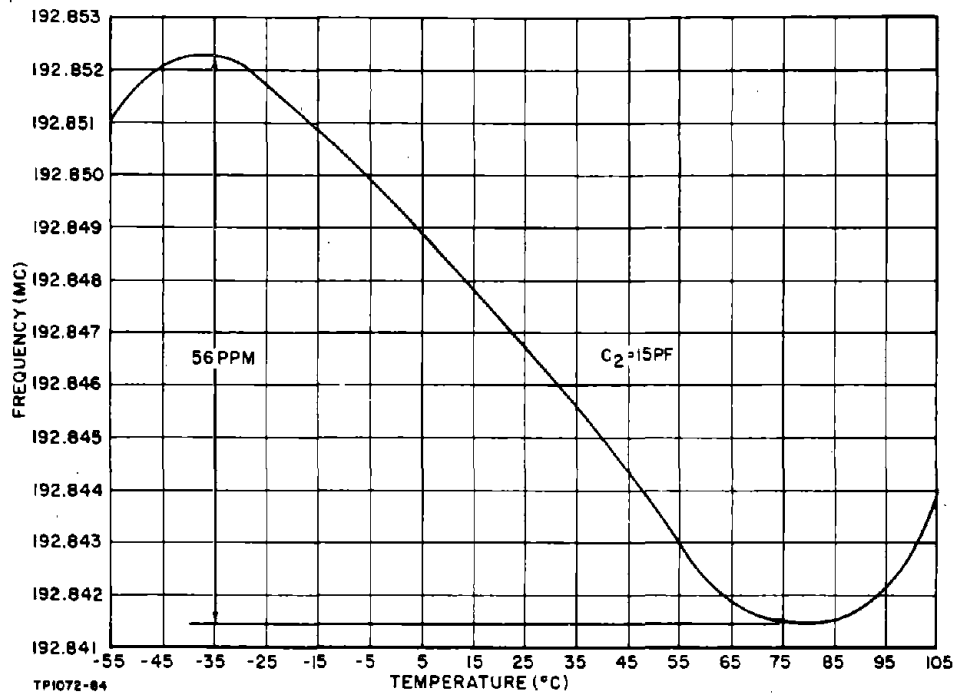


Figure 7-14. Frequency Vs. Temperature for the 193-MC Transistor Oscillator (2N917)

7-37. 150-MC Oscillator

This is essentially the same circuit that was used at 193 MC but with tuning and feedback circuit changes (see Figure 7-15). However, a comparison of the amplifier voltage gain and input impedance as a function of load for the two cases shows that the transistor characteristics changed considerably. The same comments concerning amplifier biasing apply.

The crystal units used had characteristics similar to those of the CR-56A/U but with $R_1 \text{ max} = 100 \text{ ohms}$, $P_{\text{CMAX}} = 2 \text{ MW}$. The measured amplifier data is given in Figure 7-16 and an amplifier working point was selected at $R_T = 600 \text{ ohms}$, $R_{\text{in}} = 150 \text{ ohms}$, $G_V = 34$, $X_{L(p)} = 43 \text{ ohms}$.

$$\begin{aligned} \text{Then: } A_{V_C} &= 0.6 & |A_{V_C}| &= 0.35 \\ A_{V_t} &= 0.069 & A_{V_t} &= 0.12 \\ R_{\text{FB}} &\approx 53 \text{ K} \end{aligned}$$

$$\text{Therefore: } R_L \approx R_T = 600 \text{ ohms}$$

$$\frac{C_2}{C_1} = \frac{1}{A_{V_t}} - 1 = 13.5 \quad \frac{C_2}{C_1} = 7.5$$

$$\text{For } C_2 = 50 \text{ PF, } C_1 = 3.7 \text{ PF} \quad \text{For } C_2 = 25 \text{ PF, } C_1 = 3.3 \text{ PF}$$

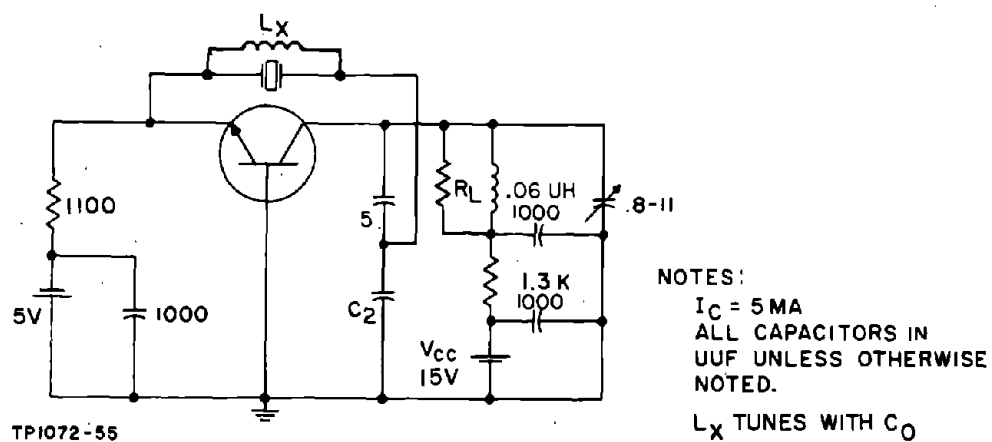


Figure 7-15. 150-MC Oscillator Circuit

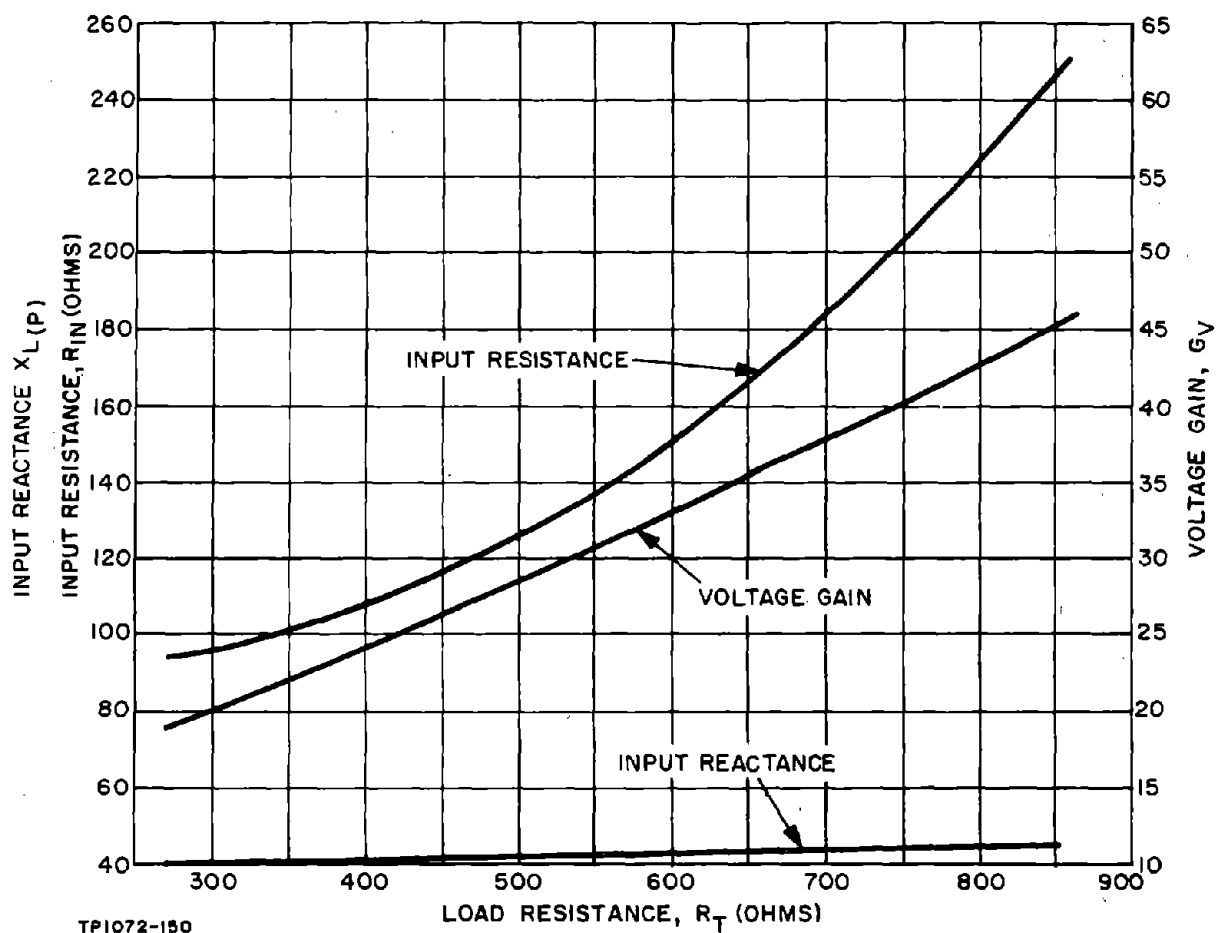


Figure 7-16. 2N917 Common Base Transistor Amplifier at 150 MC

This design was evaluated using $C_1 = 5 \text{ PF}$, $C_2 = 25$ and 50 PF with the results indicated in Figure 7-17 and Table 7-6.

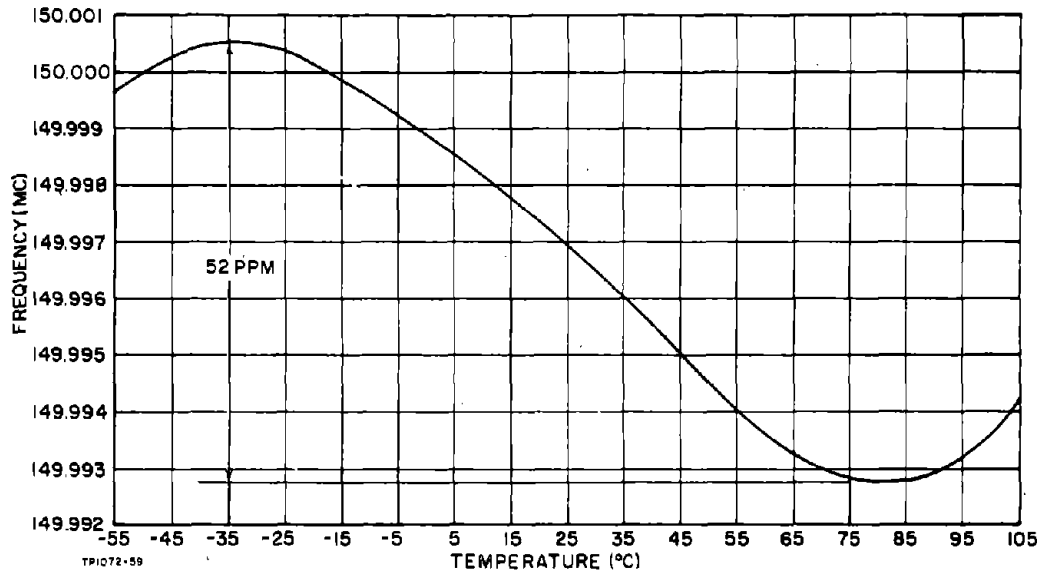


Figure 7-17. Frequency Vs. Temperature for the 150-MC Transistor Oscillator (2N917)

7-38. 120-MC Oscillator

The object of this design was to obtain a high power output. Consequently, a transistor type was selected having a dissipation rating higher than would normally be used in crystal oscillator service. The oscillator circuit is shown in Figure 7-18. The crystal unit characteristics are:

$$\text{CR-56A/U, } R_r \text{ max} = 60 \text{ ohms, } P_{\text{CMAX}} = 2 \text{ MW.}$$

The measured amplifier data are given in Figure 7-19, and a working point was selected at $R_T = 320 \text{ ohms}$, $R_{in} = 130 \text{ ohms}$, $X_{L(p)} = 19 \text{ ohms}$, $G_V = 37$.

TABLE 7-6. DESIGN EVALUATION DATA, 150-MC TRANSISTOR OSCILLATOR

Nominal $V_o = 3.5V$ (25 UUF) Oscillator Frequency = 150.0011 MC
 $V_o = 3.1V$ (50 UUF)

Crystal Characteristics: $f_r = 150.0013$ MC, $R_1 = 50$ ohms
 $f_r = 150.0018$ MC, $R_1 = 65$ ohms

EFFECT OF	CHANGE	TEST CONDITIONS
$\pm 10\%$ Change in B+ on Oscillator Frequency	± 1.4 PPM	$C_2 = 25$ UUF, $R_L = 600$ ohms, $V_e = -5V$, $T_A \approx 25^\circ C$
	± 1.5 PPM	$C_2 = 50$ UUF, $R_L = 600$ ohms, $V_e = -5V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in B+ on Output Voltage	$\Delta V_o = \pm 2\%$	$C_2 = 25$ UUF, $R_L = 600$ ohms, $V_e = -5V$, $T_A \approx 25^\circ C$
	$\Delta V_o = \pm 2\%$	$C_2 = 50$ UUF, $R_L = 600$ ohms, $V_e = -5V$, $T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Oscillator Frequency	± 1.7 PPM	$C_2 = 25$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $T_A \approx 25^\circ C$
	- - - - -	No oscillation with $C_2 = 50$ UUF for -10% change in R_L
$\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_o = \pm 8\%$	$C_2 = 25$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $T_A \approx 25^\circ C$
	- - - - -	No oscillation with $C_2 = 50$ UUF for -10% change in R_L
$-50^\circ C$ to $+80^\circ C$ Variation of T_A on Oscillator Frequency	± 35 PPM	$C_2 = 25$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $R_L = 600$ ohms
	± 35 PPM	$C_2 = 50$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $R_L = 600$ ohms
$-50^\circ C$ to $+80^\circ C$ Variation of T_A on Output Voltage	$\Delta V_o = \pm 7\%$	$C_2 = 25$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $R_L = 600$ ohms
	$\Delta V_o = \pm 11\%$	$C_2 = 50$ UUF, $V_{cc} = 15V$, $V_e = -5V$, $R_L = 600$ ohms
$T_A =$ Ambient Temperature		

Then:

$$A_{V_C} = 0.69$$

$$|A_{V_C}| = 0.29$$

$$A_{V_t} = 0.055$$

$$A_{V_t} = 0.13$$

$$R_{FB} = 60 \text{ K}$$

Therefore:

$$R_L \approx R_T = 320 \text{ ohms}$$

$$\frac{C_2}{C_1} = \frac{1}{A_{V_t}} - 1 = 17$$

$$\frac{C_2}{C_1} = 6.7$$

For $C_1 = 8 \text{ PF}$, $C_2 = 136 \text{ PF}$ For $C_1 = 8 \text{ PF}$, $C_2 = 54 \text{ PF}$

The design was evaluated for $C_2 = 50 \text{ PF}$ for R_L equal to 320 and 250 ohms with the results shown in Figure 7-20 and Table 7-7.

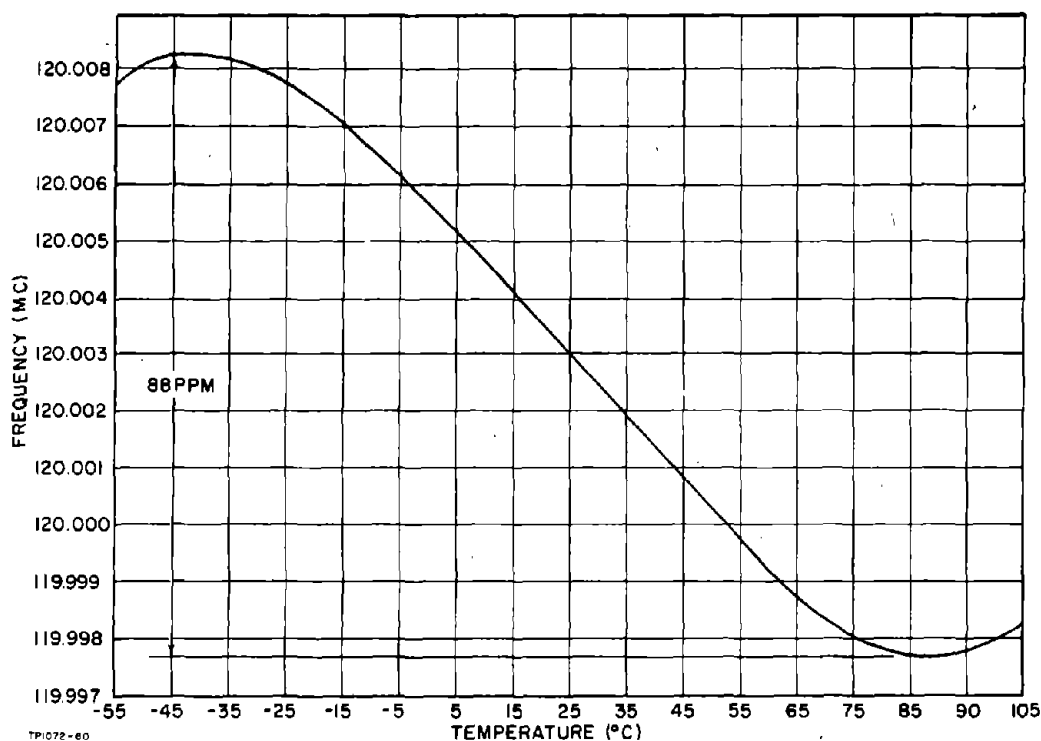


Figure 7-20. Frequency Vs. Temperature for the 120-MC Transistor Oscillator (2N2217)

TABLE 7-7. DESIGN EVALUATION DATA, 120-MC TRANSISTOR OSCILLATOR (2N2217)

Nominal $V_o = \begin{matrix} 6 \text{ V (} R_L = 320 \text{ ohms) } \\ 4.4 \text{ V (} R_L = 250 \text{ ohms) } \end{matrix}$ Oscillator Frequency = 120.0004 MC

Crystals Used: $f_r = 120.0005 \text{ MC, } R_r = 38 \text{ ohms}$
 $f_r = 119.9977 \text{ MC, } R_r = 48 \text{ ohms}$

EFFECT OF	CHANGE	TEST CONDITIONS
$\pm 10\%$ Change in $B+$ on Oscillator Frequency	$\pm 3 \text{ PPM}$	$C_2 = 50 \text{ UUF, } R_L = 320 \text{ ohms, } T_A \approx 25^\circ \text{C}$
$\pm 10\%$ Change in $B+$ on Output Voltage	$\Delta V_o = \pm 7\%$	$C_2 = 50 \text{ UUF, } R_L = 320 \text{ ohms, } T_A \approx 25^\circ \text{C}$
$\pm 10\%$ Change in R_L on Oscillator Frequency	$\pm 2 \text{ PPM}$	$C_2 = 50 \text{ UUF, } V_{cc} = 28 \text{ V, } T_A \approx 25^\circ \text{C}$
$\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_o = \pm 12\%$	$C_2 = 50 \text{ UUF, } V_{cc} = 28 \text{ V, } T_A \approx 25^\circ \text{C}$
-50°C to $+70^\circ \text{C}$ Variation of T_A on Oscillator Frequency	$\pm 52 \text{ PPM}$ $\pm 44 \text{ PPM}$	$C_2 = 50 \text{ UUF, } V_{cc} = 28 \text{ V, } R_L = 320 \text{ ohms}$ $C_2 = 50 \text{ UUF, } V_{cc} = 28 \text{ V, } R_L = 250 \text{ ohms}$
-50°C to $+70^\circ \text{C}$ Variation of T_A on Output Voltage	$\Delta V_o = \pm 12\%$ $\Delta V_o = \pm 12\%$	$C_2 = 50 \text{ UUF, } V_{cc} = 28 \text{ V, } R_L = 320 \text{ ohms}$ $C_2 = 50 \text{ UUF, } V_{cc} = 28 \text{ V, } R_L = 250 \text{ ohms}$

7-39. 75-MC Oscillator

The object of this design was to develop as much power output as possible while maintaining the crystal dissipation below the 2 MW maximum. The circuit is shown in Figure 7-21. This design followed the one at 120 MC, and the 2N2217 - 2N2219 types were again selected for evaluation. At this frequency the 2N2219 had the best voltage gain and input resistance characteristic. When converted to an oscillator and the feedback network optimized, the performance was surprisingly poor, 100 MW being the maximum output obtained. After several values of load resistance and feedback network were attempted without any improvement, it was decided to partially neutralize the transistor so that operation with a larger value of load resistance would be possible. The neutralizing scheme consisted of connecting a coil across the crystal socket. Retesting the circuit on the RX Meter (crystal removed) gave the improved curves of Figure 7-22. These curves show stable gain characteristics for $R_T = 900$ ohms. In practice 500 ohms were the maximum value before tuning hysteresis occurred. The neutralized oscillator displayed a much improved power output (170 MW).

The crystal unit characteristics are:

CR-56A/U, $R_{r \text{ max}} = 50 \text{ ohms}$, $P_{C \text{ MAX}} = 2 \text{ MW}$

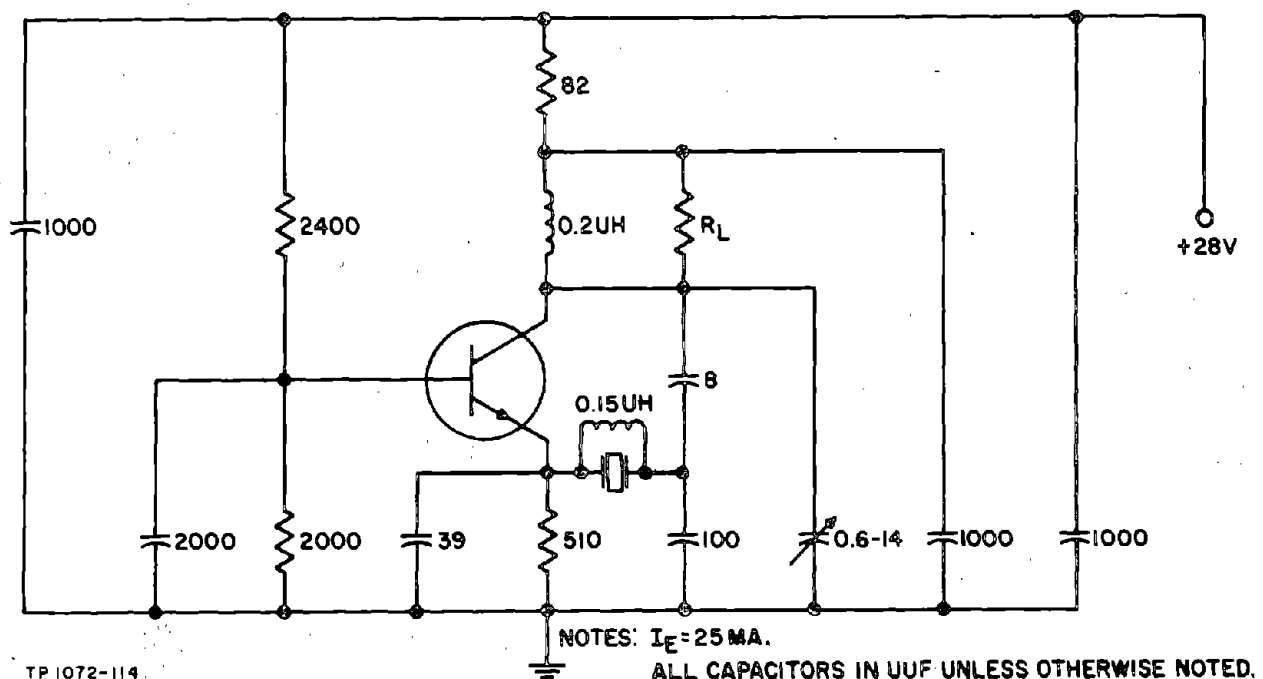


Figure 7-21. 75-MC Oscillator Circuit

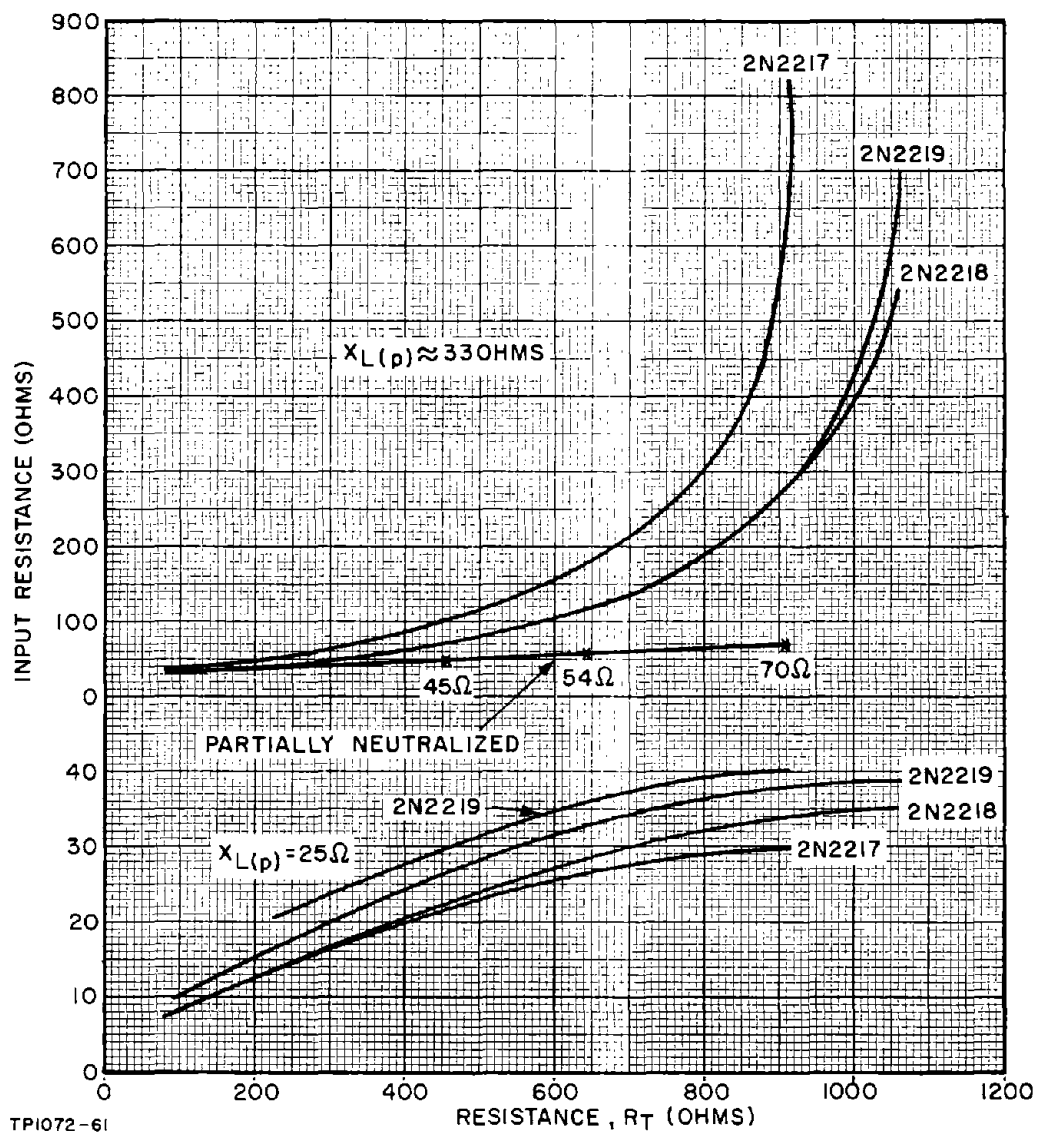


Figure 7-22. 2N2217-2N2219 Transistor Amplifier at 75 MC

The measured amplifier data for the three types of transistors are given in Figure 7-22. Using the data for the neutralized 2N2219 amplifier, a working point was selected at $R_T = 470$ ohms, $R_{in} = 46$ ohms, $G_V = 30$, $X_{L(p)} = 25$ ohms.

Then:

$$A_{V_C} = 0.48$$

$$A_{V_t} = 0.097$$

$$R_{FB} = 10 \text{ K}$$

$$|A_{V_C}| = 0.35$$

$$A_{V_t} = 0.133$$

TABLE 7-8. DESIGN EVALUATION DATA, 75-MC TRANSISTOR OSCILLATOR

Nominal $V_o = 9$ VRMS Corresponding to an Output Power of 170 MW, Oscillator Frequency = 75.0000 MCCrystal Unit: $f_r = 74.9995$ MC, $R_r = 38$ ohms

EFFECT OF	CHANGE	TEST CONDITIONS
$\pm 10\%$ Change in B+ on Oscillator Frequency	± 2.4 PPM	$R_L = 470$ ohms, $T_A \approx 25^\circ\text{C}$
$\pm 10\%$ Change in B+ on Output Voltage	$\Delta V_o = \pm 10\%$	$R_L = 470$ ohms, $T_A \approx 25^\circ\text{C}$
$\pm 10\%$ Change in R_L on Oscillator Frequency	± 1.7 PPM	$V_{cc} = 28\text{V}$, $T_A \approx 25^\circ\text{C}$
$\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_o = \pm 20\%$	$V_{cc} = 28\text{V}$, $T_A \approx 25^\circ\text{C}$
-50°C to $+80^\circ\text{C}$ Variation of T_A on Oscillator Frequency	± 12.5 PPM	$R_L = 470$ ohms, $V_{cc} = 28\text{V}$
-50°C to $+80^\circ\text{C}$ Variation of T_A on Output Voltage	$\Delta V_o = \pm 17\%$	$R_L = 470$ ohms, $V_{cc} = 28\text{V}$

Therefore:

$$R_L \approx R_T = 470 \text{ ohms}$$

$$\frac{C_2}{C_1} = \frac{1}{A_{V_t}} - 1 = 9.3$$

$$\frac{C_2}{C_1} = 6.5$$

For $C_1 = 8 \text{ PF}$, $C_2 = 75 \text{ PF}$

$C_1 = 8 \text{ PF}$, $C_2 = 52 \text{ PF}$

In this case it was necessary to decrease A_{V_t} to prevent crystal unit overdrive, and a value of 100 PF was found suitable for C_2 . The design evaluation data is presented in Figure 7-23 and Table 7-8.

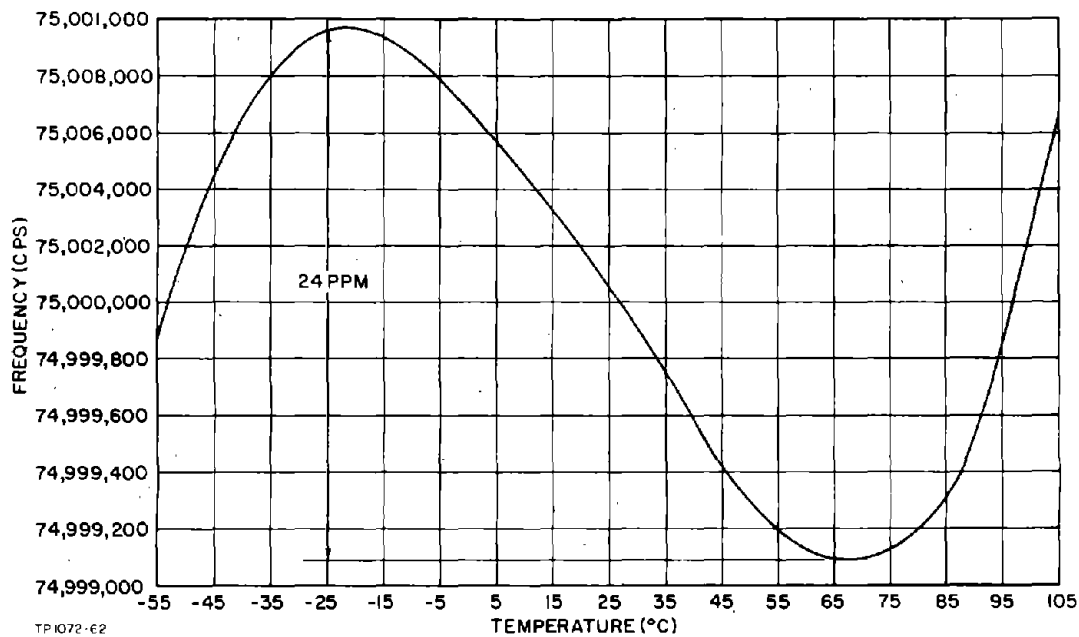


Figure 7-23. Frequency Vs. Temperature for the 75-MC Transistor Oscillator (2N2219)

7-40. TRANSISTOR SERIES OSCILLATORS, 90 TO 500 KC

NOTE: No oscillator design work was performed in this frequency range, and consequently a verified design approach cannot be proposed. The following discussion should therefore only be regarded as a tentative design approach formulated on the basis of experience at higher and lower frequencies with similar circuits.

The oscillator configuration treated for the range of 0.8 to 30 MC is also valid in this frequency range. However, the characteristics of crystal units in the 90 to 500 KC range are such that the configuration shown in Figure 7-2 is only suitable for low power applications where an oscillator output of around 1 MW is required.

This limitation is imposed by the large crystal unit resonance resistance at these frequencies which causes a drastic attenuation of the signal fed back to the transistor emitter. Consequently, the amplifier has to be operated at a high voltage gain which in turn implies a high collector load resistance level, comparable to the feedback network input resistance. Using this circuit, higher oscillator output power can only be obtained by decreasing the feedback signal attenuation. This could be achieved by introducing another impedance transforming network between the crystal output terminal and the transistor emitter as shown in Figure 7-24 (a).

Another alternative which gives similar results is to use a grounded emitter amplifier configuration as shown in Figure 7-24 (b). In this circuit the base input resistance of the transistor amplifier is sufficiently high to avoid an excessive attenuation of the feedback signal between the crystal unit input terminal and the amplifier input, thereby reducing the amplifier voltage gain requirements. This in turn allows a reduction in amplifier load resistance level and consequently an increase in power output. This is the circuit subsequently discussed. However, when the oscillator power output requirement is of the order of the crystal dissipation rating, it is recommended that the circuit described for use in the 0.8 MC to 30 MC range should be employed. The adaptation of the design procedure given for this circuit to the different crystal characteristics should be straightforward.

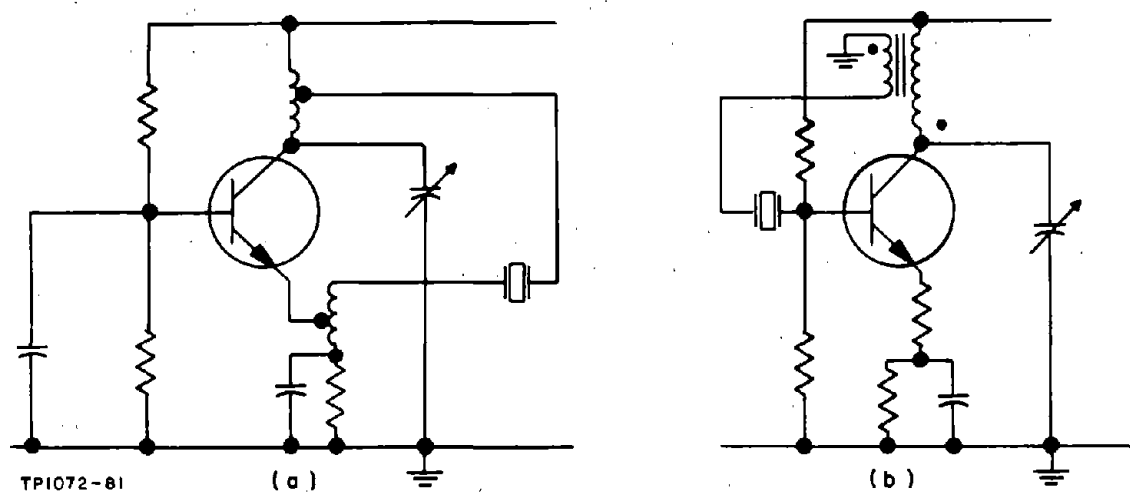


Figure 7-24. Transistor Series Oscillator Circuits

7-41. Crystal Unit Characteristics

Table 7-9 gives the major characteristics of the military standard series resonance crystal units in the frequency range of 90 to 500 KC. There are no preferred series resonance crystal units in the 90 to 200 KC range, but the CR-37A/U anti-resonance type can be used as the equivalent of a series crystal unit if a 20 PF loading capacitor is connected in series with the crystal unit. This type and the CR-42A/U for use in controlled temperature applications, for which the appropriate series loading capacitance is 32 PF, are included in Table 7-9 with this proviso.

The maximum resonance resistance of the crystal units ranges from 2.5 to 7.5 K and the rated dissipation is 2 MW in all cases. The actual value of resonance resistance likely to be encountered is from $1/9 R_{r \text{ max}}$ to $R_{r \text{ max}}$.

7-42. Amplifier Characteristics

It is recommended that only the high-frequency type transistor characterized by current gain-bandwidth products of 100 MC or larger should be employed in this frequency range. These transistor types behave as essentially resistive devices in this frequency range, and their low ohmic emitter and base resistance allow amplifier voltage gain and input resistance to be calculated from relatively simple formulae.

A discussion of the behavior of this type of transistor amplifier together with design equations is given in Paragraphs 3-12 to 3-25.

7-43. Loop Voltage Gain Equations

The loop voltage gain of the circuit of Figure 7-24 (b) can conveniently be divided into two factors. These are:

- (a) The net voltage gain G_{VR} from the crystal unit input terminal to the collector.
- (b) The voltage ratio A_{V_t} of the impedance transformer between the collector and the crystal input terminal.

The loop voltage gain is then:

$$G_{VL} = G_{VR} \cdot A_{V_t} \quad (7-57)$$

The net voltage gain of a common emitter amplifier with an emitter de-generation resistor and a series base resistor R_{bb} , at frequencies well below

TABLE 7-9. MILITARY STANDARD SERIES RESONANCE CRYSTAL UNITS, 90 TO 500 KC

Nominal Frequency (MC)	Operating Temperature (°C)	Frequency Tolerance (%)	Rated Drive (MW)	Maximum Resonance Resistance (ohms)	Crystal Unit Type	Holder Type
WIDE TEMPERATURE RANGE CRYSTAL UNITS						
*0.08 to 0.2	-40 to +70	±0.01	2	2000 to 2500	CR-16B/U	HC-21/U
**0.09 to 0.25	-40 to +70	±0.02	2	5000 to 5500	CR-37A/U	HC-13/U
0.2 to 0.5	-40 to +85	±0.01	2	2500 to 7500	CR-25A/U	HC-6/U
0.455	-40 to +70	±0.02	2	3300	CR-45/U	HC-6/U
TEMPERATURE CONTROLLED CRYSTAL UNITS						
*0.08 to 0.2	70 to 80	±0.002	2	2000 to 2500	CR-30A/U	HC-21/U
**0.09 to 0.25	70 to 80	±0.003	2	4500 to 5000	CR-42A/U	HC-13/U
0.2 to 0.5	70 to 80	±0.002	2	2500 to 7500	CR-26A/U	HC-6/U

* Special Application

** Anti-Resonance Types

the voltage gain cutoff frequency f_v , and provided that the collector load is much smaller than the collector-base diode resistance, is:

$$G_{VR} = \frac{\alpha_o R_T}{r_E + r_e + (r_{bb}' + R_{bb}) (1 - \alpha_o)} \quad (7-58)$$

The amplifier input resistance, provided that the time constant $R_{b'e} \cdot C_{b'e}$ is much less than 1, is:

$$R_i \approx r_{bb}' + R_{bb} + h_{FE} (r_E + r_e) \quad (7-59)$$

In this circuit R_{bb} is the resonance resistance of the crystal unit. Consequently, the net voltage gain will be a minimum when R_r has its maximum value $R_{r \max}$ and when α_o is equal to $\alpha_{o \min}$. These are, therefore, the values that should be used for a worst-case design. Further, since $R_{r \max}$ is at least 2 K compared to r_{bb}' values of less than 100 ohms for the transistor types considered suitable for this application, r_{bb}' can be neglected. The input resistance and voltage gain equations are then:

$$R_i \approx R_{r \max} + h_{FE \min} (r_E + r_e) \quad (7-60)$$

$$G_{VR} = \frac{\alpha_{o \min} R_T}{r_E + r_e + R_{r \max} (1 - \alpha_{o \min})} \quad (7-61)$$

The actual amplifier input resistance will be smaller than that given by the second term of Equation (7-60) due to the loading contributed by the base biasing network. The net voltage gain will then be less than that given by Equation (7-61). Frequently, however, the loading due to the base biasing network can be arranged to be negligible in comparison with the transistor input resistance. Temporarily assuming this to be the case, the net voltage gain is then:

$$G_{VR} \approx h_{FE \min} \cdot \frac{R_T}{R_i} \quad (7-62)$$

To provide a suitably low crystal unit terminating resistance level, the amplifier small signal input resistance should be small compared to $R_{r \max}$. An amplifier input resistance of from 0 to 0.33 $R_{r \max}$ is considered to adequately satisfy this requirement, and the combined input resistance of the amplifier and the crystal unit is then:

$$R_i = K R_{r \max} \quad (7-63)$$

where K has a value of from 1 to 1.33.

The minimum value of $R_{r \max}$ in this frequency range is 2.5 K, and in order to satisfy this requirement the amplifier input resistance must be not more than 850 ohms. Reference to the discussion of common-emitter amplifier input resistance given in Section 4 indicates that this requirement can be met at relatively low emitter current levels for even high current gain transistor types.

The impedance transforming network between the collector and the crystal unit input terminal will have a certain voltage ratio A_{Vt} , giving a loop voltage gain of:

$$G_{VL} = \frac{h_{FE \min} \cdot R_T \cdot A_{Vt}}{K R_{r \max}} \quad (7-64)$$

A_{Vt} is a design variable, the value of which must be selected to be sufficiently large to result in a feasible loop voltage gain, but which must also be sufficiently small to prevent crystal unit overdrive.

The resistance reflected into the collector circuit due to the loading by the feedback circuit is, neglecting losses:

$$R_{FB} = \frac{R_{in}}{A_{Vt}^2} = \frac{K R_{r \max}}{A_{Vt}^2} \quad (7-65)$$

The total amplifier load resistance R_T consists of the oscillator external load R_L , the transformed feedback network load R_{FB} , and the impedance transforming network losses. Assuming the latter to be part of R_L , the relationship is:

$$\begin{aligned} R_T &= \frac{R_L \cdot R_{FB}}{R_L + R_{FB}} \\ &= \frac{K R_L \cdot R_{r \max}}{A_{Vt}^2 \left(R_L + \frac{K R_{r \max}}{A_{Vt}^2} \right)} \end{aligned} \quad (7-66)$$

Substituting for R_T in Equation (7-64) then gives:

$$G_{VL} = \frac{h_{FE \min} \cdot R_L}{A_{Vt} \left(R_L + \frac{K R_{r \max}}{A_{Vt}^2} \right)} \quad (7-67)$$

A loop voltage gain of 1.4 is considered suitable for a worst-case design, provided that the value of $h_{FE \min}$ used is the minimum value likely to be encountered due both to the spread between units and the lowest ambient temperature

to which the oscillator will be subjected. Substituting this value into Equation (7-64) then gives:

$$\frac{R_L}{K R_{r \max}} = \frac{1.4}{A V_t (h_{FE \min} - 1.4 A V_t)} \quad (7-68)$$

This equation relates the amplifier load resistance to the combined input resistance of the amplifier in series with the crystal unit as a function of the feedback transformer voltage ratio and the transistor minimum current gain.

Plotting this relationship using $h_{FE \min}$ as a parameter gives a useful design chart which may be used to estimate for a given transistor h_{FE} the amplifier load and feedback transformer voltage ratios that are suitable. These plots are presented in Figure 7-25.

7-44. Crystal Dissipation

This subject is discussed in Paragraph 7-7 for oscillators in the 0.8 to 30 MC range. The information presented there is also applicable in this frequency range, and the resulting expression for the maximum permissible voltage at the crystal unit input terminal for a worst-case design is:

$$V_{\max} = \sqrt{\frac{P_{C \max} \cdot R_{r \max}}{2}} \quad (7-69)$$

7-45. Relative Values of Crystal Unit Dissipation and Oscillator Power Output

The voltage across the amplifier load resistance is related to V_{\max} by the voltage ratio of the feedback transformer. Consequently, the maximum oscillator power output for a worst-case design is:

$$P_L = \frac{V_{\max}^2}{A V_t^2 \cdot R_L} = \frac{P_{C \max} \cdot R_{r \max}}{2 A V_t^2 \cdot R_L} \quad (7-70)$$

Therefore, the permissible oscillator power output relative to $P_{C \max}$ is:

$$\frac{P_L}{P_{C \max}} = \frac{R_{r \max}}{2 A V_t^2 \cdot R_L} \quad (7-71)$$

Substituting for $\frac{R_{r \max}}{R_L}$ from Equation (7-68) gives:

$$\frac{K P_L}{P_{C \max}} = \frac{(h_{FE \min} - 1.4 A V_t)}{2.8 \cdot A V_t} \quad (7-72)$$

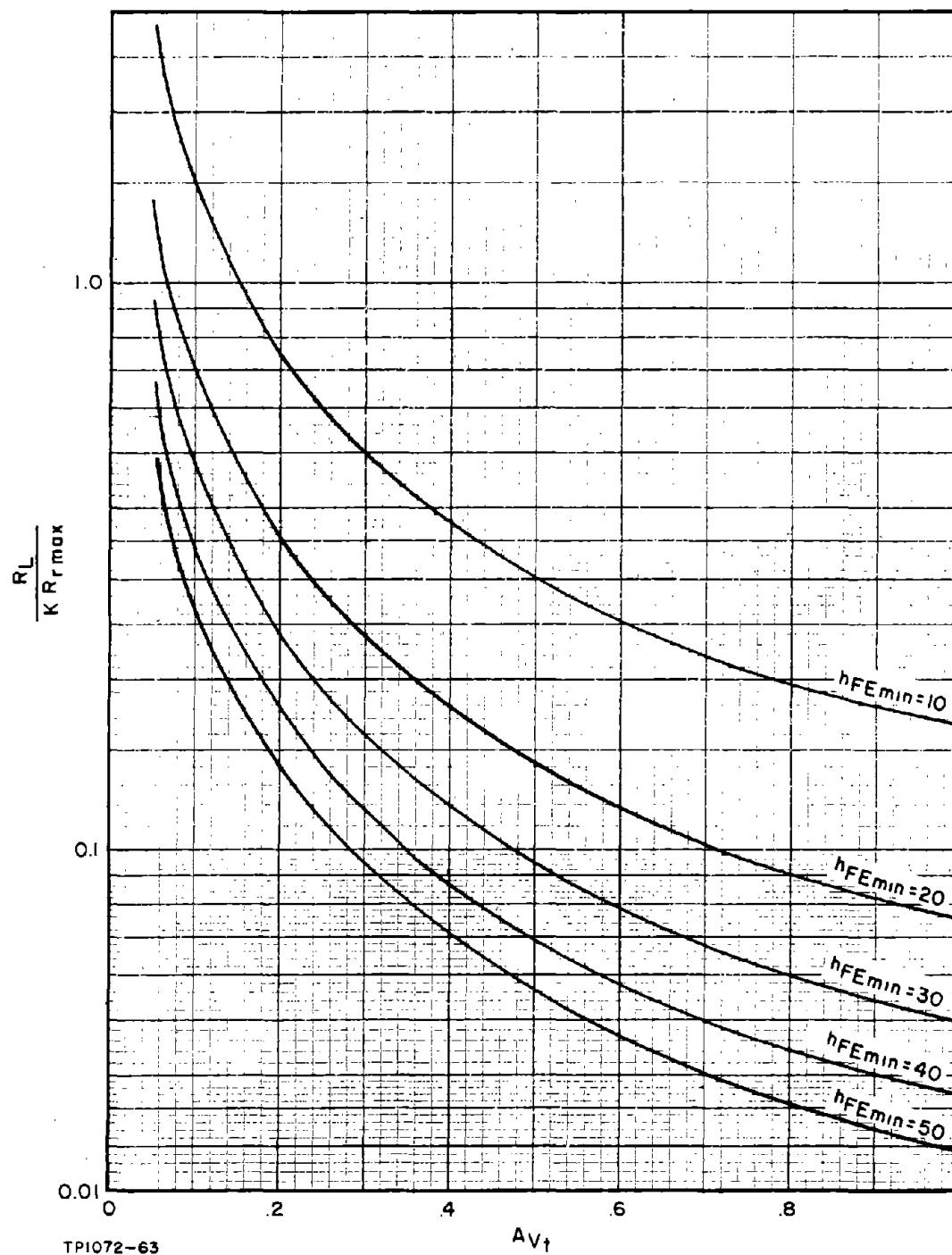


Figure 7-25. Relative Values of R_L and $R_{r \max}$ as a Function of A_{v_t} and $h_{FE \min}$

This equation also provides useful design information when plotted using $h_{FE \min}$ as a parameter. These curves are shown in Figure 7-26 and can be used to estimate for a given transistor minimum h_{FE} the required feedback transformer voltage ratio for a given power output relative to the crystal unit dissipation rating.

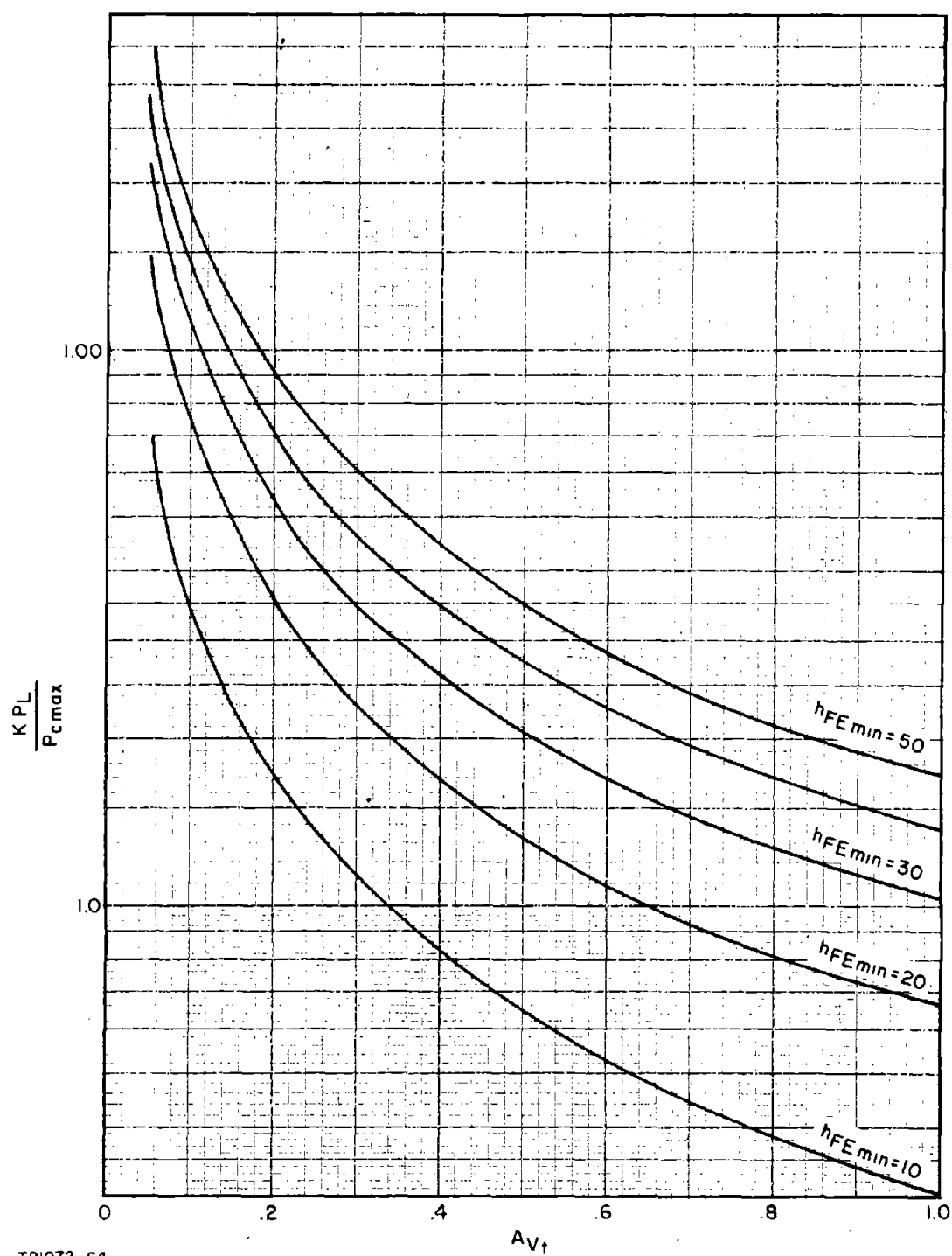
7-46. DESIGN PROCEDURE FOR SERIES RESONANCE TRANSISTOR OSCILLATORS, 90 TO 500 KC

It is suggested that the design procedure should follow the pattern of that presented in Paragraphs 7-9 to 7-13 for design in the 0.8 to 30 MC range. This procedure uses design charts similar to those given in Figure 7-25 and 7-26 to determine a suitable amplifier load resistance and feedback network, and then relates these to the amplifier biasing conditions.

7-47. Noteworthy Points

- (a) When the transistor is operated at current levels of more than 3 MA, it is desirable to employ emitter degeneration in the amplifier. When using high current gain transistors the unbypassed emitter resistor should not be too large, otherwise the amplifier input resistance may not provide a suitable crystal unit terminating resistance level. However, emitter degeneration resistor values as low as 5 ohms will substantially increase the uniformity of the amplifier characteristics.
- (b) The loading due to the base biasing network can be accounted for by considering the transistor current gain to be reduced in the same ratio as the amplifier input resistance is reduced by the loading. Alternatively, the oscillator load may be increased by a similar amount. Paragraph 3-6 gives a method of designing for a minimum loading due to the base biasing network.
- (c) If the amplifier is operated at a high voltage gain, the amplifier may have a substantial capacitive reactance input component possibly approaching the amplifier input resistance in magnitude due to feedback through C_{ob} . This may result in a loop phase lag and a resultant oscillator frequency miscorrelation. It is possible to neutralize the feedback current which causes this effect by means of a capacitor connected from the secondary of the feedback transformer to the amplifier input; that is, in parallel with the crystal socket. The capacitor value should be related to C_{ob} by the equation:

$$C_n = \frac{C_{ob}}{A_{v_t}} \quad (7-73)$$



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Figure 7-26. Oscillator Output Power Relative to Crystal Unit Dissipation Rating

There may, however, be a possibility of uncontrolled oscillation at some higher frequency due to feedback via this capacitance, and if this method fails the alternative is to redesign at a lower collector load level.

- (d) The value of $h_{FE \text{ min}}$ used in estimating the oscillator load and feedback network relationships should correspond to the minimum value of the transistor h_{FE} at the lowest operating temperature. Otherwise, the loop voltage gain is likely to be inadequate under these environmental conditions.

7-48. SERIES RESONANCE TRANSISTOR OSCILLATOR DESIGN, 1 TO 100 KC

The oscillator configuration discussed for use in the 90 KC to 500 KC range is also applicable at these frequencies although, due to the much larger values of crystal unit resonance resistance, design is more demanding and is only just feasible at the lowest frequencies. Unless an impedance transforming network is also used at the amplifier input side of the crystal unit, a large signal attenuation occurs between the crystal unit input terminal and the amplifier input, requiring the amplifier voltage gain to be high. This is not considered to be a very suitable method of decreasing the design requirements, however, and the most suitable alternative appears to be a two-stage amplifier design.

Adding another impedance transformer to the circuit would not cause undue complexity in itself, the complicating factor is the high impedance level required of the network on the crystal unit side. The maximum crystal unit resonance resistance is in the range of 60 to 200 KC, and to make a worthwhile improvement the parallel loss resistance of the impedance transformer should at least approach 10 percent of this value. At the lowest frequencies where an improvement is most desired, the 200 KC value of resonance resistance applies and this would require inductance values of several hundred millihenries if a Q of 20 to 50 is assumed. This would be fairly bulky and would also require to be tuned to avoid loop phase error. And if used untuned, the inductance required would be of the order of several henries. Neither of these possibilities appears to be desirable.

On the other hand, using a two-stage amplifier design, ample gain is obtained and the large attenuation in the feedback circuit is then acceptable. The disadvantage of this approach is the increased circuit complexity and cost.

The single-stage grounded-emitter oscillator circuit described previously for use in the 90 to 500 KC range is therefore probably the most suitable and least complex circuit. However, in order to use this circuit at the lowest frequencies, a high current gain type transistor will be required, and it may also

be necessary to use a collector signal limiting circuit to prevent crystal unit overdrive.

7-49. Crystal Unit Characteristics

The only military type series resonance crystal unit applicable in this frequency range is the CR-50A/U covering the range from 16 to 100 KC. The major characteristics of this crystal unit are:

Frequency Range:	16 to 100 KC, inclusive										
Overall Frequency Tolerance:	± 0.012 percent										
Operating Temperature Range:	-40 to $+70^{\circ}\text{C}$										
Rated Dissipation:	0.1 MW										
Maximum Resonance Resistance:	<table><tr><td>16 to 30 KC:</td><td>100 K</td></tr><tr><td>30+ to 50 KC:</td><td>90 K</td></tr><tr><td>50+ to 70 KC:</td><td>80 K</td></tr><tr><td>70+ to 90 KC:</td><td>70 K</td></tr><tr><td>90+ to 100 KC:</td><td>60 K</td></tr></table>	16 to 30 KC:	100 K	30+ to 50 KC:	90 K	50+ to 70 KC:	80 K	70+ to 90 KC:	70 K	90+ to 100 KC:	60 K
16 to 30 KC:	100 K										
30+ to 50 KC:	90 K										
50+ to 70 KC:	80 K										
70+ to 90 KC:	70 K										
90+ to 100 KC:	60 K										
Crystal Holder:	HC-13/U										

There are no military type crystal units applicable at frequencies below 16 KC, but crystal units are manufactured for operation at frequencies from below 1 KC to 16 KC. Typical manufacturer's data for these give the following major characteristics:

Overall Frequency Tolerance:	± 0.015 percent
Operating Temperature Range:	-40 to $+70^{\circ}\text{C}$
Rated Dissipation:	Values ranging from 10 to 100 UW
Maximum Resonance Resistance:	Values from 100 to 200 K.

NOTE: Of these latter, 10 UW and 200 K appear to be the suitable values to employ for design purposes.

Physical Configuration:

The resonator in these units is in the form of a relatively long quartz bar, and usually the holder is a cylindrical glass bulb 3 to 4 inches in length mounted on an octal tube base, although at the higher frequencies crystal holders of the HC-13/U type may be available.

For these crystal units the range of variation of resonance resistance likely to be encountered is from approximately $1/9 R_{r \max}$ to $R_{r \max}$.

7-50. Crystal Unit Dissipation

In the circuits to be presented the crystal unit operates into the base input impedance of a transistor. Insofar as low-level signal conditions are concerned, this resistance level is much smaller than the crystal unit resonance resistance. It would appear from this that the signal voltage at the amplifier input will be much smaller than that at the crystal unit input terminal. This leads to the conclusion that the crystal unit input voltage should not exceed that value which would cause the rated crystal dissipation when a crystal unit having a minimum value of resonance resistance is in circuit. Taking $R_{r \min}$ as $1/9 R_{r \max}$ gives the permissible input voltage as:

$$V_{\max} = \frac{1}{3} \sqrt{P_{\text{CMAX}} \cdot R_{r \max}} \quad (7-74)$$

This, however, neglects the non-linear behavior of the amplifier input resistance at the relatively large signal levels that will occur in practice. This will increase the average amplifier input resistance and produce a more equitable division of the signal between the crystal unit and the amplifier input resistance.

The permissible input signal voltage will be larger than that given by Equation (7-74) by a factor of perhaps 2. The only adequate way of ensuring that crystal overdrive does not occur is to measure the crystal unit voltage. Normal voltmeter methods are not suitable because of the non-linear waveform at the amplifier input point and oscilloscope measurements are to be preferred, particularly if a differential signal can be displayed, since the voltage appearing across the crystal can then be determined directly.

7-51. Amplifier Characteristics

The general-purpose, small-signal, low-frequency types of transistors are applicable in this frequency range. These types are usually characterized in the data sheets by means of the hybrid or h parameters. The formulae

relating these to the amplifier input and output resistance and gain are given in Paragraphs 3-7 to 3-11.

The high-frequency type transistors having current gain-bandwidth products of 100 MC or more are also suitable. These types have low ohmic base and emitter resistance which allows the amplifier voltage gain and input resistance to be estimated using relatively simple formulae. Amplifier characteristics using these types of transistors are discussed in Paragraphs 3-12 to 3-25. The preceding discussion of series oscillator design in the 90 KC to 500 KC range may be useful when using these types of transistor.

7-52. Oscillator Loop Gain Relationships

The process involved in arriving at a suitable set of loop gain relationships consists of assuming a set of transistor bias conditions and load resistance and determining the power gain and input resistance. These are then related to the crystal unit characteristics to determine the transformation ratio of the impedance transforming network between the collector circuit and the crystal unit. From this the permissible collector signal voltage before crystal overdrive occurs under the worst conditions can be calculated. Provided that the collector signal voltage can be held to this level in practice, the design is then suitable. If not, the design process must either be repeated at a lower collector-emitter DC voltage level or other means of collector signal voltage limiting must be introduced.

The following example of a design suitable for the 16 to 30 KC frequency range illustrates the approach.

NOTE: The following discussion is presented in terms of the circuit power relationships. This is not in keeping with the more usable loop voltage gain relationship used throughout the remainder of the design sections. The use of the loop voltage gain approach is recommended.

For the 2N336 transistor, the following parameters are quoted at the current and voltage levels shown in Figure 7-27.

$$h_{ib} = 55 \text{ ohms}$$

$$h_{ob} = 0.25 \times 10^{-6} \text{ mho}$$

$$h_{rb} = 700 \times 10^{-6}$$

$$h_{fb} = -0.99$$

$$I_e = 1 \text{ MA. ; } V_{ce} = 5 \text{ VOLTS}$$

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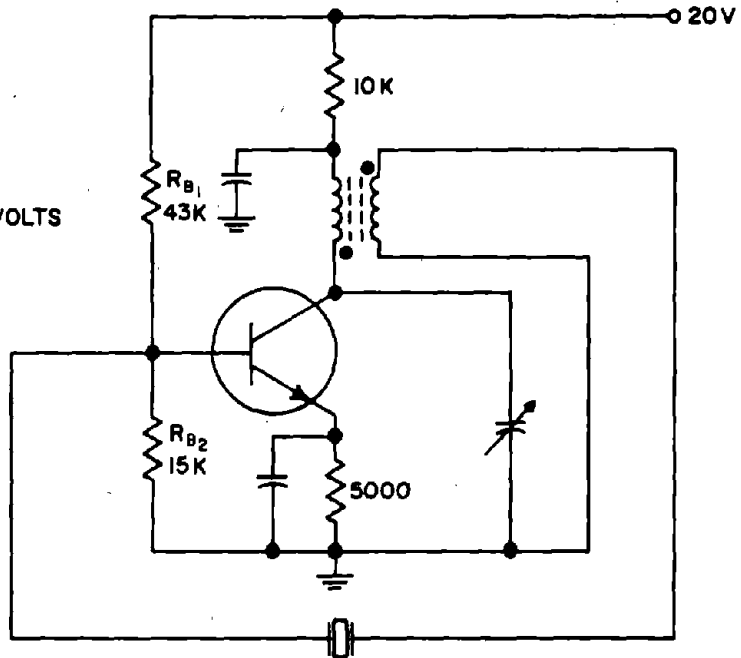


Figure 7-27. Grounded Emitter Tuned Oscillator

Conversion to the common emitter parameters gives:

$$h_{ie} = 5.5 \times 10^3 \text{ ohms}$$

$$h_{oe} = 0.25 \times 10^{-4} \text{ mho}$$

$$h_{re} = 7 \times 10^{-4}$$

$$h_{fe} = 99$$

Substituting these values in Equations (3-18) and (3-19) with $R_T = 10 \text{ K}$ gives:

$$G_p = 12,700$$

$$R_{in} = 5 \text{ K}$$

With the biasing network shown, the value of R_{in} is shunted by R_{B1} and R_{B2} in parallel, and with the values shown, this reduces R_{in} to 3.5 K and G_p to 8700. Decreasing G_p by a factor of 2 to ensure adequate loop gain gives:

$$G'_p = G_p \cdot \frac{R_{in}}{R_{in} + R_r} = 147 \text{ (} R_r = 100 \text{ K)} \quad (7-75)$$

$$R_L = \frac{G_p'}{G_p' - 1} \cdot R_T \approx R_T = 10 \text{ K} \quad (7-76)$$

$$R_{FB} = G_p' \cdot R_T = 1.47 \text{ MEGO} \quad (7-77)$$

$$\text{Transformation Ratio, } T_r = \frac{R_{FB}}{R_{in} + R_r} = 14.2 \quad (7-78)$$

giving a transformer turns ratio of 3.8 if unity coupling is assumed.

The amplifier input resistance is so low that the maximum crystal dissipation will occur when R_r has its minimum value, and the maximum permissible output voltage and power can then be obtained by considering the feedback circuit when $R_r = 11 \text{ K}$.

$$\text{Then:} \quad E = \frac{R_{in}}{R_{in} + R_r} = 0.24 \quad (7-79)$$

$$\text{Therefore,} \quad P_{FB} = \frac{P_{C\text{MAX}}}{1 - E} = 0.13 \text{ MW} \quad (7-80)$$

$$R_{FB} = T_r (R_{in} + R_r) = 206 \text{ K} \quad (7-81)$$

$$P_L = \frac{R_{FB}}{R_L} \cdot P_{FB} = 2.7 \text{ MW} \quad (7-82)$$

This gives an output voltage of approximately 5 VRMS which is larger than the transistor is capable of giving under the assumed bias conditions, and there is no danger of crystal overdrive. A larger power output could be obtained by re-designing the oscillator at a higher transistor dissipation level. No transformer losses are accounted for, and, therefore, the effective load would actually be somewhat lower than 10 K.

The impedance level seen by the crystal at the secondary terminals of the feedback transformer is approximately:

$$\frac{R_L}{T_r} = 360 \text{ ohms} \quad (7-83)$$

The crystal, therefore, sees a total terminating resistance of approximately 3.9 K.

For $I_c = 1 \text{ MA}$, $V_{CE} = 5\text{V}$, the parameters of the 2N336 are:

$$h_{ie} = 5.5 \times 10^3 \text{ ohms}$$

$$h_{re} = 1400 \times 10^{-6}$$

$$h_{fe} = 100$$

$$h_{oe} = 24 \times 10^{-6} \text{ mhos}$$

which, for $R_T = 17 \text{ K}$ gives:

$$G_p = 22,000$$

$$R_{in} = 3.8 \text{ K}$$

The total input resistance consists of 3.8 K and the two 100 K biasing resistors in parallel; that is, 3.6 K. The biasing network resistance R_b reduces the gain to:

$$G_p \times \frac{R_b}{R_b + R_{in}} = 20,000 \quad (7-80)$$

$$R_{r \max} = 200 \text{ K and } R_{r \max} + R_{in} = 204 \text{ K}$$

and therefore:

$$G'_p = G_p \cdot \frac{R_{in}}{R_{r \max} + R_{in}} = 350 \quad (7-81)$$

or

$$\frac{G'_p}{2} = 175$$

$$R_{FEB} = \frac{G'_p}{2} \times R_T = 3 \text{ MEGO} \quad (7-82)$$

The transformation ratio is:

$$T_r = \frac{R_{FEB}}{R_{r \max} + R_{in}} = 15 \quad (7-83)$$

The voltage transformation ratio is:

$$T_v = \sqrt{\frac{R_{FEB}}{R_{r \max} + R_{in}}} = 4 \quad (7-84)$$

π Network Calculation:

The coil used had $L = 110$ MH, and $r_L = 13$ ohms at 3 KC, giving:

$$X_L = 2100 \text{ ohms}$$

Ignoring loading (justified below):

$$\frac{X_L}{X_C} = T_V + 1 = 5 \quad (7-85)$$

where X_C is the reactance of the capacitance in the impedance transforming leg of the π network. Therefore:

$$X_C = 420 \text{ ohms}$$

Comparing X_C with $R_{r \max} + R_{in}$ in parallel with the 13-K resistor supplying $B+$ shows that the phase error will be less than 2 degrees and loading can be ignored. Also r'_S , the series equivalent of the load, will be approximately 14 ohms.

$$X_{Leff} = X_L - X_C = 1700 \text{ ohms} \quad (7-86)$$

$$\phi_I = \tan^{-1} \frac{X_{Leff}}{r_L + r'_S} \quad (7-87)$$

$$\phi_I < 1 \text{ degree}$$

Since loading effects are negligible, Equation (7-85) is justified. Therefore:

$$C = \frac{1}{\omega X_C} = 0.13 \text{ UF} \quad (7-88)$$

The value of the tuning capacitor is given by:

$$C_T = \frac{1}{\omega X_{Leff}} = 0.031 \text{ UF} \quad (7-89)$$

Feedback Phase Shift for $R_r = R_{r \min}$

It is shown previously that for $R_r = 200$ K, the feedback phase shift will be less than 3 degrees. If this network is then used with a crystal with $R_r = 20$ K (lowest R_r value likely to occur), this phase shift may increase. $R_{r \max} + R_{in}$

and the 13-K resistor in parallel gives a total secondary load of 8.5 K. Using the parallel to series transforms, C and R_S in parallel transform to:

$$r'_S = 8,500 \left(\frac{1}{1 + Q^2} \right) \quad (7-90)$$

$$= 21 \text{ ohms}$$

$$X'_C = X_C \frac{Q^2}{1 + Q^2} \approx X_C = 420 \text{ ohms} \quad (7-91)$$

Therefore:

$$\phi_{V_O} = \tan^{-1} \frac{X_C}{r'_S} \approx 87 \text{ degrees} \quad (7-92)$$

$$\phi_I = \tan^{-1} \frac{X_{Leff}}{r_L + r'_S} = \tan^{-1} 50 > 89 \text{ degrees} \quad (7-93)$$

$$\text{Phase error} = 180 - \phi_I - \phi_{V_O} \approx 3 \text{ degrees} \quad (7-94)$$

Maximum crystal dissipation will occur for $R_r = 20 \text{ K}$ (the assumed minimum value), and the permissible output voltage is determined as follows:

For a maximum crystal dissipation of 10 UW, the permissible feedback power P_{FB} for $R_{in} = 3.6 \text{ K}$ will be 12 UW. Therefore, the output voltage of the π network must not exceed a value of:

$$V_{max} = \sqrt{P_{FB} \times R_{r \min} + R_{in}} = 0.53 \text{ VRMS} \quad (7-95)$$

$$\begin{aligned} \text{and } V_O &= V \times T_V \\ &= 2.2 \text{ VRMS} \end{aligned} \quad (7-96)$$

The load presented to the transistor by the 13 K resistor supplying B+ when transformed through the π network is:

$$T_T \times 13,000 = 220 \text{ K}$$

Therefore, for $R_T = 17 \text{ K}$, R_L is required to be 19 K.

A value of 20 K was used for R_L .

The evaluation data are presented in Table 7-10 and Figure 7-29.

TABLE 7-10. DESIGN EVALUATION DATA, 3-KC TUNED OUTPUT TRANSISTOR OSCILLATOR

Nominal $V_o = 2.2V$; Oscillator Frequency = 2999.60 CPS

EFFECT OF	CHANGE	TEST CONDITIONS
$\pm 10\%$ Change of B+ on Oscillator Frequency	≤ 3 PPM	$R_L = 20K, T_A \approx 25^\circ C$
$\pm 10\%$ Change of B+ on Output Voltage	$\Delta V_o = \pm 3\%$	$R_L = 20K, T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Oscillator Frequency	≤ 3 PPM	$E_{cc} = 28V, T_A \approx 25^\circ C$
$\pm 10\%$ Change in R_L on Output Voltage	$\Delta V_o < 2\%$	$E_{cc} = 28V, T_A \approx 25^\circ C$
-50°C to +80°C Change in T_A on Oscillator Frequency	± 145 PPM	$E_{cc} = 28V, R_L = 20K$
-50°C to +80°C Change in T_A on Output Voltage	$\Delta V_o = \pm 13\%$	$E_{cc} = 28V, R_L = 20K$

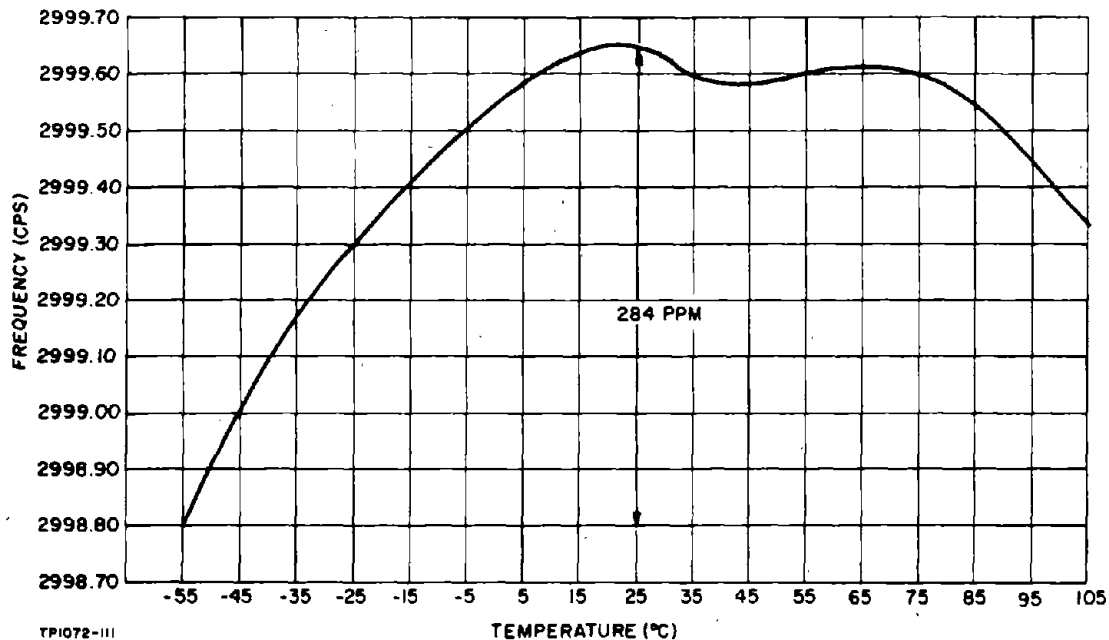
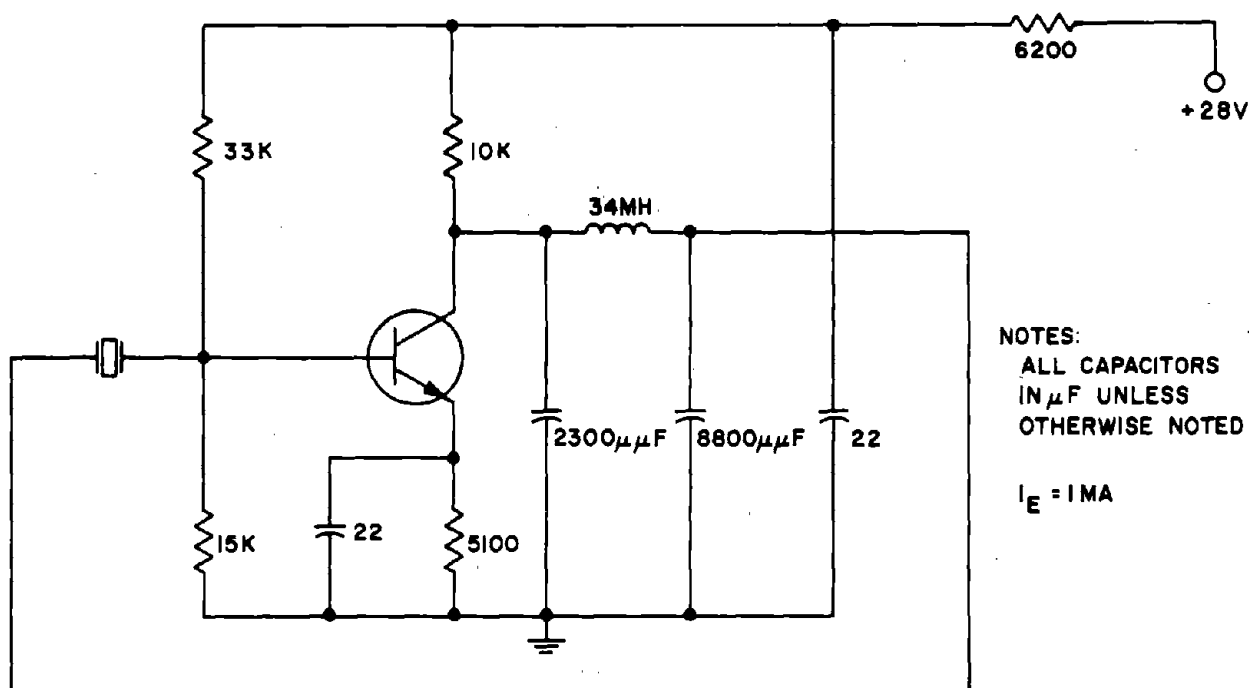


Figure 7-29. Frequency Vs. Temperature for the 3-KC Transistor Oscillator

7-55. 20-KC Transistor Oscillator

This oscillator is similar to that in Paragraph 7-54, the major difference being in the biasing arrangement. Because of the increased feedback efficiency and power dissipation of this type of crystal ($R_T \text{ max} = 100 \text{ K}$, $P_C = 0.1 \text{ MW}$), the output voltage limiting requirements are less stringent. In this particular design, V_{CE} was 4 volts and no additional limiting was required. The circuit is shown in Figure 7-30.

This oscillator could also have been designed with the collector biasing resistor in the low impedance side of the π network. If the same inductor (34 MH) was used, it would then be necessary to increase R_L to give additional gain. The reason for this is that the departure of ϕV_O from 90 degrees for the π network used in the present design would be further increased by the additional loading. This is undesirable, and the only means of reducing this phase error is by decreasing X_C ; that is, increasing T_r . This, in turn, requires increased gain. Alternatively, a lower value of inductance could be used. An inductive transformer would be preferable to the π network.



NOTES:
ALL CAPACITORS
IN μF UNLESS
OTHERWISE NOTED

$I_E = 1 \text{ MA}$

TP1072-113

Figure 7-30. 20-KC Single-Stage Transistor Oscillator

Crystal Used: CR-50/U

Resonant Frequency: 20,403.0 CPS

Resonance Resistance: 14,000 ohms

For $I_e = 1 \text{ MA}$, $V_{CE} = 5 \text{ V}$, the parameters of the 2N336 are:

$$h_{ie} = 5.5 \times 10^3 \text{ ohms}$$

$$h_{re} = 1400 \times 10^{-6}$$

$$h_{fe} = 100$$

$$h_{oe} = 24 \times 10^{-6} \text{ ohms}$$

which, for $R_T = 10 \text{ K}$ gives:

$$G_p = 14,000$$

$$R_{in} = 4.4 \text{ K}$$

The total input resistance consists of 4.4 K and the two biasing resistors in parallel; that is, 3.1 K. The biasing network resistance $R_b = 10 \text{ K}$ reduces the gain to:

$$G_p \times \frac{R_b}{R_b + R_{in}} = 10,700 \quad (7-97)$$

$$R_{r \max} = 100 \text{ K and } R_{r \max} + R_{in} = 103 \text{ K}$$

Therefore:

$$G'_p = G_p \cdot \frac{R_{in}}{R_{r \max} + R_{in}} = 320 \quad (7-98)$$

or

$$\frac{G'_p}{2} = 160$$

$$R_{FB} = \frac{G'_p}{2} \times R_T = 1.6 \text{ MEGOHM} \quad (7-99)$$

The transformation ratio is:

$$T_r = \frac{R_{FB}}{R_{r \max} + R_{in}} = 15 \quad (7-100)$$

The voltage transformation ratio is:

$$T_V = \sqrt{\frac{R_{FB}}{R_{r \max} + R_{in}}} = 3.9 \quad (7-101)$$

The coil to be used had $L = 34 \text{ MH}$, $r_L = 4 \text{ ohms}$ at 20.4 KC giving:

$$X_L = 4350 \text{ ohms}$$

Ignoring loading (justified below):

$$\frac{X_L}{X_C} = T_V + 1 = 4.9 \quad (7-102)$$

where X_C is the reactance of the capacitance in the impedance transforming leg of the π network. Therefore:

$$X_C = 890 \text{ ohms}$$

Comparing X_C with $R_{r \max} + R_{in}$ shows that the phase error will be less than 1 degree and loading can be ignored. Also, r'_s will be approximately 8 ohms.

$$X_{Leff} = X_L - X_C = 3460 \text{ ohms} \quad (7-103)$$

$$\phi_I = \tan^{-1} \frac{X_{Leff}}{r_L + r'_s} = 88 \text{ degrees} \quad (7-104)$$

Since loading effects are negligible, Equation (7-102) is justified. Therefore:

$$C = 8800 \text{ UUF}$$

The value of the tuning capacitor is given by:

$$C_T = \frac{1}{\omega \cdot X_{Leff}} = 2260 \text{ UUF} \quad (7-105)$$

Feedback Phase Shift for $R_r = R_r \text{ min}$

It is shown previously that for $R_r = 100 \text{ K}$, the feedback phase shift will be less than 3 degrees. If this network is then used with a crystal with $R_r = 10 \text{ K}$ (lowest R_r value likely to occur), this phase shift may increase. Using the parallel-to-series transforms, C and $R_r \text{ min} + R_{in}$ in parallel transform to:

$$r'_s = 61 \text{ ohms}$$

$$X_{C'} \approx X_C$$

Therefore $\phi_{V_0} = 86 \text{ degrees}$

$$\phi_I = 89 \text{ degrees}$$

$$\text{Phase error} = 5 \text{ degrees}$$

Maximum crystal dissipation will occur for $R_r = 10 \text{ K}$ (the assumed minimum value), and the permissible output voltage is determined as follows:

For a maximum crystal dissipation of 100 UW, the permissible feedback power P_{FB} for $R_{in} = 3.1 \text{ K}$ will be 130 UW. Therefore, the output voltage of the π network must not exceed a value of:

$$V = \sqrt{P_{FB} \times R_{s \text{ min}}} = 1.3 \text{ VRMS} \quad (7-106)$$

and $V_{O \text{ max}} = V \times T_v \quad (7-107)$

$$= 5.1 \text{ VRMS}$$

The design evaluation data are presented in Figure 7-31 and Table 7-11.

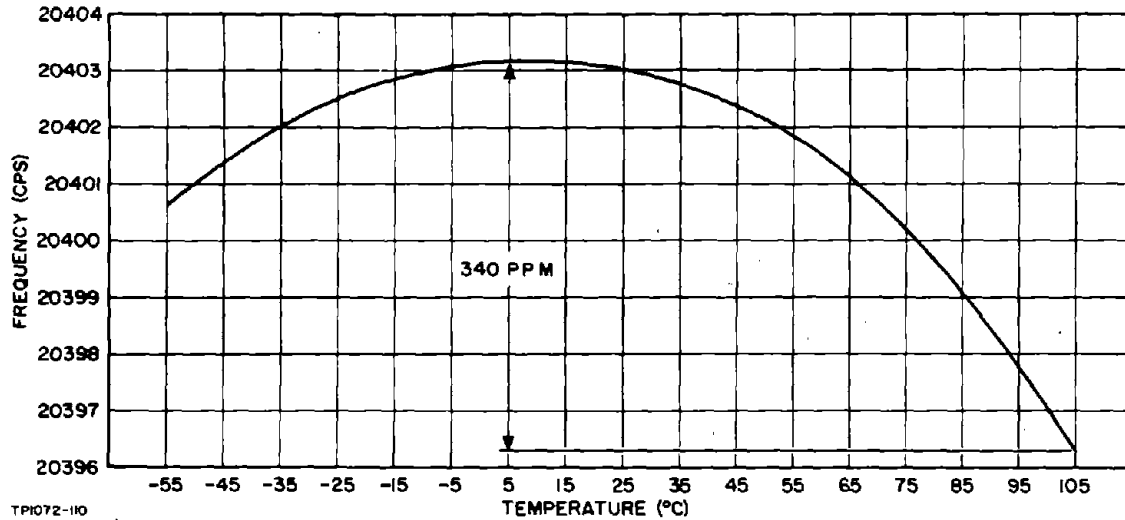


Figure 7-31. Frequency Vs. Temperature for the 20 KC Transistor Oscillator

7-56. 1-KC Two-Stage Transistor Oscillator

In this circuit the amplifier gain is well in excess of 10^6 . Consequently, there was no difficulty in providing adequate loop gain. In fact, it was necessary to severely mismatch the crystal to limit the loop gain sufficiently (note the 2-K resistor in the resistive divider feedback network, Figure 7-32).

Other methods could have been used to give the necessary selectivity. For example, a Wien Bridge network could have been used in place of the tuned circuit and resistance divider network. Furthermore, because of the high available power gain, the sacrifice in output power using the Wien Bridge would not be unduly large, since the total load resistance could be reduced appreciably by appropriately increasing the feedback power.

Crystal Used:	T-9J
Resonant Frequency:	999.93 CPS
Resonance Resistance:	55 Kilohms

TABLE 7-11. DESIGN EVALUATION DATA, 20-KC TUNED-OUTPUT TRANSISTOR OSCILLATOR

EFFECT OF	CHANGE	TEST CONDITIONS
±10% Change in B+ on Oscillator Frequency	≤ 3 PPM	$R_L = 10K, T_A \approx 25^\circ C$
±10% Change in B+ on Output Voltage	$\Delta V_o = \pm 3\%$	$R_L = 10K, T_A \approx 25^\circ C$
±10% Change in R_L on Oscillator Frequency	≤ 3 PPM	$E_{cc} = 28V, T_A \approx 25^\circ C$
±10% Change in R_L on Output Voltage	$\Delta V_o = < 2\%$	$E_{cc} = 28V, T_A \approx 25^\circ C$
-50°C to +80°C Change in T_A on Oscillator Frequency	±85 PPM	$E_{cc} = 28V, R_L = 10K$
-50°C to +80°C Change in T_A on Output Voltage	$\Delta V_o = \pm 10\%$	$E_{cc} = 28V, R_L = 10K$

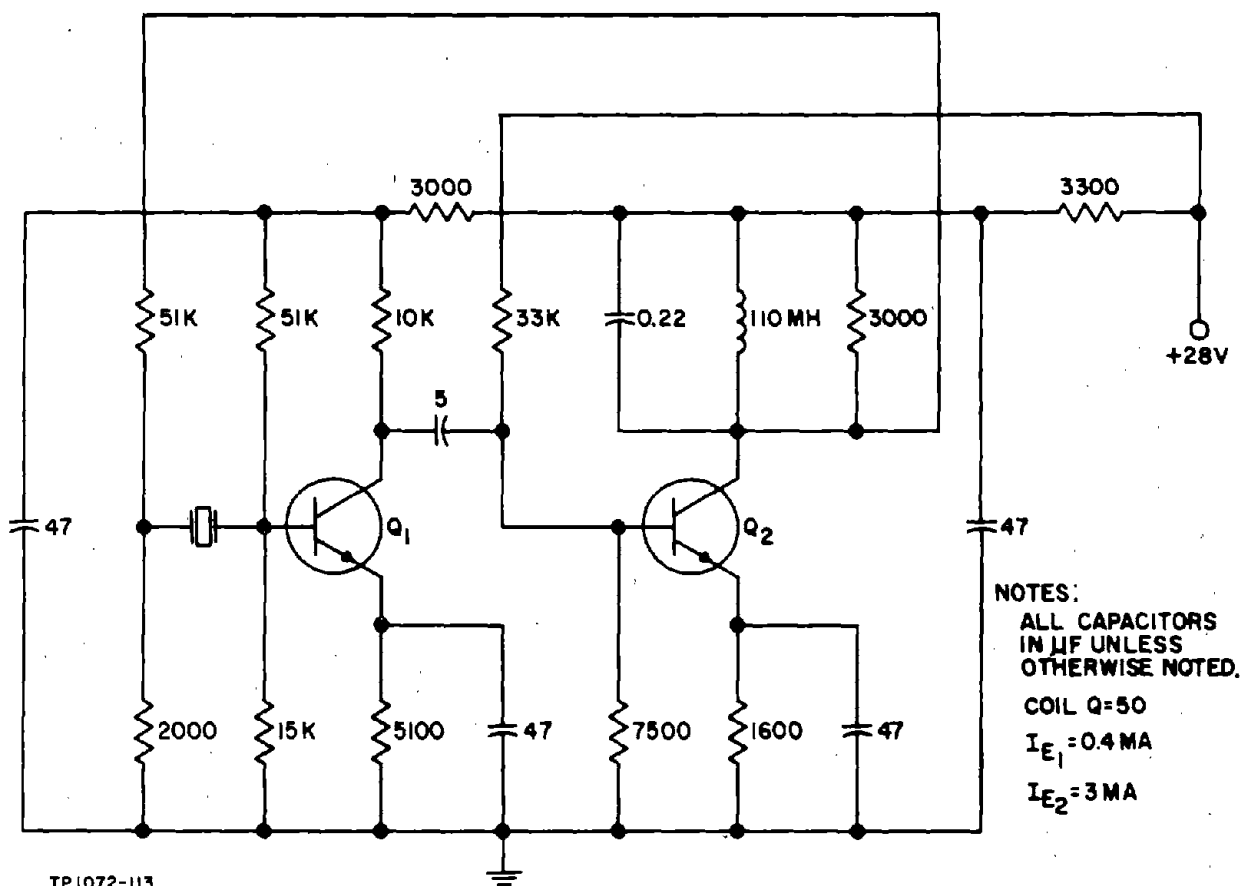


Figure 7-32. 1-KC Two-Stage Transistor Oscillator

The parameters of the 2N336 at $I_e = 1 \text{ MA}$ as given in the manufacturer's data sheets are:

$$I_e = 1 \text{ MA}, V_{cb} = 5 \text{ V}$$

$$h_{ib} = 55 \text{ ohms}$$

$$h_{fb} = -0.99$$

$$h_{rb} = 700 \times 10^{-6}$$

$$h_{ob} = 0.25 \times 10^{-6} \text{ mhos}$$

giving $\Delta_b = 714 \times 10^{-6}$

Transforming common emitter parameters gives, for $I_e = 3 \text{ MA}$, $V_{cb} = 5 \text{ V}$:

$$h_{ie} = 2.2 \text{ kilohms}$$

$$h_{re} = 10^{-3}$$

$$h_{fe} = 120$$

$$h_{oe} = 45 \times 10^{-6} \text{ mhos}$$

Similarly, for $I_e = 0.4 \text{ MA}$, $V_{CE} = 5 \text{ V}$

$$h_{ie} = 9.7 \text{ K}$$

$$h_{re} = 1.9 \times 10^{-3}$$

$$h_{fe} = 57$$

$$h_{oe} = 12 \times 10^{-6} \text{ mhos}$$

The total load on Q_2 is the load resistor (3 K), the load of the feedback network (set at 50 K), and the coil loss resistance (35 K) all in parallel, constituting a load of 2.6 K. Using the parameters for $I_e = 3 \text{ MA}$ and $R_T = 2.6 \text{ K}$ gives the second stage gain:

$$G_{p2} = 15,000$$

and $R_{in} \text{ (transistor alone)} = 1.9 \text{ K}$

The actual input resistance of the second stage consists of R_{in} in parallel with 7.5 K and 33 K (6.1 K) giving: $R_{in} \text{ (actual)} = 1.3 \text{ K}$.

This additional input load reduces the total gain of the second stage by a factor of $\frac{R}{R + R_{in} \text{ (transistor)}}$, where R is the total resistance in parallel with $R_{in} \text{ (transistor)}$. Therefore, $G'_{p2} = 0.76 \times 15,000 = 11,000$.

Using $R_{in} \text{ (actual)}$ as the load of Q_1 and the parameters for $I_e = 0.4 \text{ MA}$ gives a first stage gain: $G_{p1} = 430$

and $R_{in} \text{ (transistor)} = 9.7 \text{ K}$

Combining this with the biasing network (11.6 K) gives:

$$R_{in} \text{ (actual)} = 5.3 \text{ K}$$

and $G'_{p1} = 230$

The total power gain is:

$$G_p = 11,000 \times 230 = 2.5 \times 10^6,$$

which corresponds to a loop voltage gain:

$$G_V = \sqrt{G_p} = 1600$$

For a loop voltage gain of 1.4 (corresponding to a loop power gain of 2), the voltage attenuation of the feedback network is:

$$A_V = \frac{1600}{1.4} = 1150$$

The attenuation ratio of the crystal-transistor input portion of the network is fixed ($R_{in} = 5.3 \text{ K}$, $R_{r \text{ max}} = 200 \text{ K}$); that is:

$$A_{V_C} = \frac{205}{5.3} = 39$$

The attenuation required of the feedback resistive divider is therefore:

$$A_r = \frac{1150}{39} = 30$$

The value of A_r used was nominally 26 (51 K and 2 K).

The coil tuning capacitance required was 0.23 UF.

Design evaluation data are presented in Figure 7-33 and Table 7-12.

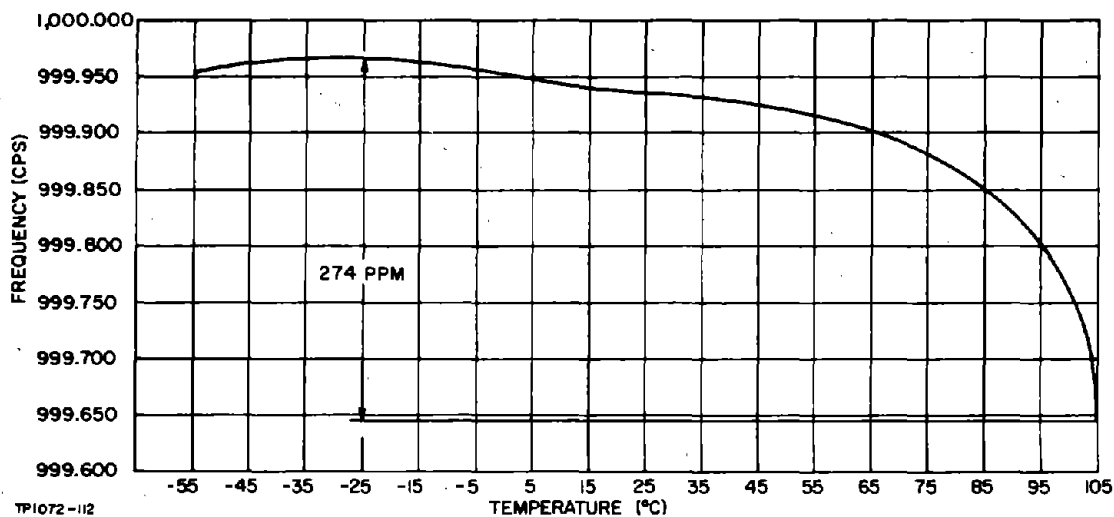


Figure 7-33. Frequency Vs. Temperature for 1 KC Two-Stage Transistor Oscillator

TABLE 7-12. DESIGN EVALUATION DATA, 1-KC TWO-STAGE TRANSISTOR OSCILLATOR

EFFECT OF	CHANGE	TEST CONDITIONS
±10% Change of B+ on Oscillator Frequency	≤ 3 PPM	$R_L = 3K, T_A \approx 25^\circ C$
±10% Change of B+ on Output Voltage	$\Delta V_o = \pm 8\%$	$R_L = 3K, T_A \approx 25^\circ C$
±10% Change in R_L on Oscillator Frequency	≤ 3 PPM	$E_{cc} = 28V, T_A \approx 25^\circ C$
±10% Change in R_L on Output Voltage	$\Delta V_o = \pm 5\%$	$E_{cc} = 28V, T_A \approx 25^\circ C$
-50°C to +80°C Change in T_A on Oscillator Frequency	±50 PPM	$E_{cc} = 28V, R_L = 3K$
-50°C to +80°C Change in T_A on Output Voltage	$\Delta V_o = \pm 3\%$	$E_{cc} = 28V, R_L = 3K$

7-57. 3-KC Two-Stage Transistor Oscillator

This circuit is similar to the oscillator evaluated in Paragraph 7-56. The sole difference is in the tuned circuit elements. At this frequency the inductor had a Q of 150 which resulted in less loading than in the 1 KC design. However since the loading was already negligible in the latter design, this had no effect on the calculations. The value of tuning capacitor required was 0.026 UF (see Figure 7-34).

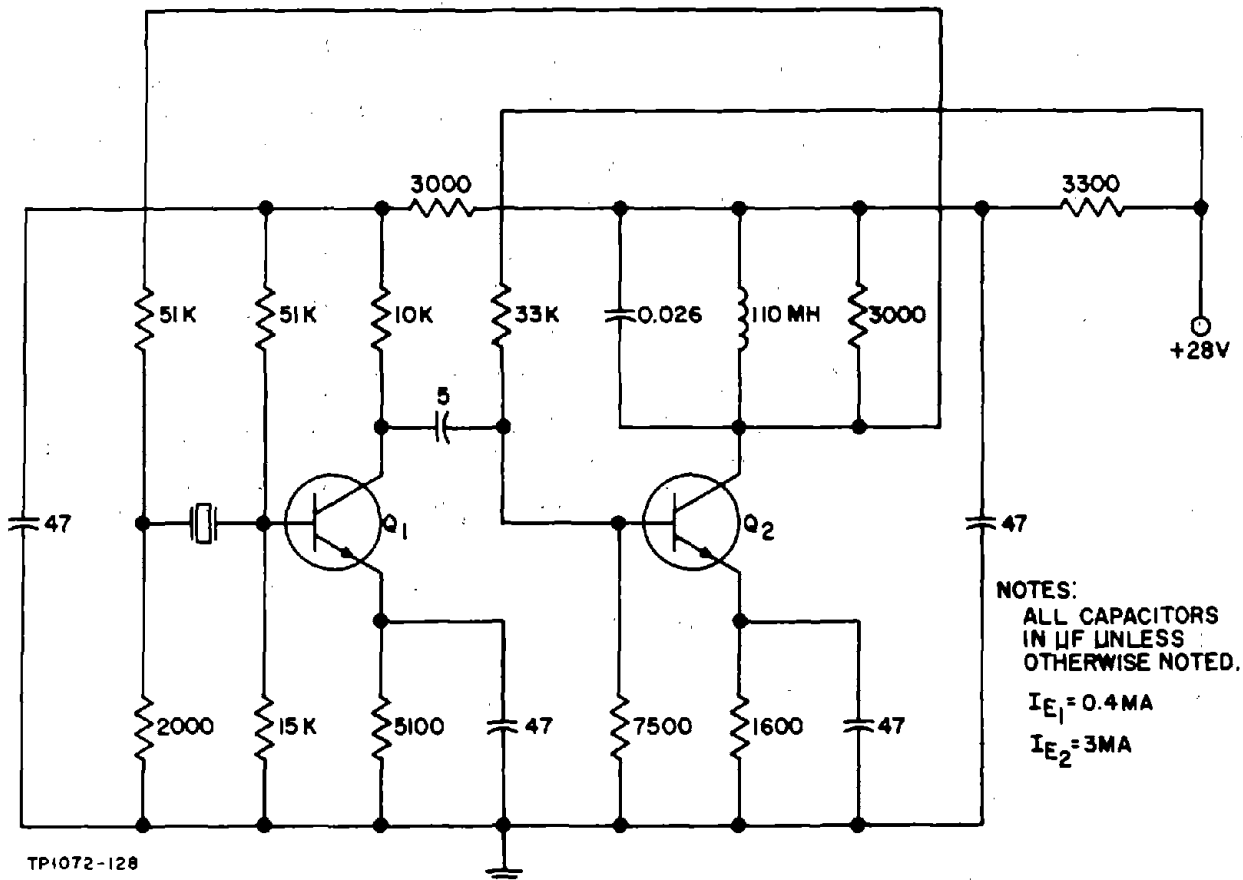


Figure 7-34. 3-KC Two-Stage Transistor Oscillator

The comments made concerning the 1-KC oscillator of this type are equally applicable to this oscillator.

Crystal Used:	T-9XY
Resonant Frequency:	2999.6 CPS
Resonance Frequency:	50 Kilohms

Design evaluation data are presented in Figure 7-35 and Table 7-13.

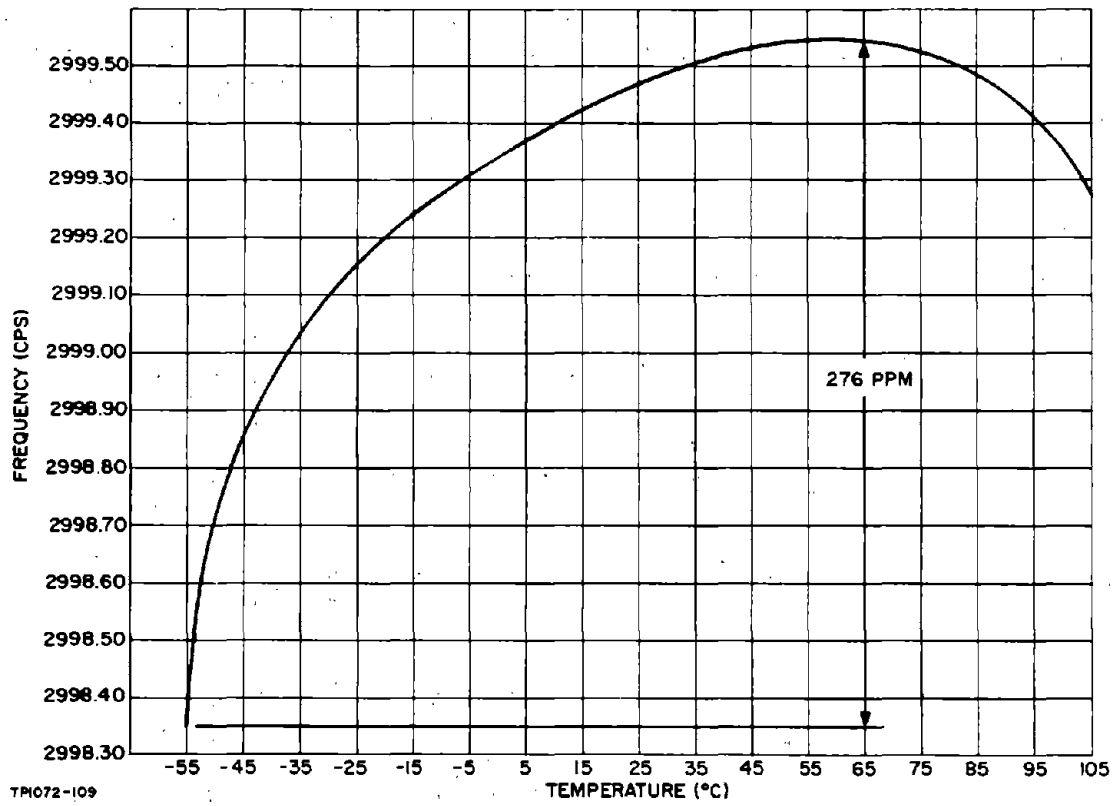


Figure 7-35. Frequency Vs. Temperature, 3-KC Two-Stage Transistor Oscillator

TABLE 7-13. DESIGN EVALUATION DATA, 3-KC TWO-STAGE TRANSISTOR OSCILLATOR

EFFECT OF	CHANGE	TEST CONDITIONS
±10% Change of B+ on Oscillator Frequency	≤ 3 PPM	$R_L = 3K, T_A \approx 25^\circ C$
±10% Change of B+ on Output Voltage	$\Delta V_o = \pm 11\%$	$R_L = 3K, T_A \approx 25^\circ C$
±10% Change in R_L on Oscillator Frequency	≤ 3 PPM	$E_{cc} = 28V, T_A \approx 25^\circ C$
±10% Change in R_L on Output Voltage	$\Delta V_o = \pm 6\%$	$E_{cc} = 28V, T_A \approx 25^\circ C$
-50°C to +80°C Change In T_A on Oscillator Frequency	± 115 PPM	$E_{cc} = 28V, R_L = 3K$
-50°C to +80°C Change In T_A on Output Voltage	$\Delta V_o < \pm 2\%$	$E_{cc} = 28V, R_L = 3K$

SECTION 8

TRANSISTOR ANTI-RESONANT OSCILLATOR DESIGN

8.1 ANTI-RESONANT OSCILLATOR CIRCUITS

The anti-resonance crystal unit lends itself to use in the circuits shown in Figure 8-1. In Figure 8-1 (a) the amplifier output resistance and load can be considered as reflected in parallel with the amplifier input by the impedance transforming network consisting of C_1 and C_2 . The effective capacitance of C_1 and C_2 in series operating in conjunction with C_3 then transforms the combined input and output resistance of the amplifier to a suitable crystal unit terminating level. The amplifier is required to have a nominal zero phase shift, and the active device configuration is usually either an emitter follower or a cathode follower.

In Figure 8-1 (b) the crystal unit operates as the inductive element of a π network of the type analyzed in Paragraph 1-10, where the impedance transforming action is discussed in detail. In this circuit the amplifier is required to have nominal phase inverting properties and the active device configuration is a grounded emitter transistor.

A useful variant of this circuit is obtained by interposing a resistor between the π network and the amplifier output as shown in Figure 8-1 (c). The major advantage of this circuit relative to that of Figure 8-1 (b) is the increased power output obtainable for comparable crystal unit loading or, alternatively, the reduction in loading that can be achieved for comparable output power levels. An analogous variant of the circuit of Figure 8-1 (a) can also be obtained by interposing a resistor between the amplifier output and the junction of the impedance transforming capacitors C_1 and C_2 .

The circuits of Figure 8-1 (b) and (c) appear to be most suited to transistor amplifier designs when the loading of the crystal unit by the amplifier is considered, and these are the circuits selected for discussion. The circuit of Figure 8-1 (b), which will hereafter be referred to as the "basic" Pierce oscillator, is most suited to low power output applications where the output power required is of the order of 1 to 5 MW. This condition is imposed jointly by crystal unit loading considerations and feasible transistor DC current and voltage requirements. This circuit is therefore limited to such applications as, for example, a receiver mixer injection signal source.

The circuit of Figure 8-1 (c), which will be referred to as the "isolating resistor" Pierce oscillator, is suited to both low and high power output applications, having the capability (if required) of giving an output of at least ten times the crystal unit dissipation rating. This may be advantageous in certain circuits such as, for example, transmitter applications.

When the basic Pierce and the isolating resistor Pierce oscillators are compared for low power applications, the former has the advantage of requiring one less trimming capacitor than the latter, but at the higher frequencies this is

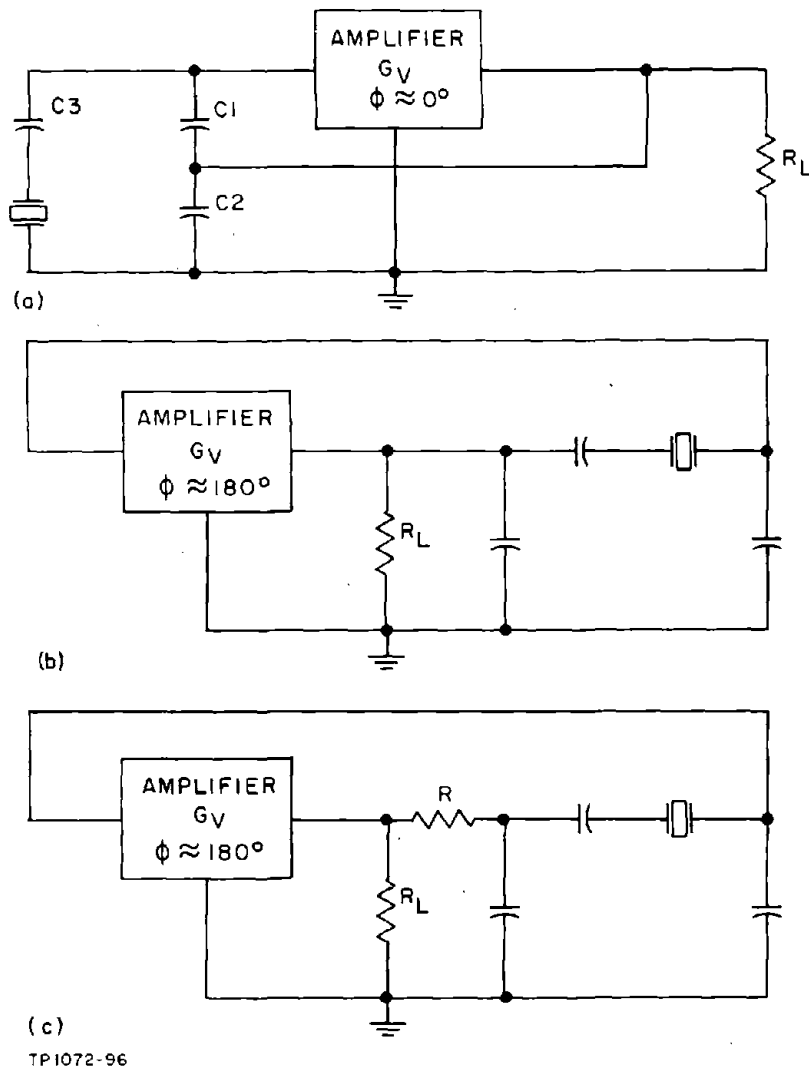


Figure 8-1. Anti-resonance Oscillator Circuits

in general offset by an increase in transistor current requirements. In addition, the isolating resistor circuit at these power levels is easier to design because of the reduction in the interaction of amplifier and feedback circuits. When all factors are considered, therefore, there appears to be little to choose between the two circuits.

These circuits have only been studied in detail for the frequency range of 0.8 to 20 MC, and this forms the bulk of the succeeding discussion. No detailed design approach can be offered for the lower frequency ranges where anti-resonance crystals are also available, but the characteristics of these crystals are such that this circuit appears to be only just feasible in the 90 KC to 500 KC range and impractical below 90 KC. A short discussion is given at the end of this section containing suggestions as to how the approach formulated for the 0.8 to 20 MC range can be adapted to the 90 to 500 KC range.

The following discussion draws heavily on the crystal π network analysis of Section 1 and the high-frequency, common-emitter transistor amplifier discussion of Section 3, to which it will be necessary to refer.

There is another method of using an anti-resonant crystal unit where the crystal unit is connected in series with a capacitor having the specified value of loading capacitance C_L . This series combination behaves in essentially the same manner as a series type crystal unit, and the design of the oscillator circuit becomes essentially that of a series oscillator. For this type of circuit reference should be made to the appropriate handbook section dealing with the design of series oscillators in the particular frequency range of interest.

8-2. Anti-resonance Crystal Units, 0.8 to 20-MC Range

Table 8-1 gives the military standard anti-resonance crystal units in the 0.8 to 25-MC range. With the exceptions of the CR-33A/U and the CR-71/U, these are all fundamental mode crystal units having similar characteristics in those frequency regions where overlap occurs. The CR-33A/U is a special applications unit which should not be used in new military equipments without governmental permission (see Table 1-5).

The CR-71/U is a fifth overtone unit intended for use in high precision crystal oscillators. This type of oscillator requires special circuit provisions such as close tolerance crystal unit temperature control, automatic gain control to maintain crystal dissipation virtually constant, and well regulated supply voltage. This type of operation is beyond the scope of this discussion and this crystal unit is only included to give complete coverage of the crystal unit types available.

Below 2.9 MC for wide temperature applications there is no real choice of crystal units available to the designer. The CR-18A/U and CR-58A/U units have identical performance characteristics, and the sole difference is in the holder pin-size. Above 2.9 MC for wide temperature range applications, there is a choice of three overall frequency tolerances of ± 0.002 percent (CR-69/U special permission required), ± 0.0025 percent (CR-66/U), and 0.005 percent (CR-78/U and CR-64/U), and the HC-18/U crystal holder is available for applications where small size is important. The CR-66/U gives a 2-to-1 improvement in overall frequency tolerance over the other types above 3 MC. However, greater care is required in its manufacture, and a higher cost can be expected.

Among the temperature controlled units, the CR-62/U gives the best overall frequency tolerance. However, its comparatively low operating temperature only allows its use in applications where the ambient temperature does not exceed approximately 65°C . The higher temperature types can be used in ambient temperatures of up to approximately 75°C , but at the expense of a doubling of the overall frequency tolerance.

TABLE 8-1. ANTI-RESONANCE CRYSTAL UNITS IN THE 0.8 TO 25-MC RANGE

Frequency Range (MC)	Temperature Range (°C)	Overall Frequency Tolerance (±%)	Equivalent Resistance	Dissipation Rating (MW)	Loading Capacitance (PF)	Max C ₀ (PF)	Crystal Unit Type	Crystal Holder Type
WIDE TEMPERATURE RANGE TYPES								
0.8 to 20	-55 to +105	0.005	625 to 20	10 and 5	32	7	CR-18A/U	HC-6/U
0.8 to 20	-55 to +105	0.005	625 to 20	10 and 5	32	7	CR-58A/U	HC-17/U
2.9 to 20	-55 to +105	0.002	175 to 25	5	30	7	CR-69/U	HC-18/U
3 to 20	-55 to +105	0.0025	60 to 25	10 and 5	30	7	CR-66/U	HC-6/U
3 to 20	-55 to +105	0.005	175 to 25	5	30	7	CR-78/U	HC-25/U
4 to 20	-55 to +105	0.005	120 to 25	5	30	7	CR-64/U	HC-18/U
10 to 25	-55 to +105	0.005	65 to 17	2.5	32	12	CR-33A/U	HC-6/U
TEMPERATURE CONTROLLED TYPES								
0.8 to 20	+70 to +80	0.002	625 to 20	5 and 2.5	32	7	CR-27A/U	HC-6/U
0.8 to 20	+80 to +90	0.002	625 to 20	5 and 2.5	32	7	CR-36A/U	HC-6/U
0.8 to 20	+70 to +80	0.001	600 to 20	5 and 2.5	32	7	CR-62/U	HC-6/U
3 to 20	+70 to +80	0.002	40 to 15	5	32	7	CR-68/U	HC-6/U
4.5 to 5.5	±0.5 (65 to 77°C)	0.00008	100 to 175		32	4	CR-71/U	HC-30/U

The crystal unit maximum equivalent resistance varies considerably as a function of frequency as shown in Figure 8-2 for the CR-18A/U and the CR-64/U types. These plots are also representative of $R_{e\max}$ in the other available types. The minimum value of equivalent resistance likely to be found is possibly about $1/9$ of $R_{e\max}$.

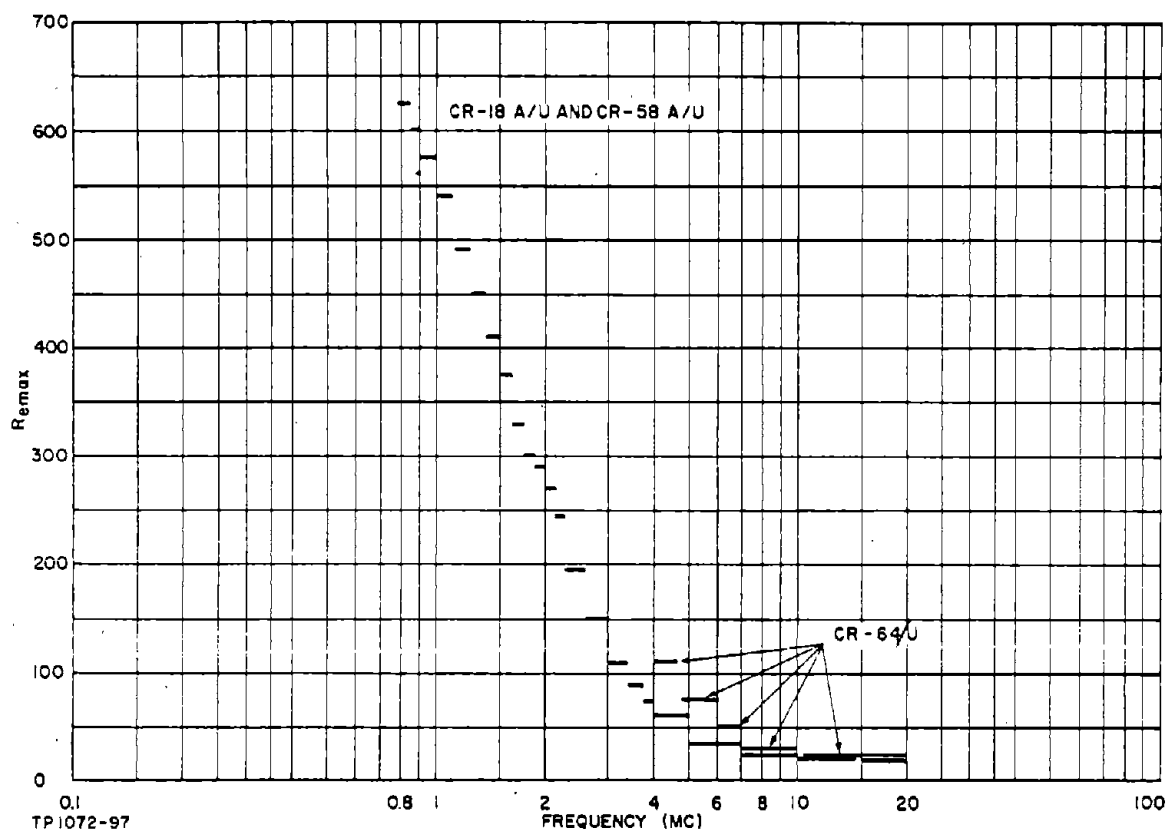


Figure 8-2. Variation of $R_{e\max}$ with Frequency

The equivalent series inductive reactance of the crystal unit at its intended operating frequency is equal to the reactance of the specified loading capacitance C_L which is either 30 or 32 PF. To avoid ambiguity, a loading capacitor of 32 PF is assumed throughout the subsequent discussion. The changes involved when designing for a 30-PF loading capacitance are minor and should be evident. The behavior of the equivalent series inductive reactance of a crystal unit designed to operate with a 32-PF loading capacitance is shown in Figure 8-3 as a function of frequency.

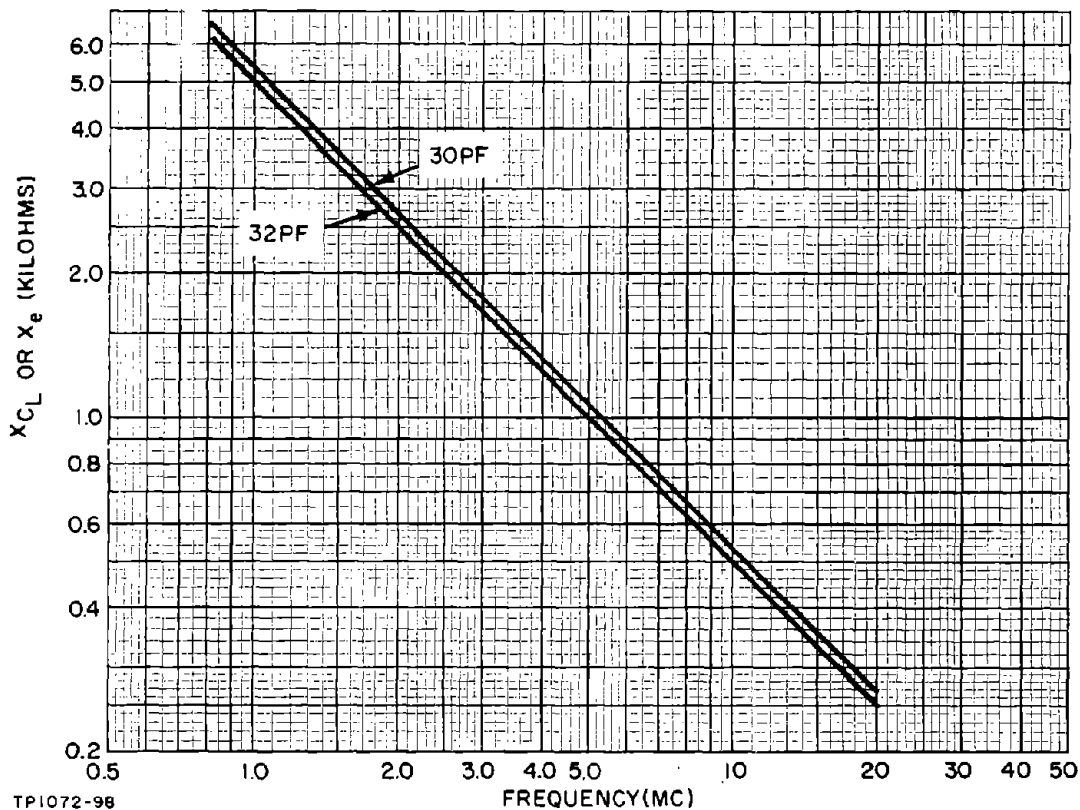


Figure 8-3. Value of X_{CL} or X_e for 30 and 32PF Loading Capacitors

8-3. Relationship Between C_L and f'_a

The actual anti-resonance frequency f'_a of the crystal unit and loading capacitance combination is determined by the value of C_L , the loading capacitance. In view of this critical relationship, it is desirable to know the effect of small changes in C_L on f'_a . f'_a is also a function of R_1 , L_1 , C_1 , and C_0 , and since a mathematical solution requires a knowledge of the values of these parameters which requires experimentation, it is simpler to experimentally determine the C_L - f'_a relationship directly. Tests were made on a number of CR-18A/U units using a CI Meter, and the results are shown in Table 8-2.

In Table 8-2 the asterisks denote that these crystals were artificially constructed "worst case" units, with the crystal equivalent resistance increased to a value of $R_{e_{max}}$ by means of a series resistor. The range of values shown for the 20-MC crystal is due to a measurement discrepancy. The value depended on the sequence in the series circuit of the added resistor, the loading capacitor, and the crystal unit. This range of frequency values for the 20-MC "worst case"

TABLE 8-2. f_a' CHANGE DUE TO C_L CHANGE

Crystal Unit Frequency (MC)	R_e (Ohms)	Change in f_a' (PPM) for 1-PF Change in C_L (32 PF Nominal)	Change in f_a' (PPM) Per Percent Change in C_L
1	230	3	1
* 1	600	3	1
3	35	6	2
3	14	8	3
5	24	9	3
* 5	60	8	2.7
13	9	8	2.7
20	8	8	2.7
*20	20	12 - 21	4 - 7

* Artificially constructed "Worse-Case" Units

unit is of doubtful accuracy. A value of 8 to 12 PPM would probably be the correct range for a true "worst case" crystal. At the lower frequencies the added resistors had no influence on the frequency change.

These results show that the change in anti-resonance frequency of a CR-18A/U crystal unit varies from 1 PPM per percent change in C_L at the low-frequency end of the range to probably 3 PPM per percent change in C_L at the high-frequency end of the range. For frequencies above 3 MC, the relationship appears to be constant at about 3 PPM per percent change in C_L .

In practice C_L consists of a network of three capacitors plus the amplifier input capacitance and, in the case of the basic Pierce circuit, the amplifier output capacitance. Above 3 MC it is therefore necessary that the capacitance presented to the crystal unit by this network should not vary by more than, say, 1 or 2 percent due to all causes if the oscillator frequency tolerance is not to unduly exceed that of the crystal unit. The input capacitance of transistor amplifiers is quite variable, both between individual transistors and with temperature. It is therefore necessary that the physical capacitance placed in parallel with the amplifier input should be as large as possible so that the percentage variation of the whole is minimized.

In the vicinity of 1 MC a threefold reduction in frequency sensitivity occurs and a corresponding relaxation in the tolerance of C_L is possible for the same oscillator frequency stability.

8-4. Relationship Between X_e and R_{\max}

In the Pierce type oscillator the crystal unit acts as the inductive element of a π network of the type discussed in Paragraph 1-10. One of the important characteristics governing the operation of the crystal π network is the ratio of $\frac{X_{\text{Leff}}}{R_{\max}}$ where:

$$X_{\text{Leff}} = X_e - X_{C_\ell} - X_{C_S} \quad (8-1)$$

The maximum value of X_{Leff} is X_e , the crystal unit equivalent series reactance and, therefore, the maximum possible value of $\frac{X_{\text{Leff}}}{R_{\max}}$ is $\frac{X_e}{R_{\max}}$.

The behavior of $\frac{X_e}{R_{\max}}$ for a CR-18A/U crystal unit is shown in Figure 8-4. This plot gives the upper limit of the ratio $\frac{X_{\text{Leff}}}{R_{\max}}$ that can be employed. In practice, because of the presence of the capacitive π network components, smaller ratios must be used.

Other crystal unit types have essentially the same $\frac{X_e}{R_{\max}}$ characteristic.

8-5. Basic Pierce Transistor Oscillators in the 0.8 to 2 MC Range

The basic Pierce oscillator circuit to be discussed is of the form shown in Figure 8-5. As will be shown subsequently, this circuit does not lend itself readily to relatively high power output applications, except under conditions which necessitate exorbitantly high amplifier power dissipation. At low power output levels, while the circuit power conversion efficiency does not improve greatly, it is not usually then of great importance, and the circuit simplicity justifies the use of this oscillator. In general, the output power capability of this oscillator is less than $0.4 P_{\text{CMAX}}$, where P_{CMAX} is the rated crystal unit dissipation.

Relating this to the crystal unit dissipation rating given in Table 8-1 shows that oscillator output powers in the regions of 4 MW below 10 MC and 2 MW between 10 and 20 MC represent the upper limit. In many transistor oscillator applications this level of power output is adequate. A particular case is that of a mixer injection source in receivers. In this application the signal

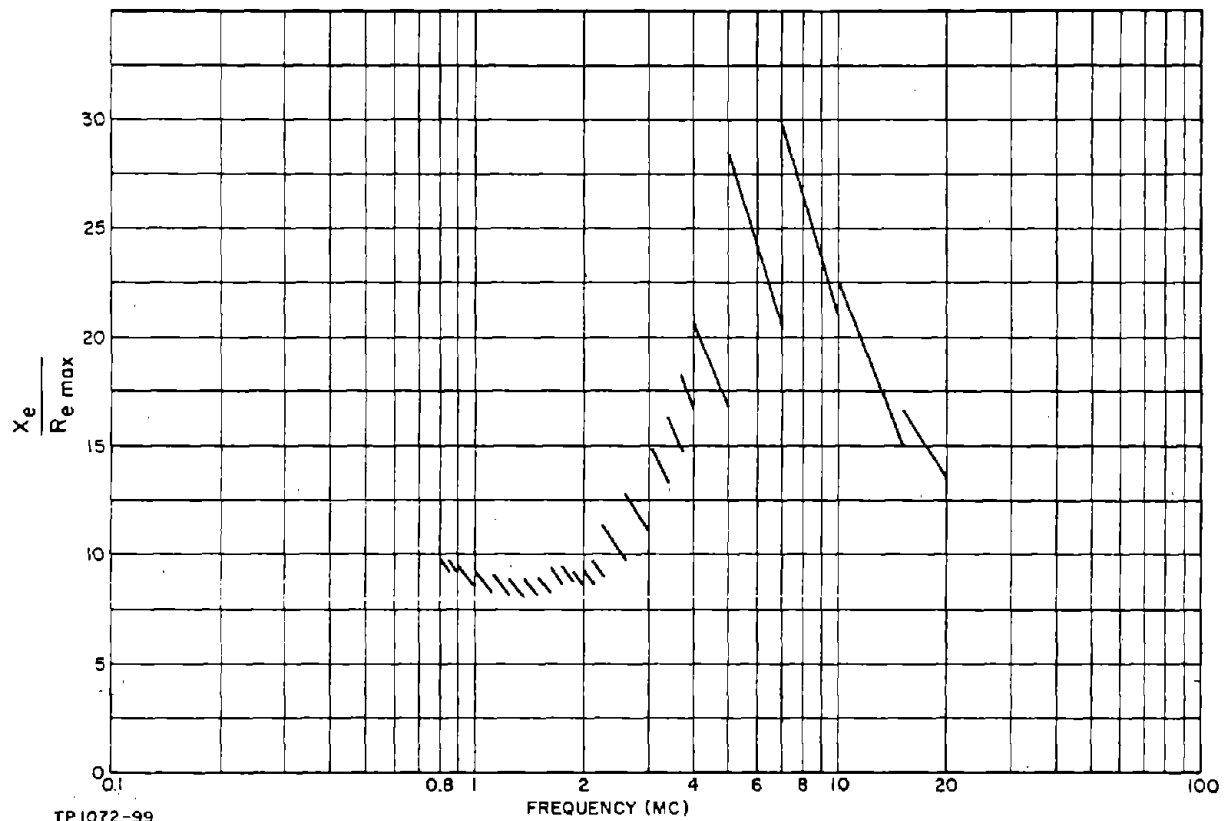
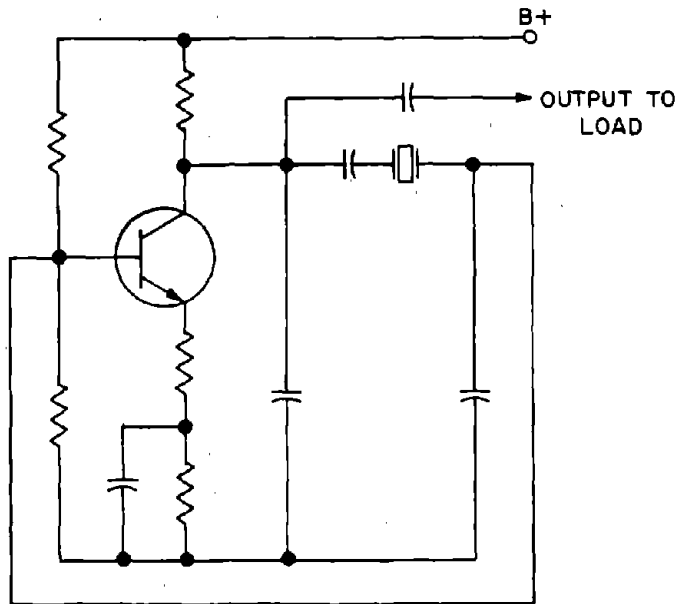
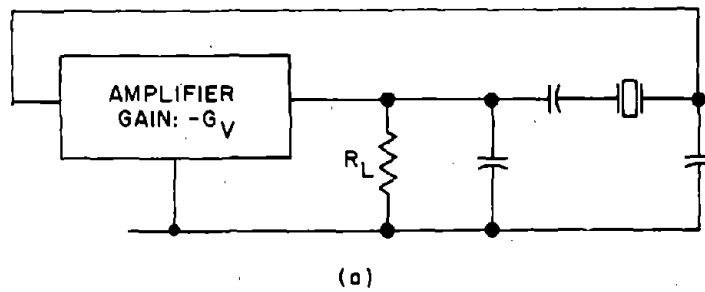


Figure 8-4. Variation of $\frac{X_e}{R_{e \max}}$ With Frequency for a CR-18A/U Crystal Unit

frequency to be heterodyned is often fed to the base of the mixer transistor and the oscillator injection frequency to the emitter at a 150- to 300-MV RMS level. The local oscillator injection power required to give efficient frequency conversion is approximately 1 MW, a power level within the capability of the basic Pierce oscillator. This is probably the greatest single application of low power crystal oscillators, and the following discussion is directed to this usage. It is not convenient at this point to justify these statements; this is reserved for Paragraph 8-14 where an illustrative example is given.

8-6. Design Approach

In developing a design procedure it is necessary to know the amplifier input and output impedance and in particular the resistive components in order that the crystal π network loading can be determined. In this circuit the crystal π network is a direct load on the amplifier output while the amplifier input is a direct load on the π network. Furthermore, since crystal unit $\frac{d\phi}{df}$ degradation considerations dictate that the oscillator external load R_L must be several times



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(b)

Figure 8-5. Basic Pierce Oscillator Circuit

greater than the input impedance of the π network for a worst-case design, the π network input impedance constitutes the major portion of the amplifier load. Because of the inherent feedback within the transistor, the amplifier input impedance is extremely dependent on the amplifier load impedance. Consequently, the amplifier input impedance is to a great extent a function of the π network characteristics, which are in turn determined by the amplifier input and output impedances and voltage gain. The amplifier and feedback network characteristics are therefore closely interrelated and must be simultaneously considered during the design process unless a degree of separation between the operations of amplification and feedback can be artificially introduced. Both the amplifier and π network design equations are complex, and the direct approach is unwieldy in all but the simplest cases. An alternative approach where, for the purposes of calculation, a greater separation between the amplification and feedback functions is obtained, is desirable.

It is possible to achieve this by converting the hybrid- π equivalent transistor circuit into the "true" π network discussed in Paragraph 3-25 and shown in Figure 3-16. The equivalent internal feedback elements R_r and C_r of the transistor now appear between the base and collector and hence between the π network input and output terminals (see Figure 8-5). If R_r and C_r are now considered to be transferred to the crystal π network, the amplifier is effectively unilateralized and the amplifier input and output impedances are no longer dependent on the amplifier load and driving source impedances, respectively.

While simplifying the amplifier design approach, the transference of C_r and R_r complicates the crystal π network design and it is first necessary to evaluate the effect of these additional components on the performance of the π network. This is the purpose of the following analysis.

8-7. Incorporation of Transistor Feedback Elements C_r and R_r into the Crystal π Network

Combining the transistor internal feedback elements C_r and R_r into the crystal π network gives the circuit shown in Figure 8-6 (a). The purpose of this analysis is to resolve the series-parallel circuit shown in solid lines in Figure

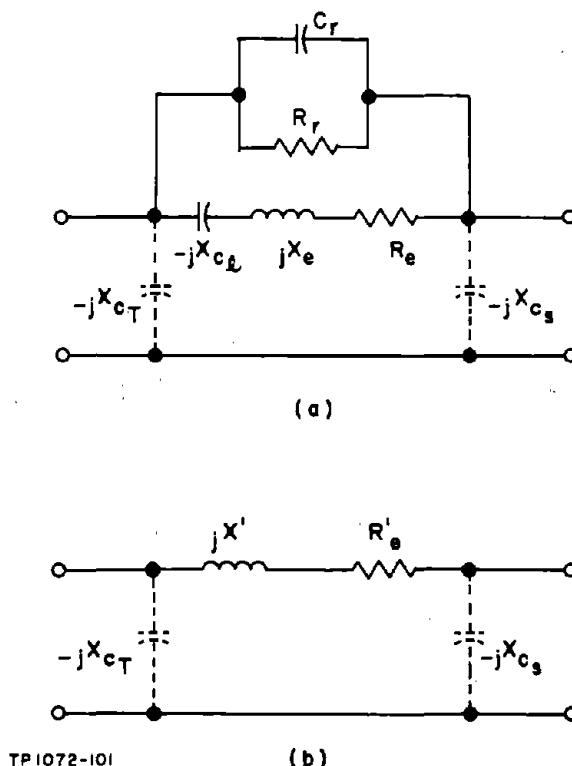


Figure 8-6. Equivalent Circuit of C_r , R_r , and the Crystal π Network

8-6 (a) into the series circuit shown in Figure 8-6 (b). R_e and $(X_e - X_{C\ell})$ can then be compared with X' and R'_e to determine the changes incurred and, in particular, the $\frac{d\phi}{dX_e}$ degradation suffered.

It is first necessary to obtain an idea of the relative magnitudes of X_{C_r} , R_r , $(X_e - X_{C\ell})$, and R_e so that suitable approximations can be made in the analysis. The characteristics of the CR-18A/U crystal unit are typical of the other types, and analyzing the effect for this crystal unit gives results that are applicable to the others. The CR-18A/U crystal unit X_e is the reactance of a 32 PF capacitor and varies from 6250 ohms at 800 KC to 250 ohms at 20 MC. The value of $X_{C\ell}$ is dependent on the $\frac{X_{Leff}}{R_{max}}$ ratio chosen for a design. Crystal dissipation and feedback network voltage attenuation ratio together dictate small $\frac{X_{Leff}}{R_{max}}$ ratios (1 to 3) at low frequencies and higher ratios (3 to 8) at the higher frequencies of the range. Therefore, $(X_e - X_{C\ell})$ will normally be less than 3 K (approximately $0.5 X_e$) at 800 KC and less than 200 ohms (approximately $0.8 X_e$) at 20 MC. At intermediate frequencies, $(X_e - X_{C\ell})$ will gradually vary from $0.5 X_e$ to $0.8 X_e$ with increasing frequency.

R_{max} varies from 625 ohms at 800 KC to 20 ohms at 20 MC, roughly following an inverse frequency relationship up to 3 MC (150 ohms) and then decreasing at a less rapid rate.

Equation (3-81) shows that C_r has a maximum value approximately equal to C_{cb}' . C_{cb}' has a value of 5 PF or less for transistors with f_T 's of 200 MC or greater and, therefore, X_{C_r} is at least eight times greater than $(X_e - X_{C\ell})$.

The relative value of R'_r (that part of R_r due to C_{cb}') can be determined by comparison with X_{C_r} . From Equations (3-78 and (3-81):

$$\frac{R'_r}{X_{C_r}} = \frac{r \left[1 + \frac{C_{b'e}'}{C_{cb}'} + \frac{X_{C_{cb}'} \cdot X_{C(p)}}{r^2} \right]}{X_{C_{cb}'} \left[1 + \left(\frac{r}{X_{C_{be}'}} \right)^2 \right]} \quad (8-2)$$

Discarding the 1 in the bracketed numerator term of Equation (8-2) since it is small compared with $\frac{X_{C_{cb}'} \cdot X_{C(p)}}{r^2}$ gives:

$$\frac{R'_r}{X_{C_r}} \approx \frac{X_{C_{b'e}'}}{r} \quad (8-3)$$

R'_r will have its minimum value at the highest frequency. For transistors with f_T 's greater than 200 MC, $\frac{X_{C_{be}}}{r}$ at 20 MC typically has a value greater than 1. Therefore, R'_r is equal to or greater than X_{C_r} at 20 MC and, since $X_{C_{be}}$ is an inverse function of frequency, the ratio of $\frac{R'_r}{X_{C_r}}$ increases with decreasing frequency, having a value of, say, 25 to 75 at 800 KC.

R''_r , that part of R_r due to R_D , has a value of from R_D to $2R_D$ in the 0.8 to 20 MC frequency range. Suitable emitter current levels for the basic Pierce oscillator circuit lie below 10 MA, and R_D will then usually be greater than 100 K which is greater than 30 times $(X_e - X_{C_L})$ under the worst condition. Therefore, at low frequencies R_r will be approximately equal to R''_r , while at the higher frequencies R'_r will determine the value of R_r .

The following relationships have been established:

$$(X_e - X_{C_L}) < 0.5 X_e \text{ at } 800 \text{ KC}$$

$$(X_e - X_{C_L}) < 0.8 X_e \text{ at } 20 \text{ MC}$$

$$X_{C_r} > 8 (X_e - X_{C_L}) \text{ at } 20 \text{ MC}$$

$$X_{C_r} > 12 (X_e - X_{C_L}) \text{ at } 800 \text{ KC}$$

$$R_r > 8 (X_e - X_{C_L}) \text{ at } 20 \text{ MC}$$

$$R_r > 30 (X_e - X_{C_L}) \text{ at } 800 \text{ KC}$$

$$20 \text{ ohms} \leq R_{e\max} \leq 625 \text{ ohms}$$

The analysis is given in two parts, considering the effects of C_r and R_r separately.

8-8. Effect of C_r

Omitting R_r from the network shown in solid lines in Figure 8-6 (a) results in the following expression for the impedance Z' of the network:

$$Z' = - \frac{j X_{C_r} \left[1 + j \frac{X_e - X_{C_L}}{R_e} \right]}{1 + j \left(\frac{X_e - X_{C_L} - X_{C_r}}{R_e} \right)} \quad (8-4)$$

The real part of Z' , R'_e is then:

$$R'_e = \frac{(X_{C_r})^2}{R_e \left[1 + \left(\frac{X_e - X_{C_l} - X_{C_r}}{R_e} \right)^2 \right]} \quad (8-5)$$

It has been shown that $X_{C_r} \gg (X_e - X_{C_l})$ or R_{\max} . Therefore:

$$\begin{aligned} R'_e &\approx R_e \left(\frac{X_{C_r}}{X_e - X_{C_l} - X_{C_r}} \right)^2 \\ &= R_e \cdot \frac{1}{\left(1 - \frac{X_e - X_{C_l}}{X_{C_r}} \right)^2} \end{aligned} \quad (8-6)$$

Substituting 0.125 for $\frac{X_e - X_{C_l}}{X_{C_r}}$ from the previously estimated relative values (worst case, 20 MC) gives:

$$R'_e \approx 1.3 R_e \quad (8-7)$$

The apparent crystal equivalent resistance is increased 30 percent due to the presence of C_r . At lower frequencies the effective increase in crystal equivalent resistance will be less, amounting to a 14-percent increase in R_e at 800 KC for the relative circuit values previously quoted. However, these values are conservative, and the effect is likely to be smaller in practice.

The imaginary part of Equation (8-4) is:

$$X' = \frac{X_{C_r} \left[\frac{X_e - X_{C_l}}{R_e^2} (X_{C_r} + X_{C_l} - X_e) - 1 \right]}{\left[1 + \left(\frac{X_{C_r} + X_{C_l} - X_e}{R_e} \right)^2 \right]} \quad (8-8)$$

The unity terms in both numerator and denominator are small relative to the other terms and can be ignored. Therefore:

$$X' \approx \frac{(X_e - X_{C_l})}{\left(1 - \frac{X_e - X_{C_l}}{X_{C_r}} \right)} \quad (8-9)$$

For $\frac{X_e - X_{C_l}}{X_{C_r}} = 0.125$ (worst case, 20 MC):

$$X' \approx 1.14 (X_e - X_{C\ell}) \quad (8-10)$$

That is, for the assumed circuit conditions, the effective reactance of $(X_e - X_{C\ell})$ is increased by 14 percent due to the presence of C_r . At lower frequencies the effect is reduced, amounting to an increase of 7 percent in $(X_e - X_{C\ell})$ at 800 KC for the relative circuit values previously quoted.

8-9. Effect of R_r

Omitting C_r from the network shown in solid lines in Figure 8-6 (a) gives the following network impedance expression:

$$Z' = \frac{R_r \cdot R_e}{R_r + R_e} \cdot \left[\frac{1 + j \left(\frac{X_e - X_{C\ell}}{R_e} \right)}{1 + j \left(\frac{X_e - X_{C\ell}}{R_e + R_r} \right)} \right] \quad (8-11)$$

The real part of Z' is:

$$R'_e = \frac{R_r \cdot R_e}{R_r + R_e} \cdot \left[\frac{1 + \frac{(X_e - X_{C\ell})^2}{R_e (R_e + R_r)}}{1 + \left(\frac{X_e - X_{C\ell}}{R_e + R_r} \right)^2} \right] \quad (8-12)$$

But:

$$R_r \gg R_e \quad (8-13)$$

and:

$$\frac{X_e - X_{C\ell}}{R_e + R_r} \ll 1 \quad (8-14)$$

Therefore:

$$R'_e \approx R_e \left[1 + \frac{(X_e - X_{C\ell})^2}{R_e \cdot R_r} \right] \quad (8-15)$$

The presence of R_r therefore effectively increases the value of R_e .

The extent of this effect can be illustrated by a numerical example. For $f = 20$ MC, $\frac{X_{Leff}}{R_{emax}} = 5$, $R_{emax} = 20$ ohms, and $R_r \approx X_{Ccb}' (5 \text{ PF}) = 1.6 \text{ K}$, $\frac{X_e - X_{C\ell}}{R_{emax}}$ will be greater than $\frac{X_{Leff}}{R_{emax}}$ having a value of, say, 7. Then, for a worst-case crystal unit ($R_e = R_{emax}$):

$$R'_{\text{emax}} \approx R_{\text{emax}} \left[1 + 7 \times \frac{140}{1600} \right] = 1.6 R_{\text{emax}} \quad (8-16)$$

This would result in a $\frac{d\phi}{dX_e}$ degradation of 38 percent. The use of lower $\frac{X_{\text{Leff}}}{R_{\text{emax}}}$ ratios causes a marked reduction in this effect.

The imaginary part of Equation (8-11) is:

$$X' = (X_e - X_{C\ell}) \left[\frac{\frac{R_r}{R_e + R_r} - \frac{R_r \cdot R_e}{(R_e + R_r)^2}}{1 + \left(\frac{X_e - X_{C\ell}}{R_e + R_r} \right)} \right] \quad (8-17)$$

For the conditions given, X' can be approximated as:

$$X' = (X_e - X_{C\ell}) \quad (8-18)$$

Therefore, the effective series reactance is unchanged by the presence of R_r .

Combining the effects of C_r and R_r gives:

$$R'_e \approx R_e \frac{\left[1 + \frac{(X_e - X_{C\ell})^2}{R_e \cdot R_r} \right]}{\left(1 - \frac{X_e - X_{C\ell}}{X_{C_r}} \right)} \quad (8-19)$$

$$X' \approx \frac{(X_e - X_{C\ell})}{\left(1 - \frac{X_e - X_{C\ell}}{X_{C_r}} \right)} \quad (8-20)$$

The effect of C_r and R_r on the effective reactance of the mid-section of π network is relatively small and can be accounted for by a small adjustment in the value of C_{ℓ} . The effect of C_r and R_r on the effective resistance of the mid-section of the π network is more severe. With the numerical values previously quoted for a 2N706A at 20 MC (the most demanding condition), R'_{emax} is approximately twice R_{emax} and the π network $\frac{d\phi}{dX_e}$ is degraded to approximately 50 percent of that of the crystal unit. As stated previously, the numerical values used in this calculation are extreme, and the degradation is not likely to be quite so severe. However, it is still likely to be larger than desired, and methods of minimizing the effect are required.

Examination of Equation (8-19) shows that R'_e will approach more closely to R_e as R_r and X_{C_r} are increased. The most obvious method is to use a transistor with smaller values of $C_{cb'}$ and $C_{b'e}$, which will increase both X_{C_r} and R_r . This is only possible at the present time by using more costly transistors. Another approach which yields a partial solution is to use emitter degeneration. This will result in an increase in R_r at the higher frequencies, causing a reduction in crystal loading. Further improvement can only be gained by minimizing the term $(X_e - X_{C_L})$ to the greatest extent consistent with transistor biasing considerations to be discussed later.

The voltage attenuation ratio of the crystal π network is also affected by the inclusion of C_r and R_r in the circuit. Substituting for X_{Leff} and R_{emax} in Equation (1-84) in terms of X' and R'_{emax} gives the modified attenuation ratio:

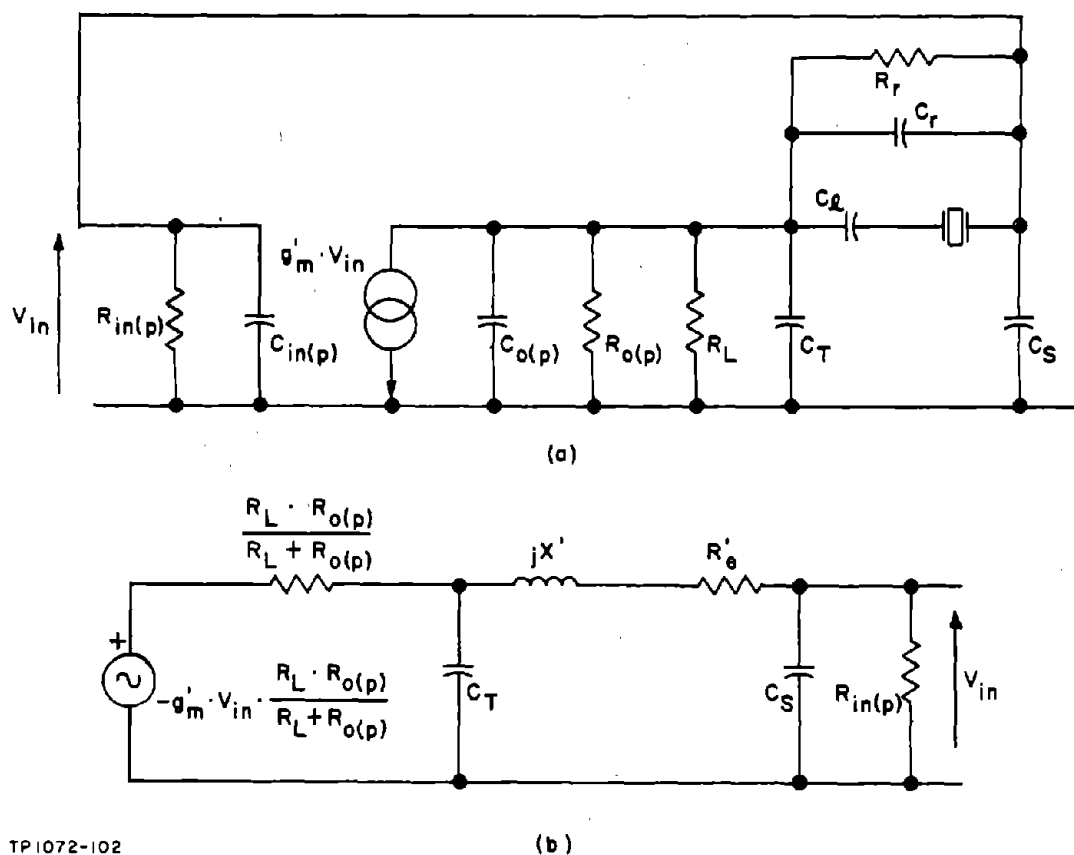
$$A'_V = - \frac{X_{C_S}}{X' - X_{C_S}} \cdot \left[\frac{1}{1 + \frac{R}{X_{C_T}} \cdot \frac{R'_{emax}}{X' - X_{C_S}}} \right] \quad (8-21)$$

8-10. Calculation of Loop Voltage Gain

Using the π equivalent transistor circuit and transferring R_r and C_r to the π network, the basic Pierce oscillator circuit is as shown in Figure 8-7 (a), where $R_{in(p)}$ and $C_{in(p)}$ are the short-circuit parallel input impedance components of the transistor amplifier including the base biasing network, and $C_{o(p)}$ and $R_{o(p)}$ are the short-circuit parallel output impedance components of the transistor amplifier. Replacing the current generator and the parallel combination of $R_{o(p)}$ and R_L by the equivalent voltage generator and series resistance (Norton's Transformation), incorporating R_r and C_r into the crystal π network as detailed in Paragraph 8-7, and adding $C_{in(p)}$ and $C_{o(p)}$ into C_S and C_T , respectively, gives the circuit of Figure 8-7 (b). Figure 8-7 (b) is of the same form as that previously analyzed in Paragraph 1-10 and, therefore, the design equations developed there are applicable to the design of the basic Pierce oscillator provided the effects of R_r and C_r are taken into account using Equations (8-19) and (8-20) and R_L and $R_{o(p)}$ in parallel are substituted for R .

The signal source voltage is now equal to the output voltage of the amplifier when loaded with R_L , and the design process simply consists of equating the amplifier voltage gain to the crystal π network attenuation, while satisfying the crystal loading conditions. The latter entails the determination of suitable values for R_L , $R_{o(p)}$, $R_{in(p)}$, and R_r .

In this frequency range the crystal unit characteristics are such that the amplifier voltage gain required is not excessive and can be readily achieved even when a large amount of emitter degeneration is employed. This is particularly



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Figure 8-7. "Basic" Pierce Oscillator Circuit Used for Loop Voltage Gain Analysis

true since the higher amplifier voltage gains are required at the low end of the frequency range where the crystal unit impedance is large compared to the transistor parallel input resistance. The amplifier parallel input resistance is then usually less than $3.6 R_{\text{emax}}$ and the ratio of X_{C_S} to $R_{\text{in}(p)}$ is governed by phase angle limited operating conditions; that is, X_{C_S} equal to or less than $1/6 R_{\text{in}(p)}$. It was shown in Paragraph 3-24 that the voltage gain-parallel input resistance product of a transistor amplifier is practically constant independent of the emitter degeneration employed. Consequently, the introduction of an emitter degeneration resistor increases $R_{\text{in}(p)}$ to the same extent that it decreases the amplifier voltage gain. Therefore, provided $R_{\text{in}(p)}$ remains less than $3.6 R_{\text{emax}}$, the increase in $R_{\text{in}(p)}$ allows a similar increase in X_{C_S} which, as shown by Equation (1-84), will result in a decrease of the π network voltage attenuation comparable to the decrease in amplifier voltage gain.

At the higher frequencies of the range, the crystal unit impedance is of the same magnitude as the amplifier parallel input resistance, and the π network attenuation and the amplifier voltage gains required are of the order of 10 to 20.

Reference to the amplifier voltage gain plots shown in Figure 3-6, 3-7 and 3-8 shows that this order of voltage gain can easily be achieved at frequencies in the vicinity of 20 MC using a large amount of emitter degeneration.

The advantages gained from using emitter degeneration are:

- (a) The amplifier voltage gain is made virtually independent of r_e and $r_{bb'}$, thereby reducing the gain spread between transistors.
- (b) The amplifier characteristics are made less frequency dependent and in particular, at all frequencies up to 20 MC the low frequency voltage gain expression gives an adequate estimate, provided the emitter resistor is sufficiently large.
- (c) The amplifier parallel output resistance is increased to a value where it can normally be neglected in the design calculation.
- (d) The value of R_F is increased at high frequencies, thereby reducing its π network loading effect.

Suitable values for the unbypassed emitter resistor appear to be 30 ohms or larger. This results in an amplifier voltage gain which is for all practical purposes independent of frequency in the 0.8 to 20 MC range for the amplifier loads normally encountered.

For these conditions, the amplifier voltage gain becomes:

$$\begin{aligned}
 G_V &= G'_m \cdot R_L \cdot \frac{R_{b'E}}{R_{b'E} + r_{bb'}} \\
 &= \frac{\alpha_o \cdot R_L}{r_e + r_E + r_{bb'}(1 - \alpha_o)}
 \end{aligned} \tag{8-22}$$

and the loop voltage gain is:

$$G_{VL} = G_V \cdot A'_V \tag{8-23}$$

where A'_V is given by Equation (8-21).

A'_V is almost directly proportional to X_{CS} which is in turn determined by the amplifier input resistance by the conditions of Equations (1-96) or (1-100), depending on whether π network phase angle or crystal input loading conditions apply. In practice the difference between A'_V and A_V is small, and it is convenient to use A_V during the preliminary loop gain calculation, introducing a correction if necessary at a later stage of the design to account for the discrepancy.

While this approach is useful in establishing the oscillator loop voltage gain and the crystal unit loading, it does not define the circuit voltage and current levels. In this circuit, the collector signal voltage corresponds to V_π , the voltage across C_T in the analysis of Paragraph 1-11, and the permissible value of collector signal voltage V_{Omax} is given by Equation (1-113). This equation shows that for a given $\frac{X_{Leff}}{R_{emax}}$ ratio, V_{Omax} will have its smallest value when the product ($P_{CMAX} \cdot R_{emax}$) has its minimum value. In this frequency range both the crystal unit power dissipation rating and the maximum equivalent resistance decrease with increasing frequency, and the most stringent conditions are placed on the collector signal voltage at 20 MC.

For a CR-18A/U crystal unit at 20 MC, P_{CMAX} is 5 MW and R_{emax} is 20 ohms. Inserting these values into Equation (1-113) together with suitable values of $\frac{X_{Leff}}{R_{emax}}$ gives:

$$\text{For } \frac{X_{Leff}}{R_{emax}} = 1, \quad V_{Omax} = 0.45 \text{ VRMS}$$

$$\text{For } \frac{X_{Leff}}{R_{emax}} = 3, \quad V_{Omax} = 1 \text{ VRMS}$$

$$\text{For } \frac{X_{Leff}}{R_{emax}} = 6, \quad V_{Omax} = 1.9 \text{ VRMS}$$

These values show that the allowable collector signal voltage at 20 MC is severely limited. At lower frequencies the effect is less severe since both P_{CMAX} and R_{emax} increase. For example, at 800 KC, P_{CMAX} is 10 MW and R_{emax} is 625 ohms. Inserting these values into Equation (1-113) gives:

$$\text{For } \frac{X_{Leff}}{R_{emax}} = 1, \quad V_{Omax} = 3.5 \text{ VRMS}$$

$$\text{For } \frac{X_{Leff}}{R_{emax}} = 2, \quad V_{Omax} = 5.6 \text{ VRMS}$$

The collector current requirements are determined by the collector load impedance. This consists of R_L in parallel with the π network input impedance as viewed across C_T . The purpose of the following discussion is to determine the collector load impedance and the collector current requirements.

8-11. Behavior of R_π and R_T as a Function of $\frac{R_e}{R_{\max}}$ and $\frac{X_{\text{Leff}}}{R_{\max}}$

The amplifier resistive load R_T is the parallel combination of the actual oscillator load R_L and the feedback network parallel input resistance, which is, in this circuit, the crystal π network parallel input resistance R_π . R_π is an inverse function of R_e and therefore can vary over a 9-to-1 range with the R_e spread likely to be encountered in crystal units. π network $\frac{d\phi}{dX_e}$ degradation considerations stipulate that R_L will have a value intermediate between the extreme values of R_π , $R_{\pi\min}$, and $R_{\pi\max}$. Consequently, R_π forms a large part of R_T which will therefore also vary considerably with crystal interchange.

If it is assumed that R_L is much smaller than the amplifier output resistance $R_o(p)$, the π network input loading will then be solely due to R_L which then replaces R in the analysis of Paragraph 1-10 insofar as π network input loading is concerned. Figure 8-8 shows the plot of $\frac{R}{R_{\max}}$ which can now be construed as a plot of $\frac{R_L}{R_{\max}}$. Therefore, for a given $\frac{X_{\text{Leff}}}{R_{\max}}$ ratio it is possible to determine R_L , R_T , and the effective parallel input resistance of the π network as seen across C_T , in terms of $R_{e\max}$ as a function of $\frac{R_e}{R_{\max}}$ from the equations:

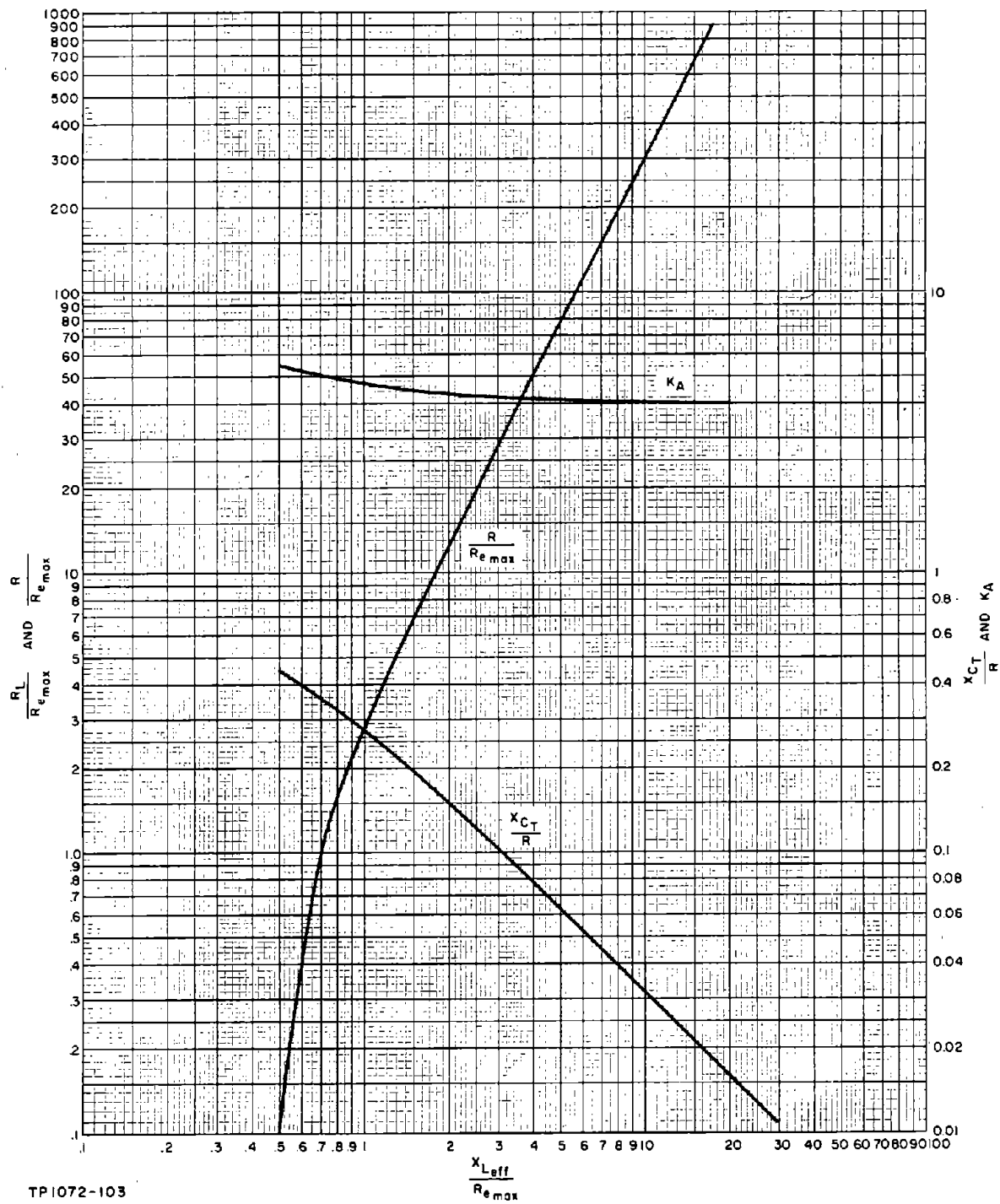
$$\frac{R_\pi}{R_{e\max}} = \frac{R_e}{R_{\max}} \left[1 + \left(\frac{X_{\text{Leff}}}{R_{\max}} \cdot \frac{R_{\max}}{R_e} \right)^2 \right] \quad (8-24)$$

(series-to-parallel transform of X_{Leff} and R_e)

and:

$$\frac{R_T}{R_{\max}} = \frac{\frac{R_L}{R_{\max}} \cdot \frac{R_\pi}{R_{\max}}}{\frac{R_L}{R_{\max}} + \frac{R_\pi}{R_{\max}}} \quad (8-25)$$

Inserting numerical values of $\frac{X_{\text{Leff}}}{R_{\max}}$ and assumed values of $\frac{R_{\max}}{R_e}$ into Equation (8-24) gives values of $\frac{R_\pi}{R_{\max}}$. These values can then be inserted into Equation (8-25) together with corresponding values of $\frac{R_L}{R_{\max}}$ to give values of $\frac{R_T}{R_{\max}}$ as a function of $\frac{R_e}{R_{\max}}$ and $\frac{X_{\text{Leff}}}{R_{\max}}$. The behavior of R_T relative to its minimum value $R_{T\min}$, which is the value obtained from Equation (8-25) for $\frac{R_e}{R_{\max}}$ equal to 1 for a given value of $\frac{X_{\text{Leff}}}{R_{\max}}$, can also be obtained from these calculations.



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Figure 8-8. K_A , $\frac{R}{R_{max}}$, and $\frac{X_{CT}}{R}$ as a Function of $\frac{X_{Leff}}{R_{max}}$

The ratio of $\frac{R_T}{R_{Tmin}}$ as a function of $\frac{R_e}{R_{emax}}$ using $\frac{X_{Leff}}{R_{emax}}$ as a parameter is plotted in Figure 8-9 which shows that for all values of $\frac{X_{Leff}}{R_{emax}}$ greater than 2, the total oscillator resistive load will vary over a range of approximately 3 to 1 with the likely crystal unit R_e spread of 9 to 1. For lower values of $\frac{X_{Leff}}{R_{emax}}$ the range of variation of R_T will be smaller, having a range of approximately 1.9 to 1 for $\frac{X_{Leff}}{R_{emax}} = 1$. However, this ignores the effect of the reactive component of the π network input impedance.

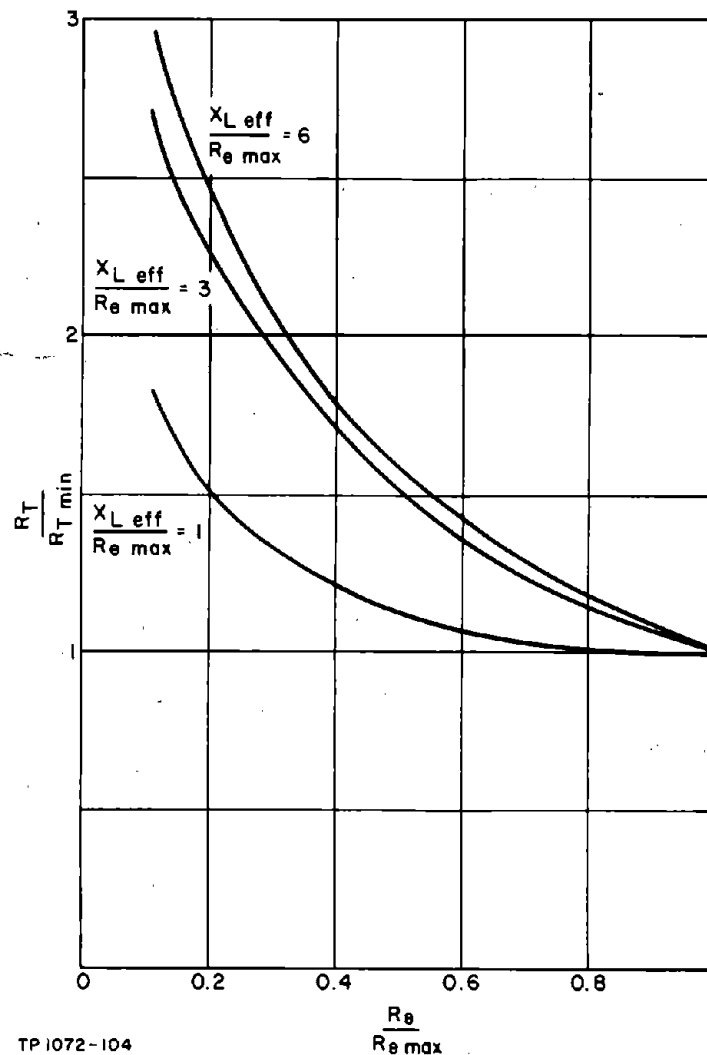


Figure 8-9. Behavior of $\frac{R_T}{R_{Tmin}}$ as a Function of R_e

The parallel input reactance of the π network, which is large compared to R_π for $\frac{X_{Leff}}{R_{max}}$ ratios larger than 2 for all values of $\frac{R_e}{R_{max}}$, becomes comparable with R_π for $\frac{X_{Leff}}{R_{max}}$ ratios much below 2 as $\frac{R_e}{R_{max}}$ approaches unity.

For example, for the condition $\frac{X_{Leff}}{R_{max}} = 1$, the amplifier total load must have a phase angle of -45 degrees to compensate for the 45-degree "excess" phase lead between π network input and output voltages due to R_{max} . The magnitude of the total amplifier load impedance is, therefore, $0.7 R_{Tmin}$ when R_e equals R_{max} , resulting in a variation of total load impedance magnitude of 2.6 to 1 with R_e variation. For higher values of $\frac{X_{Leff}}{R_{max}}$ the π network "excess" phase lead is less, requiring a smaller amplifier load phase angle and therefore a smaller π network reactive component. The amplifier total load impedance variation with crystal interchange for all $\frac{X_{Leff}}{R_{max}}$ values therefore approaches a value of 3 to 1. This is discussed further in Paragraph 8-13 where its effect on the required transistor DC collector current is determined.

8-12. Output Voltage Limiting

In the oscillator circuit in Figure 8-5 (b) the function of the resistor from B+ to collector is to parallel-feed power to the collector. However, insofar as π network loading is concerned it must be regarded as part of the oscillator load and will consume a portion of the available output power in proportion to its size relative to the true load. Unless an abnormally high supply voltage source is available, the supply of the collector-emitter DC voltage, plus a sufficient emitter-ground voltage to give adequate operating point stability, generally requires the feed resistor to be comparable with the effective external oscillator load R_L .

One effect of this is the reduction in actual oscillator output power incurred. In the frequency range up to 10 MC where 10 MW crystal units are available, this is of no consequence for the chosen application since a total output power of approximately 3 MW is obtainable without overdriving the crystal unit. Upwards of 2 MW could therefore be dissipated in the feed resistor while still leaving sufficient output power for mixer-driver applications. Above 10 MC crystal unit dissipation rating is 5 MW, and the possible output power is then less than 2 MW for the specified π network loading. The relationship between the values of feed resistor and R_L are then more critical unless increased π network loading is allowed.

Another effect which is of possibly greater importance is the relatively "soft" collector voltage limiting action obtained using a large parallel-feed resistor. Under large input signal voltage conditions, a transistor amplifier with capacitive input circuit elements tends to reverse-bias in a similar manner to a vacuum tube. The effect is less severe than for a vacuum tube, but as the input signal voltage increases some reduction in the average DC collector current occurs, with a resulting increase in emitter-collector voltage when a resistive feed is used. The likely consequence of this action can be obtained from consideration of the loop voltage gain change with crystal unit interchange. It was previously shown that the total amplifier load impedance can possibly vary over a range of approximately 3 to 1 with crystal unit interchange. The amplifier voltage gain is an approximately linear function of the load impedance, while the attenuation of the π network is essentially independent of the value of R_e . Consequently, a 3-to-1 variation in loop voltage gain can occur with crystal unit interchange. Under these conditions, when the emitter-collector DC voltage is free to vary, the limiting action will be primarily due to current limiting, and the peak output voltage will be approximately equal to the product of the DC collector current and the total load impedance. Since the latter varies over a 3-to-1 range, a corresponding variation of oscillator output voltage will occur.

This large variation of oscillator output voltage may be permissible in some applications, and it is then feasible to employ resistive collector feed. For the specific application considered here, this is not the case. Experience shows that a transistor mixer operates best with an injection signal of 200 to 350 MV and that both mixer conversion gain and signal-to-noise performance suffer when the injection signal falls outside these limits. The performance of a basic Pierce oscillator using resistive feed does not give this level of output voltage stability, and better limiting methods must be used.

Using an inductive feed stabilizes the collector-emitter DC voltage and makes it relatively independent of the base input signal voltage. This gives a "hard" collector voltage limiting action which, when combined with current limiting, results in a better oscillator output voltage stability.

8-13. Transistor Collector Current Requirements for the Basic Pierce Circuit

In setting up the transistor bias conditions the collector current must be sufficiently large to ensure that the collector signal voltage is voltage-limited rather than current-limited when the amplifier total load impedance has its minimum value. Otherwise, with a poor crystal unit in circuit, current limiting will occur which will then be superseded by voltage limiting when a better crystal unit is employed. During this transition the output voltage will increase more than necessary, with a resultant loss of output voltage stability. To ensure this condition the available collector current should be sufficient to drive the minimum collector load to be encountered.

For any given value of $\frac{X_{Leff}}{R_{emax}}$, the total load impedance has its minimum value when R_e equals R_{emax} . The resistive component R_{Tmin} for a given $\frac{X_{Leff}}{R_{emax}}$ ratio can be obtained by substituting R_{emax} for R_e in Equation (8-24) to obtain $\frac{R_{Tmin}}{R_{emax}}$ and by then substituting $\frac{R_{Tmin}}{R_{emax}}$ into Equation (8-25) to obtain $\frac{R_{Tmin}}{R_{emax}}$. The plot of $\frac{R_{Tmin}}{R_{emax}}$ as a function of $\frac{X_{Leff}}{R_{emax}}$ is given in Figure 8-10.

For ratios of $\frac{X_{Leff}}{R_{emax}}$ greater than 3, the total load impedance is essentially R_{Tmin} , but for lower ratios of $\frac{X_{Leff}}{R_{emax}}$ the total load impedance must have a relatively large parallel capacitive reactance component. This capacitive component is necessary in order to give a phase lag of amplifier output voltage relative to the amplifier input voltage in compensation for the "excess" phase lead in the π network due to R_e . The excess phase lead in the π network is:

$$\phi_I = \tan^{-1} \frac{R_{emax}}{X_{Leff}} \quad (8-26)$$

Assuming no phase shift within the transistor, the phase angle of the amplifier load must therefore be:

$$\theta = -\phi_I \quad (8-27)$$

but:

$$\begin{aligned} \theta &= -\tan^{-1} \frac{b_T}{g_T} \\ &= -\tan^{-1} \frac{R_{Tmin}}{X_T} \end{aligned} \quad (8-28)$$

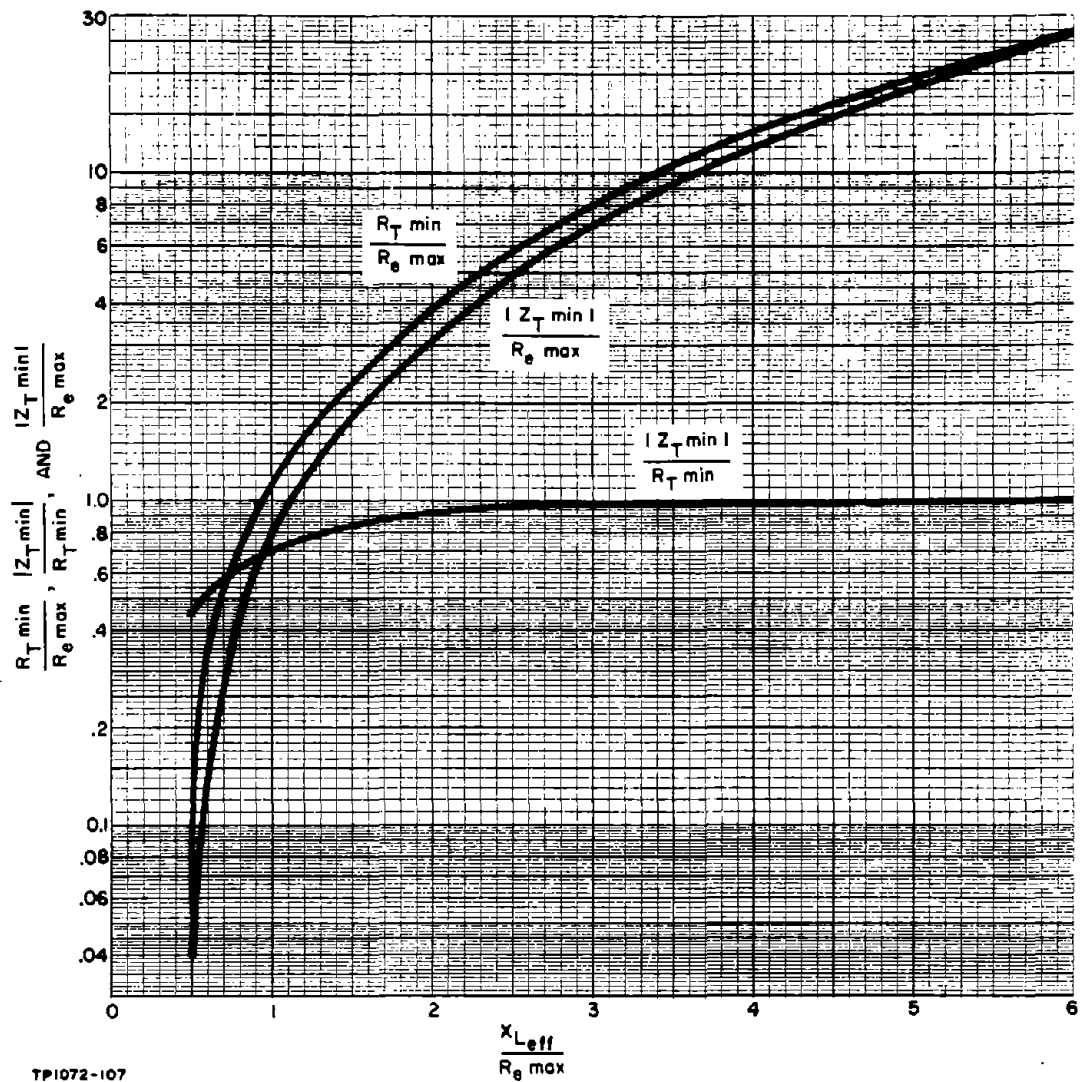
where g_T and b_T are the total load conductance and susceptance, respectively, and R_{Tmin} and X_T are the corresponding parallel impedance components.

Therefore:

$$\frac{R_{Tmin}}{X_T} = \frac{R_{emax}}{X_{Leff}} \quad (8-29)$$

The total load impedance Z_T is the parallel combination of R_T and X_T . That is:

$$Z_{Tmin} = \frac{R_{Tmin}}{1 + j \frac{R_{Tmin}}{X_T}} \quad (8-30)$$



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Figure 8-10. $\frac{|Z_{Tmin}|}{R_{Tmin}}$ and $\frac{R_{Tmin}}{R_{\theta max}}$ as Functions of $\frac{X_{Leff}}{R_{\theta max}}$

Substituting from Equation (8-29) for $\frac{R_{Tmin}}{X_T}$ gives:

$$Z_{Tmin} = \frac{R_{Tmin}}{1 + j \frac{R_{\theta max}}{X_{Leff}}} \quad (8-31)$$

and the magnitude of Z_{Tmin} is then:

$$|Z_{Tmin}| = \frac{R_{Tmin}}{\sqrt{1 + \left(\frac{R_{\theta max}}{X_{Leff}}\right)^2}} \quad (8-32)$$

Figure 8-10 gives a plot of the ratio of $\left| \frac{Z_{Tmin}}{R_{Tmin}} \right|$ as a function of $\frac{X_{Leff}}{R_{emax}}$ which shows that $\left| Z_{Tmin} \right|$ falls substantially below R_{Tmin} for $\frac{X_{Leff}}{R_{emax}}$ ratios of 2 or less.

In setting up the transistor biasing conditions, the requirement to be fulfilled to ensure voltage limiting under the worst conditions is:

$$I_C \cdot \left| Z_{Tmin} \right| \geq V_{CE} \quad (8-33)$$

where V_{CE} is the transistor collector emitter DC voltage and I_C is the DC collector current. Equation (8-33) is based on the assumption that the negative peak collector voltage swing drives the transistor into the saturation knee. This condition does occur and is the means normally employed of providing hard limiting.

Since the value of $\left| Z_{Tmin} \right|$ determines the required transistor bias conditions and is therefore a design factor, it is convenient to relate it to R_{emax} . Multiplying the values of $\left| \frac{Z_{Tmin}}{R_{Tmin}} \right|$ in the plot of Figure 8-10 by the corresponding values of $\frac{R_{Tmin}}{R_{emax}}$ results in the curve of $\left| \frac{Z_{Tmin}}{R_{emax}} \right|$ shown in Figure 8-10.

8-14. Basic Pierce Oscillator Power Output Limitations

In Paragraph 1-16 an equation is developed for the ratio of the oscillator output power relative to the crystal unit rated dissipation as a function of the π network constants for the given crystal unit loading conditions. Figure 1-18 presents a plot of this equation as a function of $\frac{X_{Leff}}{R_{emax}}$ which shows that the

oscillator power output can only exceed the crystal unit dissipation rating when $\frac{X_{Leff}}{R_{emax}}$ is less than 1. However, it has been shown in Paragraph 8-13 that the

amplifier load has a substantial parallel reactive component when the ratio $\frac{X_{Leff}}{R_{emax}}$ approaches and decreases below 1. Consequently, in the region where high power output is obtainable from this circuit, the transistor DC collector current requirement is increased in order to provide the necessary signal current for the reactive part of the load.

To illustrate this, consider an 800-KC design using a CR-18A/U crystal unit, the characteristics of which are $R_{\text{emax}} = 625$ ohms, $P_{\text{CMAX}} = 10$ MW. Figure 1-18 shows that for $\frac{X_{\text{Leff}}}{R_{\text{emax}}} = 0.5$, a load-to-crystal unit power dissipation ratio of 11.4 to 1 can be attained; that is, an oscillator power output of 114 MW. The corresponding π network ratios obtained from Figure 8-8 are $\frac{X_{\text{CT}}}{R_{\text{L}}} = 0.45$ and $\frac{R_{\text{L}}}{R_{\text{emax}}} = 0.1$. The collector signal voltage is obtained by substituting into Equation (1-113) as 2.8 VRMS. The amplifier load impedance magnitude is obtained from Figure 8-10 as $0.042 R_{\text{emax}}$; that is, 26 ohms. The required collector signal current is then 108 MA RMS, and the required DC collector current is 150 MA. The collector DC voltage required, using choke feed, will be approximately 5 VDC, resulting in a transistor collector dissipation of approximately 750 MW.

When biasing and transistor temperature stabilizing is accounted for, the total oscillator circuit dissipation will then be close to 1 W, resulting in an oscillator power efficiency of approximately 10 percent. Much higher efficiencies under comparable operating conditions can be obtained using the isolating resistor Pierce oscillator to be discussed later, and consequently the operation of the basic Pierce circuit in this manner is not recommended.

The inefficiency results because of the exorbitant capacitive current required by the π network, and a marked improvement occurs only when $\frac{X_{\text{Leff}}}{R_{\text{emax}}}$ is in the vicinity of 1. Figure 8-11 shows that the ratio of P_{L} to P_{CMAX} is then less than 1, and consequently the basic Pierce oscillator can only be employed efficiently under low output power conditions. This example shows the effect under the most favorable circumstances. At higher frequencies R_{emax} is considerably smaller, requiring higher current, lower voltage conditions for high power output.

At the higher frequencies of the range, the minimum usable value of $\frac{X_{\text{Leff}}}{R_{\text{emax}}}$ is further limited by amplifier output voltage limiting considerations. Equation (1-113) relates the permissible output voltage to P_{CMAX} , R_{emax} , and X_{Leff} . At a frequency of 20 MC the equivalent resistance and dissipation rating of a CR-18A/U crystal unit are 20 ohms and 5 MW, respectively. Substituting into Equation (1-113) gives:

$$V_{\text{Omax}} = 0.45 \text{ VRMS (0.64 V peak) for } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 1$$

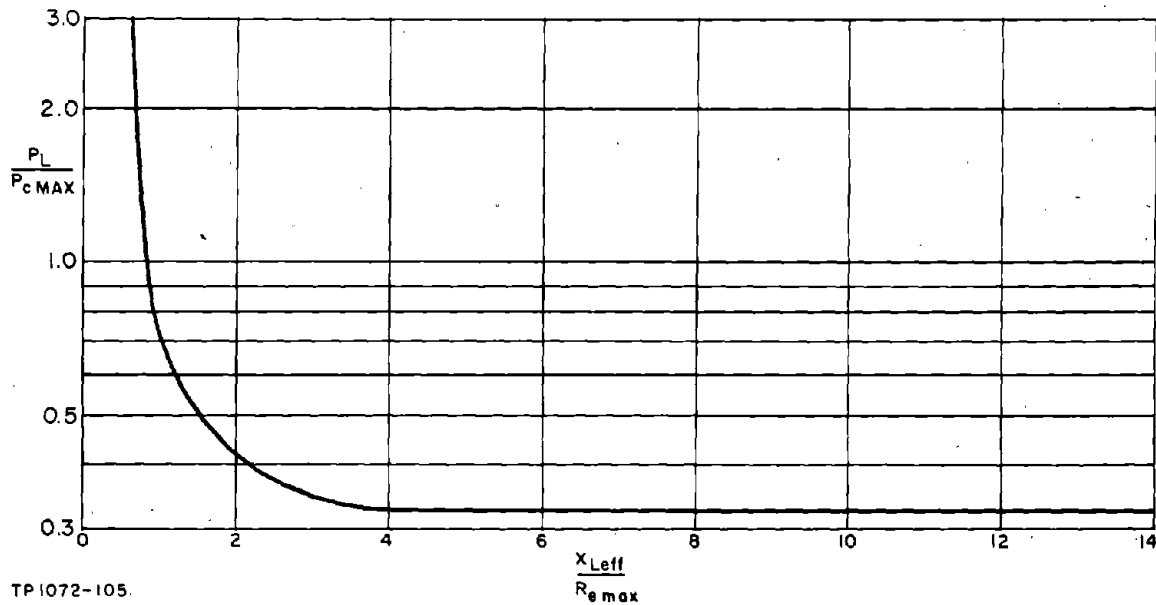


Figure 8-11. Ratio of Oscillator Output Power Relative to Crystal Dissipation Rating as a Function of X_{Leff}/R_{emax}

$$V_{Omax} = 1 \text{ VRMS (1.4 V peak) for } \frac{X_{Leff}}{R_{emax}} = 3$$

$$V_{Omax} = 1.9 \text{ VRMS (2.7 V peak) for } \frac{X_{Leff}}{R_{emax}} = 6$$

To provide a limiting action, the transistor DC collector emitter voltage V_{CE} should be approximately equal to the peak collector voltage swing.

Therefore, the use of low $\frac{X_{Leff}}{R_{emax}}$ ratios requires V_{CE} values in the 0.6 to 1.5 V range. The performance of high frequency transistors is degraded at low collector emitter voltage levels, C_{cb}' increases and f_T decreases, making this type of operation undesirable. This tends to limit the usable $\frac{X_{Leff}}{R_{emax}}$ ratios to values greater than 3, corresponding to power outputs of approximately $1/3 P_{Cmax}$.

8-15. DESIGN PROCEDURE FOR BASIC PIERCE OSCILLATOR

The preceding discussion gives all the information required to assemble a design procedure for this type of oscillator. The choice of circuit values in any particular application depends on such things as the available DC voltage and

current, and the transistor type. In order to optimize the design it is therefore necessary in the preliminary stages of the design process to make several sets of calculations to determine the most suitable $\frac{X_{Leff}}{R_{max}}$ ratio for the particular application. Once this selection is made, a series of calculations then leads to a final design.

One of the basic assumptions used in the design procedure is that emitter degeneration will be employed because of the advantages previously noted. The minimum value of the unbypassed emitter resistor should not be less than 20 or 30 ohms for best results.

Step 1

Determine the crystal unit power rating, maximum equivalent resistance, and X_e (the crystal loading capacitor reactance $X_{C_L'}$) from the crystal unit data sheet. Using the three succeeding design examples as a guide to the range of values of $\frac{X_{Leff}}{R_{max}}$ likely to be most applicable at various frequencies in the range, tabulate the following π network and amplifier characteristics for various values of $\frac{X_{Leff}}{R_{max}}$:

- (a) $\frac{R_L}{R_{max}}$; obtained from the plot of $\frac{R}{R_{max}}$ in Figure 8-8.
- (b) R_L ; obtained from $\frac{R_L}{R_{max}}$ by substituting for R_{max} .
- (c) K_A ; obtained from Figure 8-8.
- (d) R_{Tmin} ; obtained from Figure 8-10 and the known value of R_{max} .
- (e) $|Z_{Tmin}|$; obtained from Figure 8-10 and the known value of R_{max} .
- (f) V_{omax} RMS; obtained by applying Equation (1-113).
- (g) V_{omax} (Peak); V_{omax} RMS multiplied by 1.41. This represents the maximum collector-emitter voltage V_{CE} that can be used.
- (h) I_C ; V_{omax} (peak) divided by $|Z_{Tmin}|$.

Step 2

Decide the transistor type to be used. Any transistor with an f_T greater than 10 times the design frequency and a power rating at the maximum operating temperature of, say, 50 MW can be used. In the three succeeding design examples, the 2N706A has been used on the grounds that it is one of the least costly transistors available at this time.

From the manufacturer's data sheet, determine and tabulate the following transistor characteristics at the collector current and V_{CE} values arrived at in Step 1.

(a) h_{FEmin}

Most manufacturers give a guaranteed minimum common emitter current gain at 25°C at a particular collector current and voltage. In addition, the data sheet usually contains curves of the variation of typical h_{FE} with collector current and temperature. It is usually necessary to estimate h_{FEmin} from the 25°C curve, taking into consideration the relative values of the quoted minimum and typical values.

(b) f_T (typical)

Most data sheets give curves of constant f_T with V_{CE} and I_C variation. In some cases these do not cover operation at sufficiently low V_{CE} and I_C values, and extrapolation may again be necessary.

(c) BV_{CEO}

Any values of V_{omax} (peak) obtained in Step 1 which are larger than $0.5 BV_{CEO}$ cannot be used because of the possibility of voltage breakdown on the positive peak of the collector voltage swing.

(d) C_{cb}'

The data sheet usually contains a plot of C_{ob} versus collector-base voltage. The direct capacitance C_{cb} between collector and base forms a part of C_{ob} , and C_{cb}' is approximately 1 PF less than C_{ob} .

(e) r_{bb}'

In the absence of specific information, assume a value of 60 ohms.

Step 3 Calculate and tabulate:

The amplifier voltage gain is:

$$G_V = - \frac{\alpha_o \cdot R_L}{r_e + r_E + r_{bb}'(1 - \alpha_o)} \quad (8-34)$$

$$R_{b'E}' = (1 + h_{FEmin})(r_e + r_E) \quad (8-35)$$

where:

$$r_e = \frac{25}{I_e \text{ (MA)}} + r' \quad (8-36)$$

In the absence of more specific information, assume r' to be 1 ohm.

The amplifier parallel input resistance is:

$$R_{in(p)} = (r_{bb}' + R_b' E) \quad (8-37)$$

For

$$\frac{R_{in(p)}}{R_{max}} \leq 3.6, \text{ calculate:}$$

$$X_{CS} = \frac{R_{in(p)}}{6} \quad (8-38)$$

For

$$\frac{R_{in(p)}}{R_{max}} > 3.6, \text{ calculate:}$$

$$X_{CS} = \sqrt{0.1 R_{max} \cdot R_{in(p)}} \quad (8-39)$$

The crystal π network attenuation is:

$$A_V = \frac{X_{CS}}{K_A \cdot X_{Leff}} \quad (8-40)$$

where

$$K_A = 1 + \frac{R_L}{X_{CT}} \cdot \frac{R_{max}}{X_{Leff}} \quad (8-41)$$

For the given crystal loading conditions, K_A is plotted in Figure 8-8 as a function of $\frac{X_{Leff}}{R_{max}}$.

Calculate the loop voltage gain:

$$G_V \cdot A_V$$

Step 4

On the basis of the tabulated data, select a suitable $\frac{X_{Leff}}{R_{emax}}$ ratio for the design. Selection should be based on the following considerations:

- (a) The loop voltage gain calculated in Step 3 must be at least 1.3 and preferably greater, particularly at frequencies above 5 or 10 MC where the transistor amplifier voltage gain may begin to fall, causing a reduction in the loop voltage gain below that estimated. The experimentally derived curves of Figures 3-6, 3-7, and 3-8 indicate the extent of this effect, for several types of transistors. An excessive loop voltage can be ignored at this point, since corrective measures can be employed later.
- (b) The collector signal voltage will be limited by the available supply voltage V_{CC} , the transistor BV_{CEO} , or by V_{omax} , the permissible π network input voltage. At low frequencies, either or both V_{CC} and BV_{CEO} will usually determine the maximum collector signal voltage. At high frequencies, V_{omax} will probably be the limiting factor. In the first case it should be noted that, if the maximum oscillator output power is desired, the selected $\frac{X_{Leff}}{R_{emax}}$ ratio should be such as to give a V_{omax} only slightly greater than the allowable collector signal voltage determined by supply voltage or BV_{CEO} considerations. Otherwise the oscillator power output will be less than that available from this circuit. This is because the crystal unit power dissipation will be less than P_{CMAX} , and, since π network loading considerations dictate the ratio of the output power to the crystal dissipation, the output power will be correspondingly reduced.
- (c) The total current drain of the circuit decreases with increasing $\frac{X_{Leff}}{R_{emax}}$ ratio. In many applications it may be desirable to minimize the oscillator supply power by operating with as high a ratio of $\frac{X_{Leff}}{R_{emax}}$ as possible compatible with (a) and (b), and the loading effect of R_r , the resistance effectively placed across the π network mid-section by the transistor internal feedback, which tends to increase with $\frac{X_{Leff}}{R_{emax}}$.

Step 5

Calculate and tabulate:

$$C_{b'E} = \frac{1}{\omega_T (r_e + r_E)} \quad (8-42)$$

$$X_{Cb'E} = \frac{1}{\omega C_{b'E}} \quad (\text{or } \frac{C_L}{C_{b'E}} \cdot X_e) \quad (8-43)$$

$$r = \frac{R_{b'E} \cdot r_{bb'}}{R_{b'E} + r_{bb'}} \quad (8-44)$$

$$\frac{r}{X_{Cb'E}}$$

$$R_{in(p)} = (r_{bb'} + R_{b'E}) \left[\frac{1 + \left(\frac{r}{X_{Cb'E}} \right)^2}{1 + \frac{R_{b'E} \cdot r}{(X_{Cb'E})^2}} \right] \quad (8-45)$$

$$X_{Ccb'} = \frac{1}{\omega (C_{ob} - 1)} \quad (\text{or } \frac{C_L}{(C_{ob} - 1)} \cdot X_e) \quad (8-46)$$

$$X_{C(p)} = \frac{1}{\omega (C_{b'E} + C_{cb'})} \quad (\text{or } \frac{C_L}{(C_{b'E} + C_{cb'})} \cdot X_e) \quad (8-47)$$

$$\frac{r}{X_{C(p)}}$$

$$C_r = \frac{r}{r_{bb'}} \cdot \left[1 + \left(\frac{r}{X_{C(p)}} \right)^2 \right] \quad (8-48)$$

$$X_{C_r} = \frac{1}{\omega (C_r + 1)} \quad (\text{or } \frac{C_L}{(C_r + 1)} \cdot X_e) \quad (8-49)$$

R_D (h_{FE} times the slope of the collector characteristics at the given working point)

$$R_r = R_D \cdot \frac{r_{bb'}}{r} \left[1 + \left(\frac{r}{X_{Cb'E}} \right)^2 \right] \text{ in parallel with}$$

$$r_{bb'} \left[1 + \frac{C_{b'E}}{C_{cb'}} + \frac{X_{Ccb'} \cdot X_{C(p)}}{r^2} \right] \quad (8-50)$$

$$R_{o(p)} = \frac{R_D \cdot (r_E + r_e)}{\alpha_o r} \left[1 + \left(\frac{r}{X_{C_{b'E}}} \right)^2 \right] \text{ in parallel with}$$

$$\frac{(r_e + r_E)}{\alpha_o} \left[1 + \frac{C_{b'E}}{C_{cb'}} + \frac{X_{Ccb'} \cdot X_{C(p)}}{r^2} \right] \quad (8-51)$$

$$C_{o(p)} = \frac{\alpha_o \cdot r}{r_e + r_E} \cdot \frac{C_{cb'}}{\left[1 + \left(\frac{r}{X_{C(p)}} \right)^2 \right]} \quad (8-52)$$

Compare $R_{o(p)}$ with R_L . If $R_{o(p)}$ is less than, say, $5 R_L$, R_L should be increased to maintain the network loading conditions in accord with the design. The new value of R_L is given by:

$$R_L \text{ (new)} = \frac{R_{o(p)} \cdot R_L \text{ (old)}}{R_{o(p)} - R_L \text{ (old)}} \quad (8-53)$$

Calculate the transistor base bias resistor values using either the method given in Paragraph 3-26 or any other preferred method. From the values of the biasing resistors obtained, calculate:

$$R_{b(p)} = \frac{R_{b1} \cdot R_{b2}}{R_{b1} + R_{b2}} \quad (8-54)$$

Calculate the combined input resistance of $R_{in(p)}$ and $R_{b(p)}$ in parallel from Equation (8-55):

$$R''_{in(p)} = \frac{R_{b(p)} \cdot R_{in(p)}}{R_{b(p)} + R_{in(p)}} \quad (8-55)$$

If the decrease in amplifier input resistance is significant (say more than 10 percent), a loop gain adjustment should be made. If the π network output is phase angle limited, the loop gain is reduced in the ratio of $R''_{in(p)}$ to $R_{in(p)}$. If the π network is operating under output loading limited conditions, the loop gain is reduced as the square root of the ratio of $R''_{in(p)}$ to $R_{in(p)}$.

Before determining the effect of C_r and R_r on the π network, it is first necessary to finalize the loop gain. Loop voltage gains greater than 2 for the worst-case design are undesirable because of the possibility of squegging occurring when the loop gain increases, as will happen when a good crystal unit is in circuit. Often, the available loop gain will be larger than 2 after the foregoing corrections have been made. The loop voltage gain is proportional to X_{CS} , and a convenient method of reducing the loop voltage gain is to decrease X_{CS} below the value stipulated by amplifier input resistance considerations. To reduce the loop voltage gain, calculate:

$$X'_{CS} = X_{CS} \cdot \frac{G_{VL} \text{ (desired)}}{G_{VL} \text{ (calculated)}} \quad (8-56)$$

To determine the effect of C_r and R_r on the feedback network, calculate:

$$X_e - X_{C\ell} = X_{Leff} + X'_{CS} \quad (8-57)$$

where X'_{CS} is the value finally selected.

$$R'_{emax} = \left[\frac{1 + \frac{X_e - X_{C\ell}}{R_r \cdot R_{emax}}}{1 - \left(\frac{X_e - X_{C\ell}}{X_{Cr}} \right)^2} \right] \cdot R_{emax} \quad (8-58)$$

$$X' = \frac{X_e - X_{C\ell}}{1 - \frac{X_e - X_{C\ell}}{X_{Cr}}} \quad (8-59)$$

$$\frac{X' - X'_{CS}}{X' - X_{CS}} \cdot \frac{1}{R'_{emax}}$$

The π network attenuation is now:

$$A'_V = - \frac{X'_{CS}}{X' - X'_{CS}} \cdot \frac{1}{1 + \frac{R_L}{X_{CT}} \cdot \frac{R'_{emax}}{X' - X'_{CS}}} \quad (8-60)$$

where $\frac{R_L}{X_{CT}}$ is given in Figure 8-8 for the stipulated value of $\frac{X_{Leff}}{R_{emax}}$.

Compare A'_V with $A_V \cdot \frac{X_{C'S}}{X_{CS}}$. If the difference between A'_V and $A_V \cdot \frac{X_{C'S}}{X_{CS}}$ is less than 10 percent, the effect on the loop voltage gain will be small and can be neglected. If not, the value of $(X_{C'S})$ should be adjusted and R'_{emax} , X' , and A'_V recalculated until this order of agreement is obtained. It is desirable that the value of X_{CS} finally arrived at should not exceed that calculated in Step 3 on the basis of crystal loading considerations.

Step 6

Calculation of remaining component values.

(a) π Network Components

$$C_S = \frac{X_e}{X_{CS}} \cdot C_L \quad (8-61)$$

The amplifier input capacitance is approximately:

$$C_{in(p)} = C_{b'E} \left(\frac{R_{b'E}}{R_{b'E} + r_{bb'}} \right)^2 \left[\frac{1}{1 + \left(\frac{r}{X_{Cb'E}} \right)^2} \right] \quad (8-62)$$

$$C_S (\text{physical}) = C_S - C_{in(p)} \quad (8-63)$$

$$X_{C_L} = X_e - X_{Leff} - X_{CS} \quad (8-64)$$

$$C_L = \frac{X_e}{X_{C_L}} \cdot C_L \quad (8-65)$$

X_{CT} is obtained from the curve of $\frac{X_{CT}}{R}$ plotted in Figure 8-8 at the appropriate $\frac{X_{Leff}}{R_{emax}}$ for the known value of R , (R_L or R_L and $R_{o(p)}$ in parallel).

$$C_T = \frac{X_e}{X_{CT}} \cdot C_L \quad (8-66)$$

C_T is the net π network input capacitance, and allowance must be made for the amplifier output capacitance $C_{O(p)}$ and for tuning out the parallel feed inductor. A suitable value of inductance is chosen for the collector circuit.

Calculate its reactance X_A . Determine the capacitance C_A that will resonate with L at the design frequency.

$$C_A = \frac{X_e}{X_A} \cdot C_L \quad (8-67)$$

$$\text{Then } C_T (\text{physical}) = C_T + C_A - C_{O(p)} \quad (8-68)$$

(b) Emitter Circuit Components

The total resistance required in the emitter circuit is given by:

$$R_E + r_E \approx \frac{V_{BG} - 0.7}{I_E} \quad (8-69)$$

If r_E is significant, subtract to find R_E . The emitter decoupling capacitor value is determined as follows: The amplifier input impedance as seen at the emitter decoupling point will have a minimum value of $r_e + r_E$. To ensure adequate decoupling and to minimize possible phase errors, it is desirable that the reactance X_{C_E} of the emitter decoupling capacitor should not be greater than one-tenth the value of the parallel combination of $r_e + r_E$ and R_E ; that is:

$$X_{C_E} \leq \frac{(r_e + r_E) R_E}{10[r_e + r_E + R_E]} \quad (8-70)$$

and

$$C_E = \frac{X_e}{X_{C_E}} \times C_L \quad (8-71)$$

8-16. DESIGN EXAMPLES

The following design calculations illustrate the application of the design procedure. Evaluation data for these designs are presented at the end of each example. In these evaluations the effects of changing crystal units and transistors on the collector signal voltage and oscillator frequency were determined. One crystal unit was made representative of a "worst case" unit by including sufficient resistance in series with it to make its equivalent resistance equal to R_{emax} . All test data, with the exception of those for crystal unit interchange, was obtained using this "worst case" crystal unit.

Temperature tests were made in two ways. Firstly, the entire oscillator was subjected to the range of temperature. Secondly, the crystal unit was enclosed within a crystal unit oven maintained at 105°C , and the remainder of the oscillator circuit was subjected to the range of temperature. The oscillator frequency variations obtained in the latter test are primarily due to phase angle changes in the circuit other than the crystal, and the results indicate how much wider the oscillator frequency tolerance will be compared to the crystal unit frequency tolerance. The former test results mainly indicate the temperature characteristic of the particular crystal unit used in the tests and the temperature stability of the oscillator output voltage.

Judging by the results obtained, oscillator frequency stabilities of 10 to 15 PPM wider than that of the crystal alone will be obtained in situations where a large number of similar oscillators are involved under conditions where transistor and crystal unit changes will be made without oscillator frequency resetting. This will decrease to approximately ± 3 PPM when frequency resetting is allowed.

8-17. 800 KC, 2N706A Basic Pierce Oscillator

Crystal Characteristics: CR-18A/U.

$$X_e = 6250 \text{ ohms}$$

$$R_{\text{emax}} = 625 \text{ ohms}$$

$$P_{\text{CMAX}} = 10 \text{ MW}$$

Network Characteristics:

$\frac{X_{\text{Leff}}}{R_{\text{emax}}}$	X_{Leff} (ohms)	$\frac{R_L}{R_{\text{emax}}}$	R_L (K)	K_A	R_{Tmin} (ohms)	$ Z_T $ (K)	V_{omax} (RMS)	V_{omax} peak
1	625	2.7	1.7	4.7	750	0.53	3.5	5
1.5	937	6.5	4.1	4.4	1300	1.1	4.5	6.3
2	1250	12.3	7.7	4.3	2100	1.9	5.6	7.9

Transistor Characteristics:

$\frac{X_{\text{Leff}}}{R_{\text{emax}}}$	I_C (MA)	V_{CE}	h_{FEmin}	f_T (MC)	BV_{CEO}	$C_{\text{cb'}}$ (PF)	r_e (ohms)	$r_{\text{bb'}}$
1	10	4.5	20	300	15	4	2.5	60
1.5	6	6	15	300	15	4	4.3	60
2	4	7.5	14	250	15	3	6.2	60

Loop Gain ($r_E = 30 \text{ ohms}$):

$\frac{X_{\text{Leff}}}{R_{\text{emax}}}$	G_V	$R_{\text{b'E}}$ (ohms)	Approx. $R_{\text{in(p)}}$ (ohms)	$\frac{R_{\text{in(p)}}}{R_{\text{emax}}}$	X_{CS} (ohms)	A_V	G_{VL}
1	45.5	680	740	1.2	123	0.042	1.9
1.5	100	550	610	0.98	102	0.025	2.5
2	178	540	600	0.96	100	0.019	3.4

The working point is selected at $\frac{X_{Leff}}{R_{emax}} = 2$, $V_{CE} = 7 \text{ V}$, $I_E = 4 \text{ MA}$

$C_{b'E}$ (PF)	$X_{Cb'E}$ (K)	r (ohms)	$\frac{r}{X_{Cb'E}}$	$\frac{R_{b'E} \cdot r}{(X_{Cb'E})^2}$	$R_{in(p)}$	$X_{Ccb'}$ (K)	$X_{C(p)}$ (K)	$\frac{r}{X_{\alpha(p)}}$
12	17	54	0.003	≈ 0	600	67	13.5	0.004
C_r (PF)	X_{C_r} (K)	R_D (K)	R_r (K)	$R_{o(p)}$ (K)	$C_{o(p)}$ (PF)			
2.7	74	160	180	115	4			

Bias Network Values:

For a 15-V supply and $V_{CE} = 7 \text{ V}$, $V_{BG} \approx 8.7$, a ΔV_{BG} of 1 V requires:

$$R_{b1} = 7.5 \text{ K}$$

$$R_{b2} = 14 \text{ K}$$

$$R_{b(p)} = 4.9 \text{ K}$$

$$R''_{in(p)} = 530 \text{ ohms}$$

Loop gain reduction required, so no action taken.

Reducing loop voltage gain to 2:

$$X'_{C_S} = 59 \text{ ohms}$$

$$X_e - X_{C_L} = 1309 \text{ ohms}$$

$$R'_{emax} = 625 \text{ ohms}$$

$$X' = 1309 \text{ ohms}$$

C_r and R_r have negligible effect on the π network attenuation.

Calculation of Remaining Components:

$$C_S = 3400 \text{ PF}$$

$$C_{in(p)} = 10 \text{ PF}$$

$$C_S \text{ (physical)} = 3400 \text{ PF}$$

$$X_{C_L} = 4940 \text{ ohms}$$

$$C_L = 41 \text{ PF}$$

$$X_{C_T} = 1150 \text{ ohms}$$

$$C_T = 174 \text{ PF}$$

In this design a tunable inductor was used:

$$L = 500 \text{ UH}$$

$$X_A = 2.5 \text{ K}$$

$$C_A = 80 \text{ PF}$$

$$C_T \text{ (physical)} = 250 \text{ PF}$$

$$R_E = 2 \text{ K}$$

$$X_{C_E} = 3.6 \text{ ohms}$$

$$C_E = 0.05 \text{ UF}$$

DESIGN EVALUATION DATA
0.8 MC BASIC PIERCE OSCILLATOR (2N706A)
(All results obtained using limit crystal)

<u>Crystal Units</u> <u>(CR-18A/U)</u>	<u>Parallel Resonant</u> <u>Frequency (MC)</u>	<u>R_e</u> <u>(Ohms)</u>
1	0.799993	570
2	0.799998	590
3	0.800006	560
4	0.799999	630

DESIGN EVALUATION DATA
0.8 MC BASIC PIERCE OSCILLATOR (2N706A) (CONT)

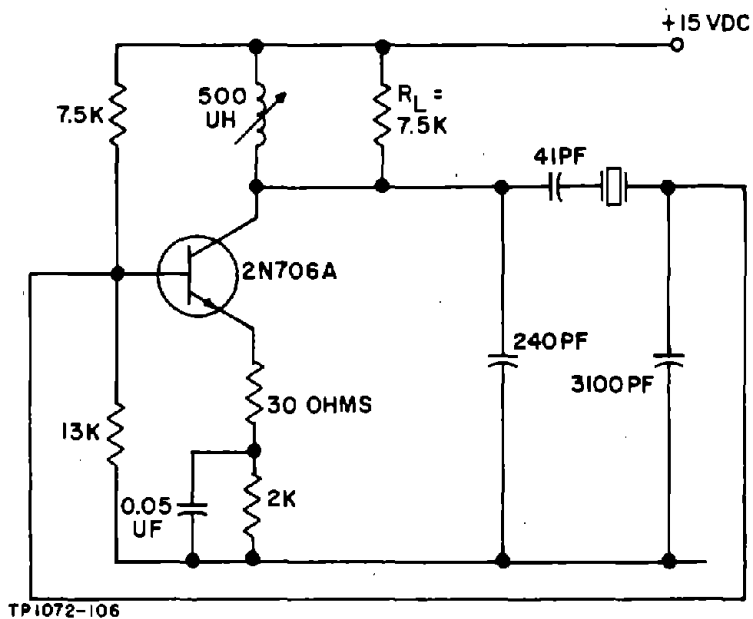


Figure 8-12. 0.8 MC Basic Pierce Oscillator Circuit (2N706A),
Schematic Diagram

Effects of		Change
+15% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = +17\%$
-20% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = -18\%$
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = \pm 3\%$
-55 C to +105 C Change in T_a on Oscillator	Frequency V_o	± 14 PPM $\Delta V_o = \pm 10\%$
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		< ± 2 PPM
Transistor Interchange (8 transistors)	Frequency V_o	< 1 PPM $\Delta V_o < \pm 1\%$
Crystal Unit Interchange (No Tuning)	Frequency Miscorrelation V_o	± 10 PPM $\Delta V_o = \pm 5\%$

8-18. 5 MC, 2N706A Basic Pierce Oscillator

Crystal Characteristics: CR-18A/U

$$X_e = 1000 \text{ ohms}$$

$$R_{e\max} = 60 \text{ ohms}$$

$$P_{C\max} = 10 \text{ MW}$$

π Network Characteristics:

$\frac{X_{Leff}}{R_{e\max}}$	$\frac{X_{Leff}}{R_{e\max}}$ (ohms)	$\frac{R_L}{R_{e\max}}$	$\frac{R_L}{R_{e\max}}$ (K)	K_A	$\frac{R_{Tmin}}{R_{e\max}}$ (ohms)	$\frac{ Z_T }{R_{e\max}}$ (K)	$\frac{V_{omax}}{R_{e\max}}$ (RMS)	$\frac{V_{omax}}{R_{e\max}}$ peak
3	180	28	1.7	4.2	440	0.42	2.45	3.5
5	300	79	4.7	4.1	1180	1.2	4	5.6

Transistor Characteristics:

$\frac{X_{Leff}}{R_{e\max}}$	I_C (MA)	V_{CE}	h_{FEmin}	f_T (MC)	BV_{CEO}	$C_{cb'}$	r_e (ohms)	$r_{bb'}$
3	9	3	20	300	15	5	2.8	60
5	5	5	15	300	15	4	5	60

Loop Gain ($r_E = 30 \text{ ohms}$):

$\frac{X_{Leff}}{R_{e\max}}$	G_V	$\frac{R_{b'E}}{R_{e\max}}$ (ohms)	Approx. $\frac{R_{in(p)}}{R_{e\max}}$	$\frac{R_{in(p)}}{R_{e\max}}$	$\frac{X_{CS}}{R_{e\max}}$ (ohms)	A_V	G_{VL}
3	45	690	750	12.5	67	0.089	4
5	112	560	620	10	61	0.05	5.6

The working point was selected at $\frac{X_{Leff}}{R_{e\max}} = 5$, $V_{CE} = 5 \text{ V}$, $I_C = 5 \text{ MA}$

$C_{b'E}$ (PF)	$X_{Cb'E}$ (K)	r (ohms)	$\frac{r}{X_{Cb'E}}$	$\frac{R_{b'E} \cdot r}{(X_{Cb'E})^2}$	$\frac{R_{in(p)}}{R_{e\max}}$ (ohms)	$\frac{X_{Ccb'}}{R_{e\max}}$ (K)	$\frac{X_{C(p)}}{R_{e\max}}$ (ohms)	$\frac{r}{X_{C(p)}}$	C_r (PF)	X_{Cr} (K)
15	2.1	54	0.026	0.007	620	8	1700	0.032	3.5	9.2

R_D (K)	R_r (K)	$R_{o(p)}$ (K)	$C_{o(p)}$ (PF)
240	140	85	6

Bias Network Values:

For a 15-V supply and $V_{CE} = 5$ V, $V_{BG} \approx 10.7$, a ΔV_{BG} of 1 V requires:

$$R_{b1} = 5.6 \text{ K}$$

$$R_{b2} = 22 \text{ K}$$

$$R_{b(p)} = 4.5 \text{ K}$$

$$R'_{in(p)} = 550 \text{ ohms}$$

Reducing the loop gain to 2 gives:

$$X'_{CS} = 22 \text{ ohms}$$

$$X_e - X_{C_L} = 320 \text{ ohms}$$

$$R'_{emax} = 60 \text{ ohms}$$

$$X' = 330 \text{ ohms}$$

C_r and R_T have negligible effect on the π network attenuation.

Calculation of Remaining Components

$$C_S = 1450 \text{ PF}$$

$$C_{in(p)} = 12 \text{ PF}$$

$$X_{C_L} = 680 \text{ ohms}$$

$$C_L = 47 \text{ PF}$$

$$X_{C_T} = 300 \text{ ohms}$$

$$C_T = 107 \text{ PF}$$

$$L = 10 \text{ UH}$$

$$X_A = 314 \text{ ohms}$$

$$C_A = 100 \text{ PF}$$

$$C_T (\text{physical}) = 200 \text{ PF}$$

$$R_E = 2 \text{ K}$$

$$X_{C_E} = 3.5 \text{ ohms}$$

$$C_E = 0.01 \text{ UH}$$

DESIGN EVALUATION DATA
5 MC BASIC PIERCE OSCILLATOR (2N706A)
(All results obtained using limit crystal)

<u>Crystal Units</u> (CR-18A/U)	<u>Parallel Resonant</u> <u>Frequency (MC)</u>	<u>R_e</u> (Ohms)
1	4.999956	16
2	4.999924	15
3	4.999973	24
4	4.999952	60

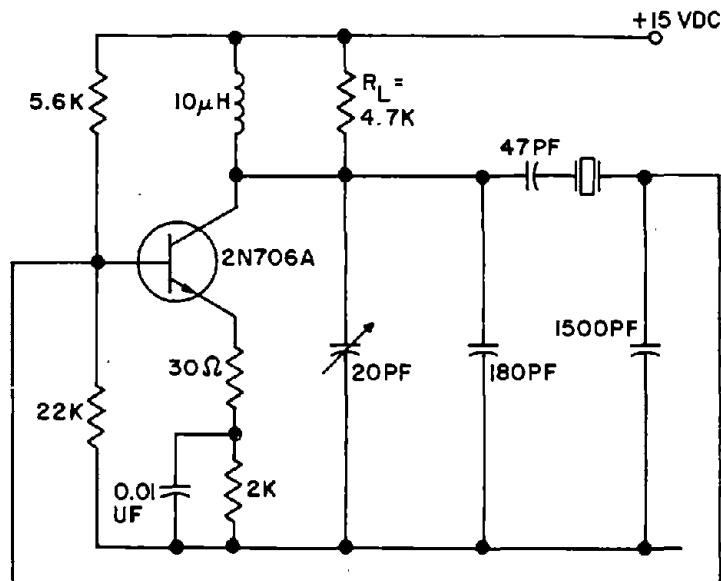


Figure 8-13. 5 MC Basic Pierce Oscillator Circuit (2N706A),
Schematic Diagram

DESIGN EVALUATION DATA
5-MC BASIC PIERCE OSCILLATOR CIRCUIT (2N706A) (CONT)

Effects of		Change
+15% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = +15\%$
-20% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = -20\%$
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o	< ± 1 PPM $\Delta V_o = \pm 6\%$
-55°C to +105°C Change in T_a on Oscillator	Frequency V_o	± 12 PPM $\Delta V_o = \pm 10\%$
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		< ± 2 PPM
Transistor Interchange (8 Transistors)	Frequency V_o	± 1 PPM $\Delta V_o = \pm 2\%$
Crystal Unit Interchange (No Tuning)	Frequency V_o	± 1 PPM $\Delta V_o = \pm 16\%$

8-19. 20 MC, 2N706A Basic Pierce Oscillator

Crystal Characteristics: CR-18A/U

$$X_e = 250 \text{ ohms}$$

$$R_{e\max} = 20 \text{ ohms}$$

$$P_{\text{CMAX}} = 5 \text{ MW}$$

Network Characteristics:

$\frac{X_{\text{Leff}}}{R_{\text{emax}}}$	X_{Leff} (ohms)	$\frac{R_L}{R_{\text{emax}}}$	R_L (ohms)	K_A	$R_{T\min}$ (ohms)	$ Z_T $ (ohms)	V_{omax} (RMS)	V_{omax} peak
3	60	28	560	4.2	148	140	1	1.4
6	120	110	2200	4.1	550	550	1.9	2.7

Transistor Characteristics:

$\frac{X_{\text{Leff}}}{R_{\text{emax}}}$	I_C (MA)	V_{CE}	$h_{FE\min}$	f_T (MC)	$C_{cb'}$ (PF)	r_e (ohms)	$r_{bb'}$ (ohms)
3	10	1.3	20	250	4	2.5	60
6	5	2.5	15	250	4	5	60

Loop Gain ($r_E = 30 \text{ ohms}$):

$\frac{X_{\text{Leff}}}{R_{\text{emax}}}$	G_V	$R_{b'E}$ (ohms)	Approx. $R_{\text{in}(p)}$ (ohms)	$\frac{R_{\text{in}(p)}}{R_{\text{emax}}}$	X_{C_S} (ohms)	A_V	G_{VL}
3	15	680	740	37	38	0.15	2.3
6	52	560	620	30	35	0.071	3.7

The working point is chosen at $\frac{X_{\text{Leff}}}{R_{\text{emax}}} = 6$.

$C_{b'E}$ (PF)	$X_{C_{b'E}}$ (ohms)	r (ohms)	$\frac{r}{X_{C_{b'E}}}$	$\frac{R_{b'E} \cdot r}{(X_{C_{b'E}})^2}$	$R_{\text{in}(p)}$ (ohms)	$X_{C_{cb'}}$ (K)	$X_{C(p)}$ (ohms)
18	445	55	0.12	0.15	535	2	360

$\frac{r}{X_{C(p)}}$	$\frac{C_r}{(PF)}$	$\frac{X_{Cr}}{(K)}$	$\frac{R_D}{(K)}$	$\frac{R_r}{(K)}$	$\frac{R_{o(p)}}{(K)}$	$\frac{C_{o(p)}}{(PF)}$
0.15	3.6	1.7	240	14	9.3	6

$R_{o(p)}$ is equal to $4.2 R_L$ and R_L should be increased accordingly. However, the oscillator power output capability is already low, and it was considered desirable to let R_L remain at 2.2 K and accept the increased crystal loading.

Calculation of Base Network Values:

Using a 10-V supply and $V_{CE} = 2.5$ V, $V_{BG} \approx 8$ V. Then a ΔV_{BG} of less than 0.2 V will occur for:

$$R_{b1} = 4.3 \text{ K}$$

$$R_{b2} = 51 \text{ K}$$

giving:

$$R_{b(p)} = 4 \text{ K}$$

$$R'_{in(p)} = 475 \text{ ohms}$$

This increased loading will automatically be remedied in reducing the excess loop gain.

Loop gain reduction to 1.6

$$X'_{CS} = 15 \text{ ohms}$$

Then:

$$X_e - X_{C\ell} = 135 \text{ ohms}$$

$$R'_{emax} = 20 \text{ ohms}$$

$$X' = 147 \text{ ohms}$$

$$X' - X'_{CS} = 132 \text{ ohms}$$

$$A'_V = 0.03$$

$$A_V \cdot \frac{X'_{CS}}{X_{CS}} = 0.031$$

Difference is less than 10 percent.

Calculation of Remaining Component Values:

$$C_S = 530 \text{ PF}$$

$$C_{in(p)} = 15 \text{ PF}$$

$$C_S \text{ (physical)} \approx 520 \text{ PF}$$

$$X_{C_J} = 115 \text{ ohms}$$

$$C_J = 70 \text{ PF}$$

$$X_{C_T} = 117 \text{ ohms}$$

$$C_T = 68 \text{ PF}$$

$$L = 6 \text{ UH}$$

$$X_A = 750 \text{ ohms}$$

$$C_A = 11 \text{ PF}$$

$$C_T \text{ (physical)} \approx 70 \text{ PF}$$

$$R_E = 1.5 \text{ K}$$

$$X_{C_E} = 3.5 \text{ ohms}$$

$$C_E = 2200 \text{ PF}$$

DESIGN EVALUATION DATA
20 MC BASIC PIERCE OSCILLATOR (2N706A)
(All results obtained using limit crystal)

<u>Crystal Units</u> (CR-18A/U)	<u>Parallel Resonant</u> <u>Frequency (MC)</u>	<u>R_e</u> (Ohms)
1	20.000270	7
2	20.000600	8
3	20.000400	7
4	20.000200	8
5	20.000000	20

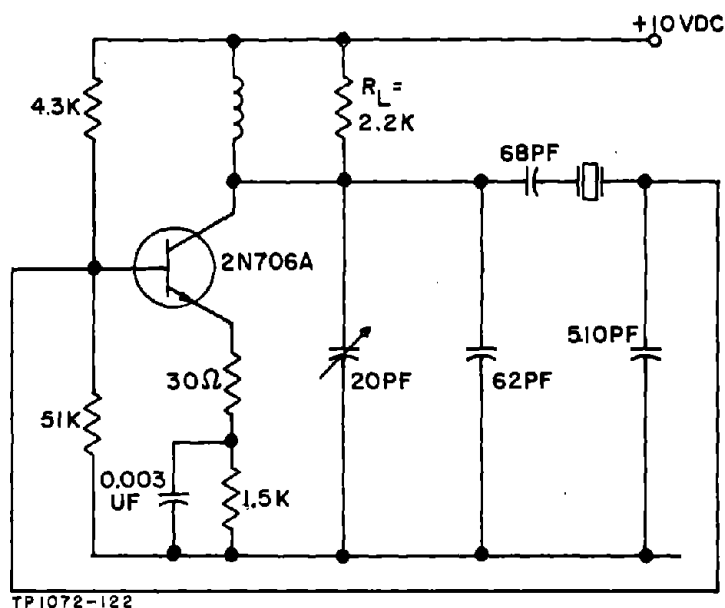


Figure 8-14, 20-MC Basic Pierce Oscillator Circuit (2N706A),
Schematic Diagram

DESIGN EVALUATION DATA
20 MC BASIC PIERCE OSCILLATOR (2N706A) (Cont)

Effects of		Change
+15% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = +15\%$
-20% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = -23\%$
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = \pm 3\%$
-55°C to +105°C Change in T_a on Oscillator	Frequency V_o	± 25 PPM $\Delta V_o = \pm 10\%$
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		< ± 2 PPM
Transistor Interchange (8 Transistors)	Frequency V_o	± 5 PPM $\Delta V_o = \pm 4\%$
Crystal Unit Interchange (No Tuning)	Frequency V_o	± 5 PPM $\pm 26\%$

8-20. Isolating Resistor Pierce Oscillator, 0.8 to 20 MC Range

Referring to Figure 1-17 (the circuit used to determine the loading effect of the π network driving source) if R is regarded as a resistor interposed between the output of an amplifier and the reactive part of the π network, the resulting circuit is shown in Figure 8-15. The consequence of viewing the circuit in this way are:

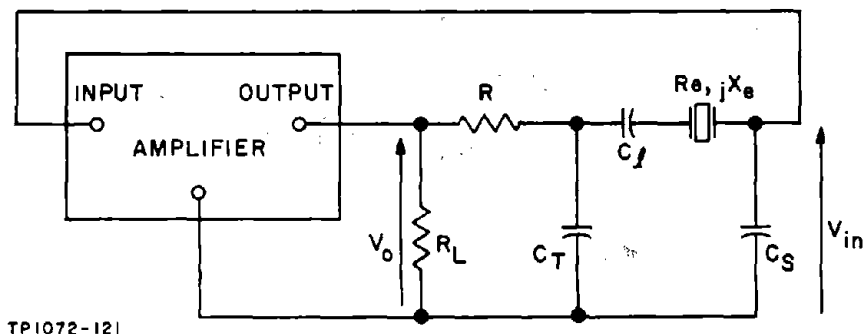


Figure 8-15. Pierce Oscillator Circuit Using an Isolating Resistor

(a) Provided R is much greater than R_L , the amplifier load impedance is practically independent of the π network input impedance and is essentially equal to R_L . Consequently, the amplifier input impedance is also virtually independent of the π network impedance. Therefore, the isolation between amplifier voltage gain and feedback functions is inherent in this circuit.

(b) The power division between the oscillator load R_L and the feedback network is roughly inversely proportional to the relative values of R and R_L . By making R much larger than R_L , the oscillator output power can be made many times greater than the feedback power and hence the crystal unit dissipation.

(c) The required amplifier voltage gain is increased in comparison with that required in the basic Pierce circuit since the voltage attenuation introduced by R must now be counteracted. For the crystal loading conditions previously established, this requires the amplifier voltage gain to be increased approximately 4 times for a given ratio of $\frac{X_{Leff}}{R_{emax}}$. The conditions placed on the amplifier are therefore more demanding in this respect than in the basic Pierce oscillator. In general, this means that it is no longer possible to use a large amount of emitter degeneration in the amplifier circuit. Consequently, the

amplifier characteristics are likely to be more frequency dependent at frequencies above a few megacycles.

8-21. Loop Voltage Gain

The formulae used in calculating the loop gain are as follows:
The maximum voltage attenuation ratio of the π network is given in Paragraph 1-10 as:

$$A_V = - \frac{X_{CS}}{X_{Leff}} \cdot \frac{1}{\left[1 + \frac{R}{X_{CT}} \cdot \frac{R_{emax}}{X_{Leff}} \right]}$$

$$= - \frac{X_{CS}}{K_A \cdot X_{Leff}} \quad (8-72)$$

where the value of X_{CS} for the given π network loading and phase angle limiting conditions is:

$$X_{CS} \leq \begin{cases} 1/6 R_{in(p)} \text{ for } R_{in(p)} \leq 3.6 R_{e \max} \\ \text{or} \\ \sqrt{0.1 R_{e \max} \cdot R_{in(p)}} \text{ for } R_{in(p)} > 3.6 R_{e \max} \end{cases} \quad (8-73)$$

The approximate value of the amplifier input resistance is given in Paragraph 3-20 as:

$$R_{in(p)} \approx (r_{bb'} + R_{b'e}) \left[\frac{1 + \left(\frac{r}{r_e} \cdot \frac{f}{f_T} \right)^2}{1 + h_{FEmin} \cdot \frac{r}{r_E} \left(\frac{f}{f_T} \right)^2} \right] \quad (8-74)$$

$$R_{b'e} = (1 + h_{FEmin}) r_e \quad (8-75)$$

The amplifier gain at frequencies up to the cutoff frequency f_V is:

$$G_V = \frac{\alpha_o \cdot R_T}{r_e + r_{bb'}(1 - \alpha_o) + (r_{bb'} + r_e) \cdot \frac{R_T}{R_D}} \quad (8-76)$$

where R_T is the parallel combination of the π network input resistance and R_L . Assuming that the π network input resistance is equal to R :

$$R_T = \frac{R_L \cdot R}{R_L + R} \quad (8-77)$$

The loop voltage gain is then:

$$G_{V_L} = G_V \cdot A_V \quad (8-78)$$

At frequencies above f_V it is considered desirable to determine G_V experimentally, although preliminary estimates sufficient to establish the desired transistor bias conditions can be obtained from a knowledge of the low frequency voltage gain, and behavior of f_V , and the voltage gain frequency dependence shown in Figures 3-6 thru 3-8.

The maximum collector signal voltage allowed without exceeding the crystal dissipation rating is from Paragraph 1-16:

$$V_{o\max} = 3.8 \frac{X_{Leff}}{R_{e\max}} \sqrt{P_{C\max} \cdot R_{e\max}} \quad (8-79)$$

For the CR-18A/U crystal unit which has a 10 MW dissipation rating between 0.8 and 10 MC and a 5 MW rating between 10 and 20 MC, Equation (8-79) can be restated as:

(a) Below 10 MC

$$V_{o\max} = 0.37 \frac{X_{Leff}}{R_{e\max}} \cdot \sqrt{R_{e\max}} \quad (8-80)$$

(b) Above 10 MC

$$V_{o\max} = 0.26 \cdot \frac{X_{Leff}}{R_{e\max}} \cdot \sqrt{R_{e\max}} \quad (8-81)$$

At frequencies of 0.8, 5, and 20 MC, the values of $V_{o\max}$ obtained by substituting for $R_{e\max}$ in Equations (8-80) and (8-81) are:

$$0.8 \text{ MC}; \quad V_{o\max} \approx 9.2 \frac{X_{Leff}}{R_{e\max}} V_{RMS}$$

$$5 \text{ MC}; \quad V_{\text{omax}} \approx 2.9 \frac{X_{\text{Leff}}}{R_{\text{emax}}} V_{\text{RMS}}$$

$$20 \text{ MC}; \quad V_{\text{omax}} \approx 1.16 \frac{X_{\text{Leff}}}{R_{\text{emax}}} V_{\text{RMS}}$$

8-22. DESIGN PROCEDURE FOR PIERCE OSCILLATOR USING AN ISOLATING RESISTOR

Step 1, Crystal Characteristics

Determine the crystal unit power rating, its equivalent reactance and maximum equivalent resistance from MIL-C-3098, Supplement 1. The crystal unit equivalent inductive reactance X_e is equal to the reactance of the specified loading capacitor C_L which will be either 30 or 32 PF. Figure 8-3 gives this information. Determine the permissible π network input voltage per unit of $\frac{X_{\text{Leff}}}{R_{\text{emax}}}$, using Equation (8-79).

Step 2, Selection of Transistor Type

(a) The transistor power dissipation at the highest operating temperature should be at least 2 to 3 times the desired output power.

(b) If possible the gain-bandwidth product of the transistor should be greater than 40 times the design frequency. If this condition can be met the amplifier voltage gain and input resistance will be essentially frequency independent at the amplifier load levels likely to be used.

(c) When condition (b) can be met, a large $h_{\text{FE min}}$ is desirable. $R_{b'e}$ will then be increased together with $R_{\text{in(p)}}$. This will allow an increase in X_{CS} resulting in a decrease in feedback network attenuation. However, a large value of $h_{\text{FE min}}$ makes the amplifier input resistance frequency-dependent at a lower frequency (see Equation (8-74)). Therefore, at frequencies above say 4 or 5 MC, no advantage is conferred by using a transistor with a $h_{\text{FE min}}$ greater than 20.

(d) If high power output is desired at the low end of the frequency range, a transistor with a high collector-emitter breakdown voltage will be required. At these frequencies the oscillator power output capability is determined by the transistor breakdown voltage and dissipation ratings. At higher frequencies the permissible crystal π network input voltage is usually the factor that limits the collector signal voltage, and high values of collector-emitter breakdown voltage are not then required.

In general, the higher the oscillator power output, the more stringent will be the transistor amplifier requirements. The following design examples will serve as a guide to the design limitations imposed by transistor characteristics.

Step 3

The oscillator power output may be limited by:

- (a) Transistor power dissipation
- (b) Transistor collector-emitter breakdown voltage rating
- (c) The available supply voltage
- (d) The combination of crystal power dissipation and inadequate amplifier voltage gain - input resistance product

It is therefore necessary to determine if any of these factors will prevent the desired power output from being obtained with the selected transistor. The amplifier is first considered to find the DC operating conditions that can be employed. With this information it is then possible to estimate the available loop gain.

From the transistor data sheet determine the permissible transistor power dissipation $P_{D \max}$ at the highest oscillator operating temperature and the base open-circuit collector-emitter breakdown voltage rating BV_{CEO} . BV_{CEO} is selected rather than BV_{CER} as a design limit because the base biasing network will probably need to be as large as possible consistent with a reasonable transistor bias point stability. It is therefore likely, insofar as breakdown voltage rating is concerned, that the transistor will be operating under biasing conditions where the base open-circuit voltage rating is applicable. If, as the design progresses, this is not found to be the case, an appropriate correction can be made if necessary.

BV_{CEO} determines the maximum allowable peak-to-peak collector signal voltage swing, and since this changes with variations of the oscillator load, $B+$, oscillator loop gain, and ambient temperature, the collector peak-to-peak signal voltage selected for a "worst case" design must be somewhat smaller than BV_{CEO} to allow for increases due to these causes. If a 30 percent allowance is made, the permissible RMS collector signal voltage for a "worst case" design ($R_e = R_{e \max}$) is:

$$V_o = 0.7 \frac{BV_{CEO}}{2.8} \quad (8-82)$$

The loop voltage gain for the "worst case" design will subsequently be fixed at a value of from 1.3 to 2, and under these conditions the amplifier operation approaches Class AB, the collector signal swinging between collector saturation and $2 V_{CE}$ in a reasonably sinusoidal manner. Therefore, the DC collector-emitter voltage will be approximately:

$$V_{CE} = \frac{0.7 BV_{CEO}}{2} \quad (8-83)$$

It is advisable that the emitter should be biased at least 2 volts above ground, and preferably higher, to ensure a reasonable transistor bias point stability with temperature. If the available supply voltage exceeds the collector-emitter DC voltage calculated from Equation (8-83) by more than this amount, this value of V_{CE} is the maximum allowable. If this is not the case, the maximum collector-emitter voltage, allowing for adequate biasing stability, will be:

$$V_{CE} = V_{CC} - 3 \quad (8-84)$$

where V_{CC} is the available supply voltage. Lower values of V_{CE} than those calculated from Equation (8-83) or (8-84) can of course be used. However, this will reduce the oscillator power conversion efficiency, since, for a given power output, the collector current and hence the circuit dissipation will increase.

The amplifier is then designed in a similar manner to a Class A power amplifier. The maximum allowable collector current is obtained from the previously calculated maximum transistor dissipation rating at the highest operating ambient temperature as:

$$I_{C \max} = \frac{P_{D \max}}{V_{CE}} \quad (8-85)$$

A small safety factor is desirable to allow for power supply variations, and I_C should be, say, 10 percent below the value calculated.

The maximum amplifier output for a "worst case" design will approach 50 percent of the transistor dissipation; that is:

$$P_{T \max} \approx 0.5 P_{D \max} \quad (8-86)$$

If this is larger than required, the DC collector current can be reduced accordingly. $P_{T \max}$ should, however, be larger than the desired power output since it also includes the feedback power. A suitable estimate for the feedback power at the low end of the range is 10 to 20 percent, increasing to 20 to 40 percent at 20 MC.

The amplifier load is then given by:

$$R_T = \frac{V_{CE}}{I_C} \quad (8-87)$$

where V_{CE} and I_C are the values finally selected.

The maximum crystal unit dissipation occurs when a crystal unit with an equivalent resistance of less than $R_{e \max}$ is in circuit and, therefore, when the loop gain is greater than the "worst case" design value. Also, despite the limiting occurring in the circuit, the increase in loop gain usually results in an increase in the collector signal voltage relative to that obtained for a "worst case" design. In determining the value of $\frac{X_{Leff}}{R_{e \max}}$ required to prevent the crystal unit dissipation exceeding the rating, it is therefore necessary to apply a correction factor allowing for this increase in collector signal voltage above the values expected for a "worst case" design. In the case where the collector-emitter breakdown voltage rating is the limiting factor, this correction can be conveniently introduced by assuming that the peak-to-peak collector signal voltage swing will approach BV_{CEO} when maximum crystal unit dissipation occurs. The formula for calculating the minimum required $\frac{X_{Leff}}{R_{e \max}}$ ratio is then:

$$\text{Minimum } \frac{X_{Leff}}{R_{e \max}} = \frac{BV_{CEO}}{2.8 \cdot V_{o \max} \text{ per unit } \frac{X_{Leff}}{R_{e \max}}} \quad (8-88)$$

A similar allowance for a 40 percent increase in the collector signal voltage for other V_{CE} values is given by the formula:

$$\text{Minimum } \frac{X_{Leff}}{R_{e \max}} = \frac{V_{CE}}{V_{o \max} \text{ per unit } \frac{X_{Leff}}{R_{e \max}}} \quad (8-89)$$

This is the minimum value of $\frac{X_{Leff}}{R_{e \max}}$ that can be used without the possibility of crystal unit overdrive. Higher values may be used but only at the expense of increasing the π network attenuation and hence increasing the amplifier voltage gain required. This may, in turn, require an increase in R_T with a consequent reduction in oscillator power output. The value of $\frac{X_{Leff}}{R_{e \max}}$ obtained from Equation (8-88) or (8-89) is a suitable value to assume initially for the purpose of calculating the oscillator loop gain; this value may then be increased if the loop gain obtained for the desired bias conditions is excessive.

From Figure 8-8 calculate R from the curve of $\frac{R}{R_{e \max}}$ at the appropriate value of $\frac{X_{Leff}}{R_{e \max}}$. The oscillator external load to be reflected into the collector circuit R_L is then approximately given as:

$$R_L \approx \frac{R_T \cdot R}{R - R_T} \quad (8-90)$$

Calculate X_{Leff} from the known value of $R_{e \max}$.

The oscillator loop gain can now be estimated for the derived amplifier bias and π network conditions to determine the design feasibility under these conditions.

Step 4, Loop Gain Determination

For the V_{CE} and I_C values obtained, determine $h_{FE \min}$ from the transistor data sheet. Most manufacturers give a guaranteed minimum common emitter current gain at 25°C at a particular collector current and voltage. In addition, the data sheet normally contains curves showing the typical variation of typical h_{FE} with collector current and temperature. It will normally be necessary to estimate $h_{FE \min}$ from the 25°C data, taking into account the relative values of the quoted typical and minimum values.

Also determine from the transistor data sheet the typical value of f_T at the V_{CE} and I_C values under consideration.

Calculate:

$$r_e = \left(\frac{25}{I_e} + r' \right) \quad (8-91)$$

$$R_{b'e} = r_e (h_{FE} + 1) \quad (8-92)$$

where, in the absence of more specific information, r' can be considered as 1 ohm.

The voltage gain, assuming no frequency effects, will be:

$$G_{V_o} \approx \frac{\alpha_o \cdot R_T}{r_e + r_{bb'}(1 - \alpha_o) + (r_{bb'} + r_e) \frac{R_T}{R_D}} \quad (8-93)$$

where R_D can be determined approximately from the collector curves.

Calculate:

$$\begin{aligned} & \frac{r}{r_e} \\ & \left(\frac{f}{f_T} \right)^2 \\ & R_{in(p)} \approx (r_{bb'} + R_{b'e}) \left[\frac{1 + \left(\frac{r}{r_e} \cdot \frac{f}{f_T} \right)^2}{1 + h_{FEmin} \cdot \frac{r}{r_e} \cdot \left(\frac{f}{f_T} \right)^2} \right] \end{aligned} \quad (8-94)$$

and

$$\frac{R_{in(p)}}{R_{e\max}}$$

The next step in the design procedure depends on the relative values of f_V and the design frequency. If the value of $R_{in(p)}$ is reduced say more than 20 percent by the frequency dependent factor, the transistor is operating near to or above its transconductance cutoff frequency $f_V/2$. The amplifier voltage gain will then be below its low frequency value. A second check can be made by calculating the value of $\frac{R_T}{X_{Ccb}} (r_e + r_{bb'})$ and comparing with $r_e + r_{bb'} (1 - \alpha_0)$. If the former exceeds the latter in value, the amplifier is operating above f_V . The amplifier voltage gain operating condition can also be roughly estimated from the voltage gain plots given in Figures 3-6, 3-7, and 3-8 and the relative characteristics of the transistor being considered for the design. When obtaining this estimate it should be noted that for two amplifiers having the same low frequency gain but different emitter currents and loads, the one having the higher emitter current will usually have the lower f_V .

From the foregoing it should be possible to obtain an estimate of the amplifier voltage, and the loop gain is determined as follows:

Calculate:

$$X_{CS} = \begin{cases} \frac{R_{in(p)}}{6} & \text{for } R_{in(p)} \leq 3.6 R_{e\max} \\ \sqrt{0.1 R_{e\max} R_{in(p)}} & \text{for } R_{in(p)} > 3.6 R_{e\max} \end{cases} \quad (8-95)$$

$$A_V = \frac{X_{CS}}{K_A \cdot X_{Leff}} \quad (8-96)$$

where K_A is given in Figure 8-8.

The loop voltage gain is then:

$$G_{VL} = G_V \cdot A_V \quad (8-97)$$

If the loop voltage gain is less than, say, 1.5 at low frequencies or less than 2 at frequencies where the voltage gain is a rough estimate, the design is probably not feasible. In any case, it is desirable to build a breadboard circuit to determine the actual voltage gain for the calculated biasing and load conditions. Little additional work is entailed if the breadboard layout is adaptable as the oscillator prototype chassis. Several transistors should be tested to ensure a representative sample. At this point the procedure divides, depending on the loop gain obtained using the lowest measured voltage gain.

(a) If the loop voltage gain is greater than 1.3, the design is feasible. It is desirable to include some emitter degeneration in the amplifier circuit, and its effect on the voltage gain can be determined as follows. At frequencies where the amplifier voltage gain is essentially independent of frequency, the effect of emitter degeneration can be determined by substituting $r_e + r_E$ for r_e in Equation (8-93). At higher frequencies it is advisable to measure the voltage gain as a function of r_E .

The new value of $R_{in(p)}$ is then calculated substituting $r_e + r_E$ for r_e in Equation (8-94) and the new values of X_{CS} and A_V determined using the equations previously given.

(b) If the loop gain calculated using the lowest measured voltage gain is less than 1.3, the design is not feasible and must be repeated. The alternatives are then to use a better transistor (in general, a transistor with a higher $h_{FE \min}$ or BV_{CEO} at low frequencies; higher f_T above 10 MC) or accept a power output reduction. For the latter course the loop voltage gain can be increased by increasing R_T or decreasing X_{Leff} . Increasing R_T also decreases the collector current required, while decreasing X_{Leff} reduces the collector-emitter voltage allowed. The loop gain is approximately proportional to the ratio of R_T to X_{Leff} , and a given percentage reduction in X_{Leff} or increase in R_T will result in similar increases in loop voltage gain. Therefore, since the minimum oscillator power output is approximately proportional to V_{CE}^2 and inversely proportional to R_T (neglecting R), the reduction in

oscillator power output is generally smaller when R_T is increased. $R_{in(p)}$ is also increased due to the reduction in emitter current, allowing X_{C_S} to be increased. This will also cause an increase in loop voltage gain.

When designing below the cutoff frequency f_V , the value of R_T can be determined by calculation. Above f_V an experimental approach is recommended; the transistor current levels being appropriately adjusted to suit the loads used. Adjustments of R_T are made until values of G_V , $R_{in(p)}$, and A_V are obtained that result in a loop gain of 1.3 or greater.

The effect of an emitter degeneration resistor is then investigated using the approach outlined in (a).

Step 5

Determine the base biasing resistor values by the method shown in Paragraph 3-26, or by any other suitable method, and calculate $R_{b(p)}$, the input resistance of this network.

The value of $\frac{\Delta V_{BG}}{V_{BG}}$ to be used in the calculation of the required base biasing network currents is a matter of choice for the designer. A small $\frac{\Delta V_{BG}}{V_{BG}}$ will result in a stable transistor working point and a low value of $R_{b(p)}$ and vice-versa.

Compare $R_{b(p)}$ with $R_{in(p)}$ to determine the π network loading incurred. $R_{b(p)}$ will usually be large compared to $R_{in(p)}$ and can be ignored. If not, X_{C_S} should be decreased appropriately and a corresponding amplifier gain increase made.

Step 6, Calculation of Remaining Component Values

Calculate:

$$C_S \text{ from } X_{C_S}$$

Estimate $C_{in(p)}$ from the plots given in Figure 3-12 using the relative values of transistor f_T 's and C_{ob} 's as a guide.

$$\text{Actual } C_S \approx C_S - C_{in(p)} \quad (8-98)$$

$$X_{C_L} = X_e - X_{Leff} - X_{C_S} \quad (8-99)$$

$$C_L = \frac{1}{\omega X_{C_L}} \quad (\text{or } \frac{X_e}{X_{C_L}} \cdot C_L) \quad (8-100)$$

X_{C_T} is obtained from Figure 8-11 and the known value of R .

$$C_T = \frac{1}{\omega X_{C_T}} \quad (\text{or } \frac{X_e}{X_{C_T}} \cdot C_L) \quad (8-101)$$

The collector tuning network values are difficult to estimate because of the dependence of the output capacitance on the base terminating impedance. At the lower frequencies of the range, $C_{O(p)}$ can be expected to be 10 to 30 times C_{Ob} , falling to 1 to 5 C_{Ob} at 20 MC. It will probably be necessary to adjust the tuning network values experimentally to obtain correct tuning.

The effective parallel resistance of the tuning inductor should be large compared to R_T to avoid reducing the loop gain and to optimize the output power.

Calculation of emitter circuit components - The total resistance required in the emitter circuit is:

$$R_E + r_e = \frac{V_{BG}^{-0.7}}{I_E} \quad (8-102)$$

If r_e is significant, subtract to find R_E .

Determination of emitter decoupling capacitor value - The amplifier input resistance as seen at the emitter decoupling point will not be much greater than $r_e + r_E$. Therefore, it is desirable that the reactance of the decoupling capacitor X_{CE} should be not greater than one-tenth of $r_e + r_E$.

That is:

$$X_{CE} \approx \frac{r_e + r_E}{10} \quad (8-103)$$

Then:

$$C_E = \frac{1}{\omega X_{CE}} \quad (\text{or } \frac{X_e}{X_{CE}} \cdot C_L) \quad (8-104)$$

If no emitter degeneration is used, this may be difficult to achieve because of the low value of r_e and, hence, the large C_E required. The best that can then be achieved will probably be the selection of a value of C_E that is self-resonant at the design frequency.

The emphasis in the preceding design procedure is on obtaining a relatively high oscillator output power since this type of Pierce circuit is particularly advantageous in this application. However, this configuration need not be confined solely to high output power designs, and it is equally valid when only a few milliwatts of power output is required. In this case, the amplifier total load resistance R_T and hence the oscillator external load can be increased appreciably, and it is then possible to reduce the amplifier voltage gain by introducing a large emitter degeneration resistance with a value of, say, 20 ohms or larger. This in turn will make the amplifier voltage gain essentially frequency-independent and equal to its low frequency value up to 20 MC and also increase the amplifier input resistance and capacitance.

For low output power requirements, therefore, the stipulation of, say, 20 ohms of emitter degeneration enables the design to be determined by means of a simple calculation. At the higher frequencies in particular, this approach is therefore perhaps superior to the basic Pierce insofar as design simplicity is concerned, although it does have the disadvantage of requiring an additional tuning capacitor.

8-23. OSCILLATOR DESIGN EXAMPLES

The following design examples illustrate the application of the design procedure at various frequencies of the 0.8 to 20 MC range. The transistor types used in these designs were chosen for the following reasons:

(a) The 2N706A is probably the least costly silicon transistor available at this time. It does, however, have a reasonable gain-bandwidth product which makes its use feasible for medium power output designs particularly below 10 MC.

(b) The 2N2219 represents a compromise between cost and performance characteristics. It is at present a medium priced transistor with characteristics that are apparently unique; namely, a reasonable gain-bandwidth product, a high h_{FEmin} , a relatively large power dissipation, and a relatively high V_{CEO} . The high V_{CEO} and large power dissipation are admirably suited to high power oscillator design at the lower frequencies of the range.

8-24. 800 KC, 2N2219 Pierce Oscillator Using An Isolating Resistor

The CR-18A/U crystal unit characteristics are:

$$X_e = 6250 \text{ ohms}$$

$$R_{\text{emax}} = 625 \text{ ohms}$$

$$P_{\text{CMAX}} = 10 \text{ MW}$$

$$V_{\text{omax}} \text{ per unit } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 9.2 \text{ VRMS}$$

Transistor characteristics (2N2219):

$$\text{Maximum Power Dissipation at } 105^{\circ}\text{C} = 380 \text{ MW}$$

$$BV_{\text{CEO}} = 30 \text{ V}$$

$$\text{Permissible collector signal voltage} = 7.5 \text{ VRMS}$$

$$V_{\text{CE}} = 10 \text{ VDC}$$

$$\text{Necessary } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 0.7 \text{ (use a value of 1)}$$

$$R = 1.7 \text{ K}$$

$$\text{Permissible } I_{\text{C}} = 38 \text{ MA (use 35 MA)}$$

$$R_{\text{T}} = 290 \text{ ohms}$$

$$R_{\text{L}} = 350 \text{ ohms}$$

$$h_{\text{FEmin}} = 85$$

$$\text{Typical } f_{\text{T}} \approx 350 \text{ MC}$$

$$r_e \approx 1 \text{ ohm (} r' \approx 0.3 \text{ ohm)}$$

$$r_{\text{bb}}' = 60 \text{ ohms}$$

$$C_{cb'} = 3 \text{ PF}$$

$$X_{C_{cb'}} = 67 \text{ K}$$

$$r_{bb'}(1 - \alpha_o) \approx 0.7 \text{ ohm}$$

$$G_{V_o} \approx 170$$

$$\frac{R_T}{X_{C_{cb'}}} (r_e + r_{bb'}) \approx 0.26$$

$$R_{b'e} = 85 \text{ ohms}$$

$$r = 35 \text{ ohms}$$

$$\frac{r}{r_E} = 35$$

$$\left(\frac{f}{f_T}\right)^2 = 5.2 \times 10^{-6}$$

$$R_{in(p)} \approx 145 \text{ ohms}$$

$$R_{in(p)} < 3.6 R_{emax}$$

$$X_{CS} = 24 \text{ ohms}$$

$$A_V = 0.082$$

$$G_{V_L} = 1.4$$

Let $r_E = 5 \text{ ohms}$

$$R_{in(p)} \approx 630 \text{ ohms}$$

$$X_{CS} = 105 \text{ ohms}$$

$$G_V = 43$$

$$A_V = 0.036$$

$$G_{V_L} = 1.5$$

Biasing Network:

With a 28 VDC supply and $V_{CE} = 10$ VDC, $V_{BG} \approx 18$ VDC.

For ΔV_{BG} of 2.2 VDC, $\Delta I_E \approx 12$ percent. These values were used as an example in Paragraph 3-26 and gave:

$$R_{b1} = 10 \text{ K}$$

$$R_{b2} = 30 \text{ K}$$

$$R_{b(p)} = 7.5 \text{ K}$$

$R_{b(p)}$ is more than 10 $R_{in(p)}$ and can be ignored.

Calculation of remaining components:

$$C_S = 1900 \text{ PF}$$

$$C_{in(p)} \approx 200 \text{ PF}$$

Estimated physical $C_S \approx 1700 \text{ PF}$ (actual was 1600 PF)

$$X_{C_L} = 5.5 \text{ K}$$

$$C_L = 36 \text{ PF}$$

$$X_{C_T} = 460 \text{ ohms}$$

$$C_T = 430 \text{ PF}$$

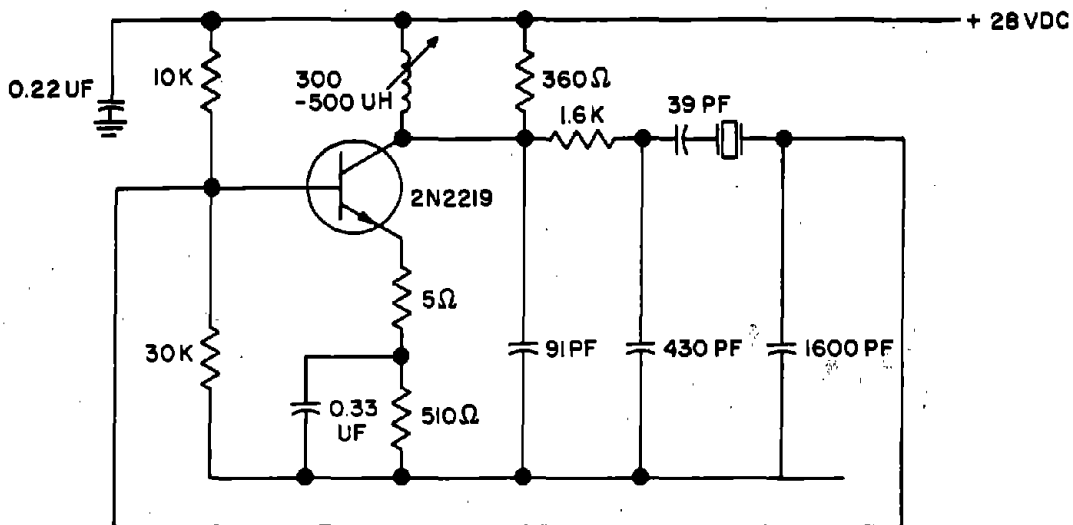
$$R_E = 510 \text{ ohms}$$

$$X_{CE} \approx 0.6 \text{ ohm}$$

$$C_E = 0.33 \text{ UF}$$

DESIGN EVALUATION DATA
0.8 MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N2219)
(All results obtained using limit crystal)

Crystal Units (CR-18A/U)	Parallel Resonant Frequency (MC)	R _e (Ohms)
1	0.799993	570
2	0.799998	590
3	0.800006	560
4	0.799999	630



TP1072-120

Figure 8-16. 0.8-MC Isolating Resistor Pierce Oscillator Circuit (2N2219),
Schematic Diagram

DESIGN EVALUATION DATA
0.8 MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N2219)
(All results obtained using limit crystal)

Effect of		Change
+15% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = +15\%$
-20% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = -22\%$
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o	< ± 1 PPM $\Delta V_o = \pm 8\%$
-55°C to +105°C Change in T_a on Oscillator	Frequency V_o	± 14 PPM $\Delta V_o = \pm 7\%$
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		< ± 2 PPM
Transistor Inter- change (5 units, retuning to maxi- mum output)	Frequency V_o	< ± 1 PPM $\Delta V_o = \pm 1\%$
Crystal Unit Interchange	Frequency miscorrelation V_o	± 3 PPM $\Delta V_o = \pm 3\%$

8-25. 5 MC, 2N2219 Pierce Oscillator Using An Isolating Resistor

The CR-18A/U crystal unit characteristics are:

$$X_e = 1 \text{ K}$$

$$R_{\text{emax}} = 60 \text{ ohms}$$

$$P_{\text{CMAX}} = 10 \text{ MW}$$

$$V_{\text{omax}} \text{ per unit } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 2.9 \text{ VRMS}$$

Transistor Characteristics (2N2219):

$$\text{Maximum Power Dissipation at } 105^{\circ}\text{C} = 380 \text{ MW}$$

$$BV_{\text{CEO}} = 30 \text{ V}$$

$$\text{Permissible collector signal voltage} = 7.5 \text{ VRMS}$$

$$V_{\text{CE}} = 10 \text{ VDC}$$

$$\text{Necessary } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 3.5$$

$$R = 2.3 \text{ K}$$

$$\text{Permissible } I_{\text{C}} = 38 \text{ MA (use 35 MA)}$$

$$R_{\text{T}} = 290 \text{ ohms}$$

$$R_{\text{L}} = 330 \text{ ohms}$$

$$h_{\text{FEmin}} = 85$$

$$\text{Typical } f_{\text{T}} \approx 350 \text{ MC}$$

$$r_e = 1 \text{ ohm (} r' \approx 0.3 \text{ ohm)}$$

$$r_{\text{bb}'} = 60 \text{ ohms}$$

$$C_{cb'} = 3 \text{ PF}$$

$$X_{Ccb'} = 10.7 \text{ K}$$

$$r_{bb'}(1 - \alpha_o) \approx 0.7 \text{ ohm}$$

$$\frac{R_T}{X_{Ccb'}} (r_e + r_{bb'}) = 1.7$$

Operation is in the vicinity of f_V . Therefore, G_V will be down probably 20 percent from G_{V_o} .

$$0.8 G_{V_o} = 136$$

$$R_{b'e} = 85 \text{ ohms}$$

$$r = 35 \text{ ohms}$$

$$\frac{r}{r_E} = 35$$

$$\left(\frac{f}{f_T}\right)^2 = 2 \times 10^{-4}$$

$$R_{in(p)} = 112 \text{ ohms}$$

$$< 3.6 R_{emax}$$

$$X_{CS} = 19 \text{ ohms}$$

$$A_V = 0.0216$$

$$G_{V_L} = 2.9$$

Loop gain is high and can be reduced by emitter degeneration.

Let r_E equal 12 ohms.

$$R_{b'E} = 1.1 \text{ K}$$

$$R_{in(p)} = 1 \text{ K}$$

$$X_{CS} = 77 \text{ ohms}$$

$$A_V = 0.097$$

$$G_V \approx 21$$

$$G_{VL} = 2$$

Biasing Network:

See 800 KC Design Example

$$R_{b1} = 10 \text{ K}$$

$$R_{b2} = 30 \text{ K}$$

$$R_{b(p)} = 7.5 \text{ K}$$

The combined input resistance is 900 ohms, reducing X_{CS} to 73 ohms. The loop gain will still be adequate.

$$C_S = 440 \text{ PF}$$

$$C_{in(p)} \approx 150 \text{ PF}$$

Estimated Physical $C_S \approx 300 \text{ PF}$ (actual was 220 PF)

$$X_{C_L} = 716 \text{ ohms}$$

$$C_L = 45 \text{ PF}$$

$$X_{C_T} = 207 \text{ ohms}$$

$$C_T = 155 \text{ PF}$$

$$R_E = 500 \text{ ohms}$$

$$X_{CE} \approx 0.6 \text{ ohm}$$

$$C_E = 0.05 \text{ UF}$$

DESIGN EVALUATION DATA
 5-MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N2219)
 (All results obtained using limit crystal)

<u>Crystal Units</u> (CR-18A/U)	<u>Parallel Resonant</u> <u>Frequency (MC)</u>	<u>R_e</u> <u>(Ohms)</u>
1	4.999956	16
2	4.999924	15
3	4.999973	24
4	4.999952	60

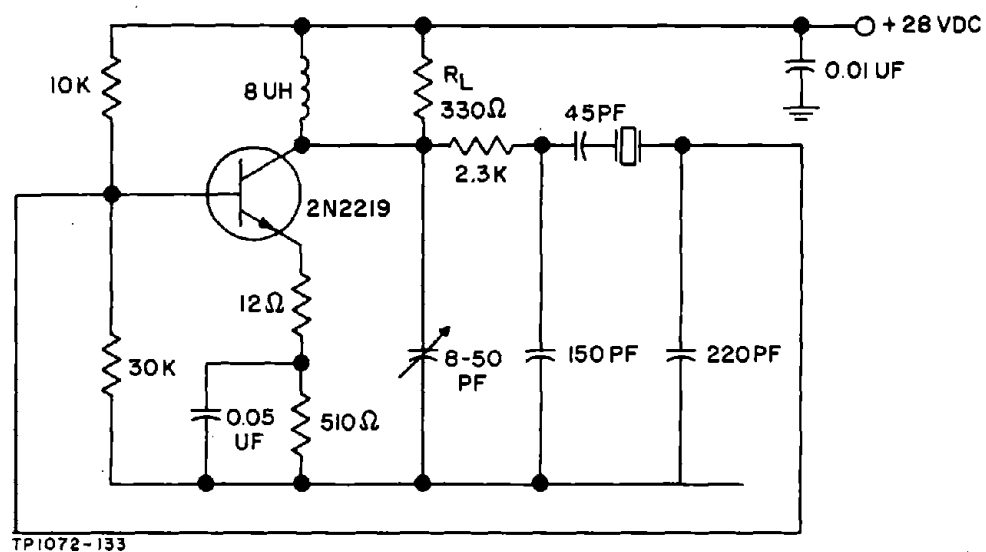


Figure 8-17. 5-MC Isolating Resistor Pierce Oscillator Circuit (2N2219),
 Schematic Diagram

DESIGN EVALUATION DATA
 5-MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N2219)
 (All results obtained using limit crystal)

Effect of		Change
+15% B+ Change on Oscillator	Frequency V_o	$< 1 \text{ PPM}$ $\Delta V_o = +17\%$
-20% B+ Change on Oscillator	Frequency V_o	$< 1 \text{ PPM}$ $\Delta V_o = -21\%$
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o	$< \pm 1 \text{ PPM}$ $\Delta V_o = \pm 7\%$
-55°C to $+105^\circ\text{C}$ Change in T_a on Oscillator	Frequency V_o	$\pm 11 \text{ PPM}$ $\Delta V_o = \pm 5\%$
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		$< \pm 2 \text{ PPM}$
Transistor Inter- change (5 units, retuning to maxi- mum output)	Frequency V_o	$< \pm 2 \text{ PPM}$ $\Delta V_o < 1\%$
Crystal Unit Interchange	Frequency miscorrelation V_o	$\pm 2 \text{ PPM}$ $\Delta V_o = \pm 14\%$

8-26. 20-MC, 2N2219 Pierce Oscillator Using An Isolating Resistor

The CR-18A/U crystal unit characteristics are:

$$X_e = 250 \text{ ohms}$$

$$R_{\text{emax}} = 20 \text{ ohms}$$

$$P_{\text{CMAX}} = 5 \text{ MW}$$

$$V_{\text{omax}} \text{ per unit } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 1.16 \text{ VRMS}$$

Transistor Characteristics (2N2219)

$$\text{Maximum Power Dissipation at } 105^\circ \text{C} = 380 \text{ MW}$$

$$BV_{\text{CEO}} = 30 \text{ V}$$

At the transistor bias levels used in the previous examples, the amplifier is working well above the cutoff frequency at 20 MC. At $I_E = 30 \text{ MA}$ the voltage gains with 500-ohm and 1-K amplifier loads were 45 and 50, respectively. Reference to Table 3-6 shows that $R_{\text{in(p)}}$ is approximately 70 ohms under these conditions, giving $A_V \approx 63$. The loop gain is therefore inadequate. The loop gain can be increased by either decreasing X_{Leff} or increasing R_T . Experimental data showed that a voltage gain of 100 was obtainable when $R_T = 820 \text{ ohms}$ and $I_E = 12 \text{ MA}$. Then:

$$V_{\text{CE}} = 10 \text{ V}$$

$$\frac{X_{\text{Leff}}}{R_{\text{emax}}} = 8.6$$

$$R = 4.4 \text{ K}$$

$$R_L = 1 \text{ K}$$

$$h_{\text{FEmin}} = 75$$

$$\text{Typical } f_T \approx 340 \text{ MC}$$

$$r_e = 2.4 \text{ ohms} \quad r' \approx 0.3 \text{ ohm}$$

$$R_{in(p)} = 90 \text{ ohms}$$

$$X_{CS} = 13.4 \text{ ohms}$$

$$A_V = 0.019$$

$$G_{V_L} = 1.9$$

$$\text{For } r_E = 30 \text{ ohms}$$

$$\text{Measured } G_V = 20$$

$$R_{b'E} = 2400 \text{ ohms}$$

$$r = 59 \text{ ohms}$$

$$\left(\frac{f}{f_T}\right)^2 = 33 \times 10^{-4}$$

$$R_{in(p)} = 1700 \text{ ohms}$$

$$X_{CS} = 58 \text{ ohms}$$

$$A_V = 0.083$$

$$G_{V_L} = 1.7$$

For a 28 VDC supply and $V_{CE} = 10 \text{ V}$, V_{BG} is approximately 18 V. For:

$$\Delta V_{BG} = 2.2 \text{ V}$$

$$\frac{I_{B1}}{I'_B} = 2.6$$

$$\frac{I_{B2}}{I'_B} = 1.6$$

Then:

$$\frac{\Delta I_B}{I'_B} = 0.77$$

but:

$$I'_B = \frac{12}{1.06 \times 75} = 0.15 \text{ MA}$$

Therefore:

$$I_{B_1} = 0.39 \text{ MA}$$

$$I_{B_2} = 0.24 \text{ MA}$$

and:

$$R_{b_1} = 34 \text{ K}$$

$$R_{b_2} = 75 \text{ K}$$

$$R_{b(p)} = 23 \text{ K}$$

$R_{b(p)}$ is greater than $10 R_{in(p)}$ and can be neglected.

With this value of loop gain the physical value of C_S is undesirably low and some improvement was obtained by reducing X_{CS} and the loop gain. For $X_{CS} = 40 \text{ ohms}$, $G_{V_L} = 1.2$. This low value is permissible because of the large amount of emitter degeneration employed.

$$C_S = 200 \text{ PF}$$

$$C_{in(p)} \approx 75 \text{ PF}$$

Estimated Physical $C_S \approx 125 \text{ PF}$ (Actual was 75 PF)

$$X_{C_L} = 38 \text{ ohms}$$

$$C_L = 210 \text{ PF}$$

$$X_{C_T} = 163 \text{ ohms}$$

$$C_T = 49 \text{ PF}$$

$$R_E = 1.5 \text{ K}$$

$$X_{CE} \approx 3.3 \text{ ohms}$$

$$C_E = 2400 \text{ PF}$$

DESIGN EVALUATION DATA
20-MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N2219)
(All results obtained using limit crystal)

<u>Crystal Units</u> (CR-18A/U)	<u>Parallel Resonant</u> <u>Frequency (MC)</u>	<u>R_e</u> (Ohms)
1	20.000270	7
2	20.000600	8
3	20.000400	7
4	20.000200	8
5	20.000000	20

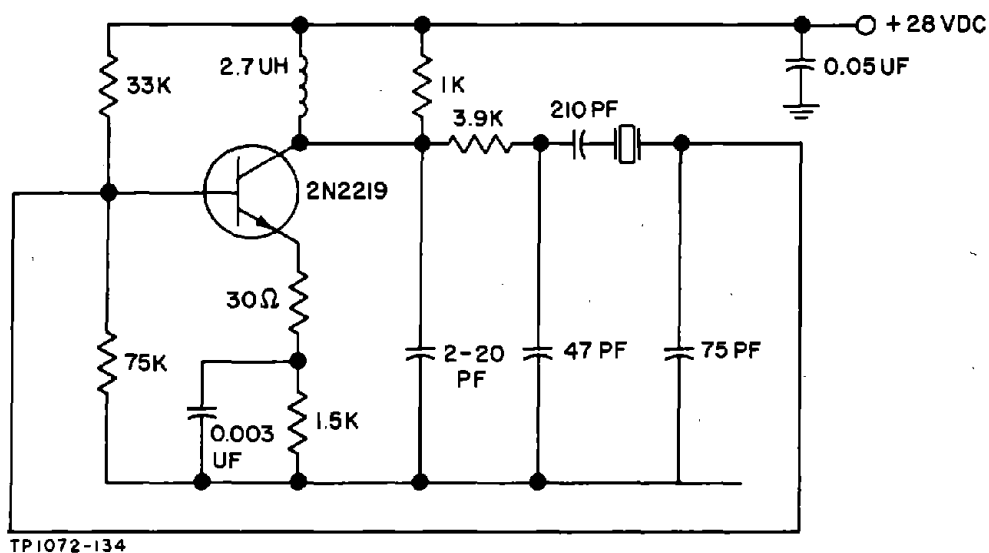


Figure 8-18. 20-MC Isolating Resistor Pierce Oscillator Circuit (2N2219),
Schematic Diagram

DESIGN EVALUATION DATA
 20-MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N2219)
 (All results obtained using limit crystal)

Effect of		Change
+15% B+ Change on Oscillator	Frequency V_o	1 PPM $\Delta V_o = +21\%$
-20% B+ Change on Oscillator	Frequency V_o	2 PPM $\Delta V_o = -31\%$
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o	$< \pm 1$ PPM $\Delta V_o = \pm 10\%$
-55°C to $+105^\circ\text{C}$ Change in T_a on Oscillator	Frequency V_o	± 25 PPM $\Delta V_o = \pm 5\%$
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		< 2 PPM
Transistor Inter- change (5 units, retuning to maxi- mum output)	Frequency V_o	< 1 PPM $\Delta V_o = \pm 10\%$
Crystal Unit Interchange	Frequency miscorrelation V_o	± 7 PPM $\Delta V_o = \pm 23\%$

8-27. 5-MC, 2N706A Pierce Oscillator Using An Isolating Resistor

The CR-18A/U crystal unit characteristics are:

$$X_e = 1 \text{ K}$$

$$R_{\text{emax}} = 60 \text{ ohms}$$

$$P_{\text{CMAX}} = 10 \text{ MW}$$

$$V_{\text{omax}} \text{ per unit } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 2.9 \text{ VRMS}$$

Transistor Characteristics (2N706A):

$$\text{Maximum Power Dissipation at } 105^{\circ}\text{C} = 140 \text{ MW}$$

$$BV_{\text{CEO}} = 15 \text{ VDC}$$

$$\text{Permissible collector signal voltage} = 3.5 \text{ VRMS}$$

$$V_{\text{CE}} = 5 \text{ VDC}$$

$$\text{Necessary } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 2$$

$$R = 740 \text{ ohms}$$

$$\text{Permissible } I_{\text{C}} = 28 \text{ MA (use 21 MA)}$$

$$R_{\text{T}} = 240 \text{ ohms}$$

$$R_{\text{L}} = 350 \text{ ohms}$$

$$h_{\text{FEmin}} = 20$$

$$\text{Typical } f_{\text{T}} \approx 300 \text{ MC}$$

$$r_e = 1.2 \text{ ohms (} r' \approx 0 \text{ ohm)}$$

$$r_{\text{bb}'} = 60 \text{ ohms}$$

$$C_{cb'} = 2.5 \text{ PF}$$

$$X_{Ccb'} = 13 \text{ K}$$

$$R_D \approx 75 \text{ K}$$

$$\frac{R_T}{R_D} (r_e + r_{bb'}) = 0.2 \text{ ohm}$$

$$\frac{R_T}{X_{Ccb'}} (r_e + r_{bb'}) = 1.2 \text{ ohms}$$

Operation is in the vicinity of f_V . Therefore, G_V will be down probably 20 percent below G_{V_o} .

$$0.8 G_{V_o} = 42$$

$$R_{b'e} = 25 \text{ ohms}$$

$$r = 18 \text{ ohms}$$

$$\frac{r}{r_e} = 15$$

$$\left(\frac{f}{f_T}\right)^2 = 2.8 \times 10^{-4}$$

$$R_{in(p)} = 78 \text{ ohms}$$

$$< 3.6 R_{emax}$$

$$X_{CS} = 13 \text{ ohms}$$

$$A_V = 0.025$$

$$G_{V_L} = 1.05$$

The loop gain is inadequate. However, since the design frequency is close to f_V and output phase angle conditions determine the value of X_{CS} , the amplifier voltage gain-input resistance product of the amplifier can be increased sufficiently using emitter degeneration.

For $r_E = 4 \text{ ohms}$

$$R_{b'E} = 110 \text{ ohms}$$

$$r = 39 \text{ ohms}$$

$$\frac{r}{r_e + r_E} = 7.5$$

$$R_{in(p)} = 170 \text{ ohms}$$

$$< 3.6 R_{emax}$$

$$X_{CS} = 28 \text{ ohms}$$

The amplifier will now be operating below f_V and:

$$G_{V_o} = 27$$

$$A_V = 0.0525$$

$$G_{V_L} = 1.4$$

The loop gain is now adequate.

Biasing Network:

For a 20 VDC supply and $V_{CE} = 5 \text{ VDC}$, V_{BG} is approximately 15 V.
For a ΔV_{BG} of 2 V, ΔI_E is 13 percent.

Then:

$$R_{b1} = 2.5 \text{ K}$$

$$R_{b2} = 15 \text{ K}$$

$$R_{b(p)} = 2.2 \text{ K}$$

$R_{b(p)}$ is more than 10 $R_{in(p)}$ and can be ignored.

Calculation of Remaining Components:

$$C_S = 1140 \text{ PF}$$

$$C_{in(p)} \approx 150 \text{ PF}$$

Estimated physical $C_S = 1000 \text{ PF}$ (actual was 510 PF)

$$X_{C_I} = 850 \text{ ohms}$$

$$C_I = 38 \text{ PF}$$

$$X_{C_T} = 110 \text{ ohms}$$

$$C_T = 290 \text{ PF}$$

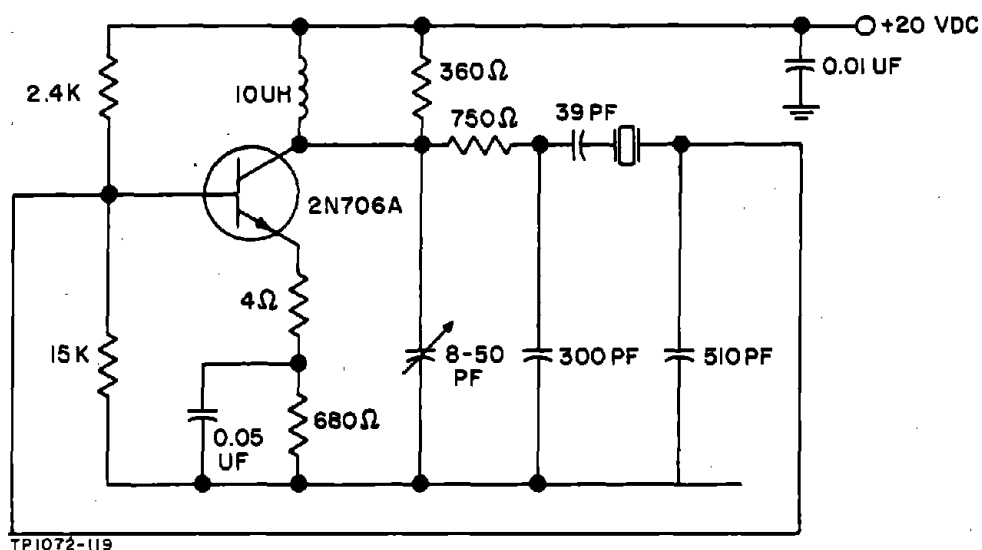
$$R_E = 720 \text{ ohms}$$

$$X_{C_E} \approx 0.5 \text{ ohm}$$

$$C_E = 0.05 \text{ UF}$$

DESIGN EVALUATION DATA
5-MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N706A)
(All results obtained using limit crystal)

<u>Crystal Units</u> (CR-18/U)	<u>Parallel Resonant</u> <u>Frequency (MC)</u>	<u>R_e</u> (Ohms)
1	4.999956	16
2	4.999924	15
3	4.999973	24
4	4.999952	60



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Figure 8-19. 5-MC Isolating Resistor Pierce Oscillator Circuit (2N706A),
Schematic Diagram

DESIGN EVALUATION DATA
5-MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N706A)
(All results obtained using limit crystal)

Effect of		Change
+15% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = +16\%$
-20% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = -23\%$
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o	< ± 1 PPM $\Delta V_o = \pm 5\%$
-55°C to $+105^\circ\text{C}$ Change in T_a on Oscillator	Frequency V_o	± 12 PPM $\Delta V_o = \pm 7\%$
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		< ± 2 PPM
Transistor Inter- change (8 units, retuning to maxi- mum output)	Frequency V_o	< ± 1 PPM $\Delta V_o = \pm 4\%$
Crystal Unit Interchange	Frequency miscorrelation V_o	± 2 PPM $\Delta V_o = \pm 6\%$

8-28. 20-MC, 2N706A Pierce Oscillator Using An Isolating Resistor

The CR-18A/U crystal characteristics are:

$$X_e = 250 \text{ ohms}$$

$$R_{\text{emax}} = 20 \text{ ohms}$$

$$P_{\text{CMAX}} = 5 \text{ MW}$$

$$V_{\text{omax}} \text{ per unit } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 1.16 \text{ VRMS}$$

Transistor Characteristics:

At the transistor bias levels used in the example of Paragraph 8-27, the amplifier is working well above the cutoff frequency at 20 MC. Experimental data shows that the loop voltage gain margin is insufficient. Increasing R_T to 500 ohms gives a voltage gain of 50 at an emitter current of 10 MA. The design calculation is then as follows:

$$BV_{\text{CEO}} = 15 \text{ VDC}$$

$$\text{Permissible collector signal voltage} = 3.5 \text{ VRMS}$$

$$V_{\text{CE}} = 5 \text{ VDC}$$

$$\text{Necessary } \frac{X_{\text{Leff}}}{R_{\text{emax}}} = 4.3$$

$$R = 1.2 \text{ K}$$

$$R_L = 880 \text{ ohms}$$

$$h_{\text{FEmin}} = 20$$

$$\text{Typical } f_T = 300 \text{ MC}$$

$$r_e = 2.5 \text{ ohms (} r' \approx 0 \text{ ohm)}$$

$$R_{\text{in(p)}} = 110 \text{ ohms}$$

$$X_{\text{CS}} = 15 \text{ ohms}$$

$$A_V = 0.042$$

$$G_{V_L} = 2.1$$

Let $r_E = 3 \text{ ohms}$

Measured

$$G_V = 30$$

$$R_{b'E} = 115$$

$$R_{in(p)} = 130 \text{ ohms}$$

$$X_{CS} = 16 \text{ ohms}$$

$$A_V = 0.047$$

$$G_{V_L} = 1.4$$

Bias Network:

For a 20 VDC supply and $V_{CE} = 5 \text{ VDC}$, $V_{BG} \approx 15 \text{ VDC}$, the condition $\Delta V_{BG} = 2 \text{ V}$ is satisfied for:

$$R_{b1} = 5 \text{ K}$$

$$R_{b2} = 30 \text{ K}$$

$$R_{b(p)} = 4.3 \text{ K}$$

$R_{b(p)}$ is more than 10 $R_{in(p)}$ and can be neglected.

$$C_S = 500 \text{ PF}$$

Estimated physical $C_{in(p)} \approx 80 \text{ PF}$

Estimated Physical $C_S \approx 400 \text{ PF}$ (Actual was 220 PF)

$$X_{C_l} = 150 \text{ ohms}$$

$$C_l = 54 \text{ PF}$$

$$X_{C_T} = 85 \text{ ohms}$$

$$C_T = 94 \text{ PF}$$

$$R_E = 1.5 \text{ K}$$

$$X_{CE} \approx 0.6 \text{ ohm}$$

$$C_E = 0.013 \text{ UF}$$

DESIGN EVALUATION DATA
20-MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N706A)
 (All results obtained using limit crystal)

<u>Crystal Units</u> <u>(CR-18A/U)</u>	<u>Parallel Resonant</u> <u>Frequency (MC)</u>	<u>R_e</u> <u>(Ohms)</u>
1	20.000270	7
2	20.000600	8
3	20.000400	7
4	20.000200	8
5	20.000000	20

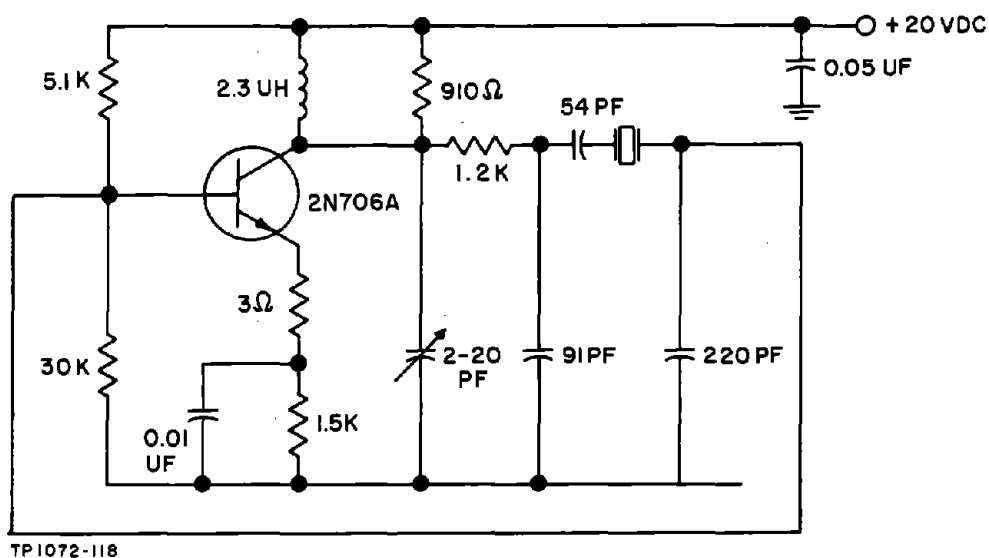


Figure 8-20. 20-MC Isolating Resistor Pierce Oscillator Circuit (2N706A),
 Schematic Diagram

DESIGN EVALUATION DATA
 20-MC ISOLATING RESISTOR PIERCE OSCILLATOR (2N706A)
 (All results obtained using limit crystal)

Effect of		Change
+15% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = +15\%$
-20% B+ Change on Oscillator	Frequency V_o	-2 PPM $\Delta V_o = -23\%$
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o	< ± 1 PPM $\Delta V_o = \pm 6\%$
-55°C to +105°C Change in T_a on Oscillator	Frequency V_o	± 25 PPM $\Delta V_o = \pm 8\%$
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test		< ± 2 PPM
Transistor Inter- change (8 units, retuning to maxi- mum output	Frequency V_o	± 3 PPM $\Delta V_o = \pm 7\%$
Crystal Unit Interchange	Frequency misrelation V_o	± 8 PPM $\Delta V_o = \pm 28\%$

8-29. DESIGN NOTES FOR TRANSISTOR ANTI-RESONANCE OSCILLATORS,
1 KC TO 500 KC

No design work has been carried out in this frequency range, and the following discussion should be regarded as a suggestion of how the design process devised for the 0.8 to 20 MC range may be adapted to produce suitable designs in a part of this range.

The major characteristics of the military type anti-resonance crystal units applicable to the 16 KC to 500 KC range are given in Table 8-3. There are no military anti-resonance crystal units below 16 KC, but crystal units having characteristics similar to those presented in Table 8-3 for the range from 1 to 16 KC are obtainable.

Comparison of the characteristics presented in Table 8-3 with those previously given for the 0.8 to 20 MC range shows that in the 90 to 500 KC range the crystal unit impedance levels are increased by roughly one order of magnitude and the dissipation rating reduced by a factor of 5 relative to those in the 0.8 to 2 MC range. And below 100 KC the relative impedance levels are increased by about 2 orders of magnitude while the dissipation rating is comparably decreased. This in general means that the permissible π network input signal voltage is comparable to that applying in the 0.8 to 20 MC range.

The range of values of the ratio $\frac{X_e}{R_{e \max}}$ is somewhat wider, ranging from 40 to 2.5 in the frequency range of 1 to 16 KC, 4.5 to 0.89 in the 16 to 100 KC range, and 18 to 1.9 in the 90 to 500 KC range.

The increase in the crystal unit impedance level also causes a similar increase in that of the π network and, since the input resistance of a common emitter amplifier at these frequencies is essentially the same as that obtaining at the lower frequencies of the 0.8 to 20 MC when using transistors with current gain-bandwidth products of 100 MC or more, an increase in the π network attenuation results. However, the π network input impedance is also increased, in turn increasing the amplifier load impedance level, resulting in an increased amplifier voltage gain. These tend to compensate to a great extent as shown by the following partial design calculation for a 500-KC basic Pierce oscillator.

The crystal characteristics are

$$R_{e \max} = 8.5 \text{ K}, P_{C\text{MAX}} = 2 \text{ MW}, X_e = 16 \text{ K}, \frac{X_e}{R_{e \max}} = 1.9.$$

TABLE 8-3. ANTI-RESONANCE CRYSTAL UNIT CHARACTERISTICS,
1 KC TO 500 KC

Frequency Range (KC)	Temperature Range (°C)	Overall Frequency Tolerance (±%)	Equivalent Resistance (Kilohms)	Dissipation Rating (MW)	Loading Capacitance (PF)	Crystal Unit Type	Crystal Holder Type
1 - 16	-40 to +70	0.015	200	0.01	20	---	---
16 - 100	-40 to +70	0.012	110 to 90	0.1	20	CR-38A/U	HC-13/U
*80 - 200	-40 to +70	0.01	5 to 6	2	32	CR-15B/U	HC-21/U
90 - 250	-40 to +70	0.02	5 and 5.5	2	20	CR-37A/U	HC-13/U
*80 - 860	-30 to +75	0.01	3	2	45	CR-43/U	HC-16/U
*200 - 500	-40 to +85	0.01	5.3 to 8.5	2	20	CR-46A/U	HC-6/U
200 - 500	-55 to +90	0.015	5.3 to 8.5	2	20	CR-63A/U	HC-6/U
TEMPERATURE CONTROLLED TYPES							
*80 - 200	70 to 80	0.002	5 to 6	2	32	CR-29A/U	HC-21/U
90 - 250	70 to 80	0.003	4.5 and 5	2	32	CR-42A/U	HC-13/U
200 - 500	70 to 80	0.002	5.3 to 8.5	2	20	CR-47A/U	HC-6/U
*500	80 to 90	0.001	3	0.5	32	CR-57/U	HC-6/U

*Special Applications

For

$$\frac{X_{Leff}}{R_{e\max}} = 1, X_{Leff} = 8.5 \text{ K}, R_L = 23 \text{ K}, K_A = 4.7,$$

$$|Z_{T\min}| = 7 \text{ K}, V_{O\max} = 5.9 \text{ VRMS.}$$

$$I_C = 1.2 \text{ MA}, V_{CE} = 8 \text{ VDC.}$$

For a transistor type having $h_{FE\min} = 15$ and using an emitter degeneration resistor of 30 ohms, $r_e + r_E \approx 50$ ohms and $R_{in(p)} \approx 800$ ohms. Then $X_{CS} = 133$ ohms, $A_V = 0.0033$, $G_V = 460$, and $G_{VL} = 1.5$.

This is the worst design case in the 90 to 500 KC range, and similar designs should therefore be feasible at the lower frequencies. It may be necessary to increase the transistor collector current to achieve a minimum current gain of 15 if the less costly types are employed. This may in turn cause an appreciable amplifier input resistance due to the biasing network.

Below 90 KC, the total load impedance will be comparable with the transistor output impedance, and the amplifier voltage gain will not be as large as expected. This can be improved by employing a larger emitter degeneration resistor which will reduce the amplifier voltage gain, increase its input resistance, and allow a decrease in the π network attenuation. However, the base biasing network input resistance may then be a limiting factor preventing a suitable loop voltage gain from being attained. There are several possible methods of reducing this effect such as, for example, bootstrapping the base resistors AC-wise to the transistor emitter or using two transistors in a Darlington connection (emitter follower driving the common emitter amplifier), thereby reducing the first stage DC base current requirements and increasing the amplifier input resistance by a factor of approximately $h_{FE\min}$.

The isolating resistor Pierce appears feasible in the 90 to 500 KC range, provided that the transistor type has a high minimum common emitter current gain. Judging by quick calculations feasible designs should be obtainable for $h_{FE\min}$ values of 50 or more. This configuration does not appear to be practicable below 90 KC, except in multiple transistor designs.

SECTION 9

VACUUM TUBE ANTI-RESONANCE OSCILLATOR DESIGN

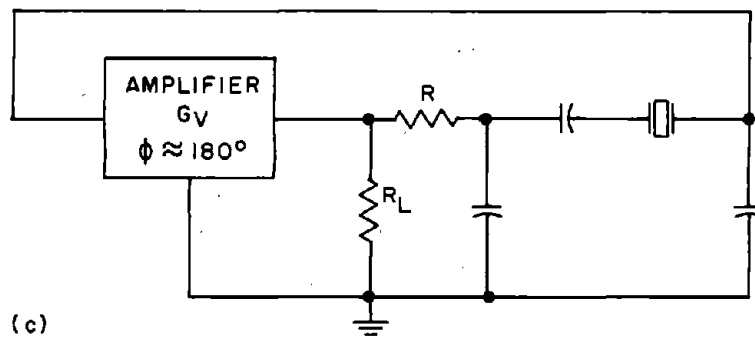
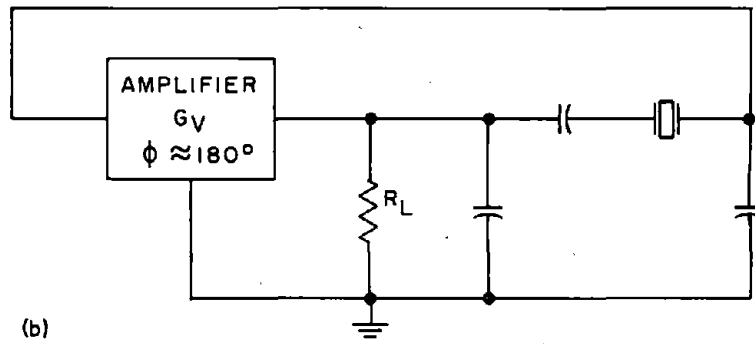
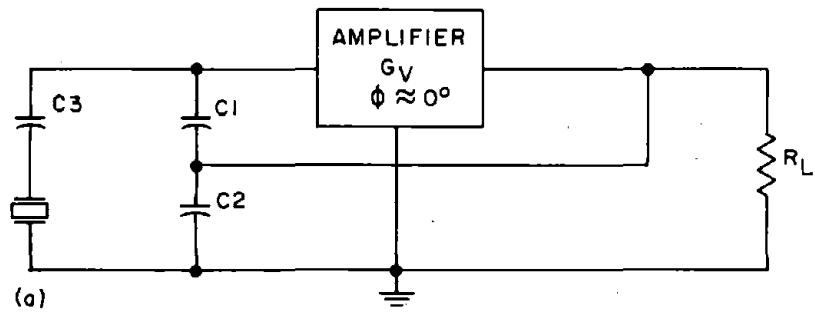
9-1. INTRODUCTION

The anti-resonance crystal unit is suited for use in the circuits of Figure 9-1. In the circuit shown in Figure 9-1(a), the amplifier output resistance and load can be considered as reflected in parallel with the amplifier input by the impedance transforming network consisting of C_1 and C_2 . The effective capacitance of C_1 and C_2 in series operating in conjunction with C_3 then transforms the combined input and output resistance of the amplifier to a suitable terminating level for the crystal unit. The amplifier is required to have a nominal zero phase shift and is usually in the form of a cathode follower.

In the circuit of Figure 9-1(b) the crystal unit operates as the inductive element of a π network of the type analyzed in Paragraph 1-10, where the impedance transforming action is discussed in detail. In this circuit the amplifier is required to have nominal phase inverting properties and is usually in the form of a common cathode amplifier.

A useful variant of this circuit is obtained by interposing a resistor between the π network and the amplifier output, as shown in Figure 9-1(c). One advantage of this circuit relative to that of Figure 8-1(b) is the increased output power that can be obtained for a comparable crystal unit loading or, alternatively, the reduction in loading that can be obtained for comparable output power. However, the major advantage in tube oscillators is the larger allowable plate signal voltage in this circuit. Over a substantial portion of the frequency range the characteristics of crystal units are such that, in the circuits of Figure 9-1(a) and (b), it is necessary to limit the plate signal voltage to less than 10 VRMS in order to avoid exceeding the crystal unit dissipation rating. This is difficult to achieve with conventional tubes if the tube is to provide the limiting action, without sacrificing the desirable characteristics of the amplifier. In the circuit of Figure 9-1(c) the allowable plate signal voltage is approximately doubled relative to that of the other two and therefore gives considerable relief in this respect. This subject is dealt with in more detail in the subsequent discussion.

The circuits of Figure 9-1(a) and (b) are often referred to as the Pierce type oscillator after their originator. In order to distinguish them from the circuit of Figure 9-1(c), which is a variant of these circuits, they will be referred to here as the "basic" Pierce oscillator and the circuit of Figure 9-1(c) will be referred to as the "isolating resistor" Pierce oscillator.



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Figure 9-1. Anti-resonance Oscillator Circuits

There is another method of using an anti-resonant crystal unit where it is connected in series with a capacitor having the specified value of loading capacitance C_L . This series combination behaves in essentially the same manner as a series type crystal unit, and the design of the oscillator circuit becomes essentially that of a series oscillator. For this type of circuit, reference should be made to the appropriate handbook section dealing with the design of series oscillators in the particular frequency range of interest.

The characteristics of crystal units vary drastically across the frequency range, and it is impractical to discuss the design of this type of oscillator at all frequencies simultaneously. The discussion is therefore divided into three parts dealing with the frequency ranges of 1 to 100 KC, 90 to 500 KC, and 800 KC to 20 MC. The latter is probably the most used range and is presented first.

9-2. TRIODE ANTI-RESONANCE OSCILLATOR DESIGN, 0.8 TO 20 MC RANGE

9-3. Crystal Unit Characteristics

The available crystal unit types and their more pertinent characteristics are given in Table 9-1. More detailed information is contained in MIL-C-3098, Supplement 1. With the exceptions of the CR-33A/U and the CR-71/U, these are all fundamental mode crystal units having similar characteristics in those frequency regions where overlap occurs. The CR-33A/U is a special application unit which should not be used in new military equipments without governmental permission (see Table 1-5).

The CR-71/U is a fifth overtone unit intended for use in high-precision crystal oscillators. This type of oscillator requires special circuit provisions such as close tolerance crystal unit temperature control, automatic gain control to maintain crystal dissipation virtually constant, and well regulated supply voltage. This type of operation is beyond the scope of this discussion, and this crystal unit is only included to give complete coverage of the crystal unit types available.

Below 2.9 MC for wide temperature applications there is no real choice of crystal units available to the designer. The CR-18A/U and CR58A/U units have identical performance characteristics, and the sole difference is in the holder pin-size. Above 2.9 MC for wide temperature range applications, there is a choice of three overall frequency tolerances: ± 0.002 percent (CR-69/U), ± 0.0025 percent (CR-66/U), and 0.005 percent (CR-78/U, CR-18A/U, and CR-64/U). The CR-66/U gives a 2-to-1 improvement in overall frequency tolerance over the other types above 3 MC. However, greater care is required in its manufacture, and a higher cost can be expected.

TABLE 9-1. ANTI-RESONANCE CRYSTAL UNITS, 0.8 TO 25-MC RANGE

Frequency Range (MC)	Temperature Range (°C)	Overall Frequency Tolerance (±%)	Equivalent Resistance	Dissipation Rating (MW)	Loading Capacitance (PF)	Max. Co (PF)	Crystal Unit Type	Crystal Holder Type
WIDE TEMPERATURE RANGE TYPES								
0.8 to 20	-55 to +105	0.005	625 to 20	10 and 5	32	7	CR-18A/U	HC-6/U
0.8 to 20	-55 to +105	0.005	625 to 20	10 and 5	32	7	CR-58A/U	HC-17/U
2.9 to 20	-55 to +105	0.002	175 to 25	5	30	7	CR-69/U	HC-18/U
3 to 20	-55 to +105	0.0025	60 to 25	10 and 5	30	7	CR-66/U	HC-6/U
3 to 20	-55 to +105	0.005	175 to 25	5	30	7	CR-78/U	HC-25/U
4 to 20	-55 to +105	0.005	120 to 25	5	30	7	CR-64/U	HC-18/U
10 to 25	-55 to +105	0.005	65 to 17	2.5	32	12	CR-33A/U	HC-6/U
TEMPERATURE CONTROLLED TYPES								
0.8 to 20	+70 to +80	0.002	625 to 20	5 and 2.5	32	7	CR-27A/U	HC-6/U
0.8 to 20	+80 to +90	0.002	625 to 20	5 and 2.5	32	7	CR-36A/U	HC-6/U
0.8 to 20	+70 to +80	0.001	600 to 20	5 and 2.5	32	7	CR-62/U	HC-6/U
3 to 20	+70 to +80	0.002	40 to 15	5	32	7	CR-68/U	HC-6/U
4.5 to 5.5	±0.5 (65 to 77°C)	0.00008	100 to 175		32	4	CR-71/U	HC-30/U

Among the temperature controlled units, the CR-62/U gives the best overall frequency tolerance. However, its comparatively low operating temperature only allows its use in applications where the ambient temperature does not exceed approximately 65°C. The higher temperature types can be used in ambient temperatures of up to approximately 75°C, but at the expense of a doubling of the overall frequency tolerance.

The crystal unit maximum equivalent resistance varies considerably as a function of frequency, as shown in Figure 9-2 for the CR-18A/U and the CR-64/U types. These plots are also representative of $R_{e \text{ max}}$ in the other available types. The minimum value of equivalent resistance likely to be encountered is perhaps $1/9 R_{e \text{ max}}$.

These units are designed to operate in conjunction with either a 30 or 32 PF loading capacitance, depending on type. The magnitude of this value of capacitive reactance X_{CL} is therefore equal to the inductive reactance of the crystal unit X_e at its operating frequency. This is an important design parameter, and the variation of X_e or X_{CL} across the frequency range is given in Figure 9-3 for future reference.

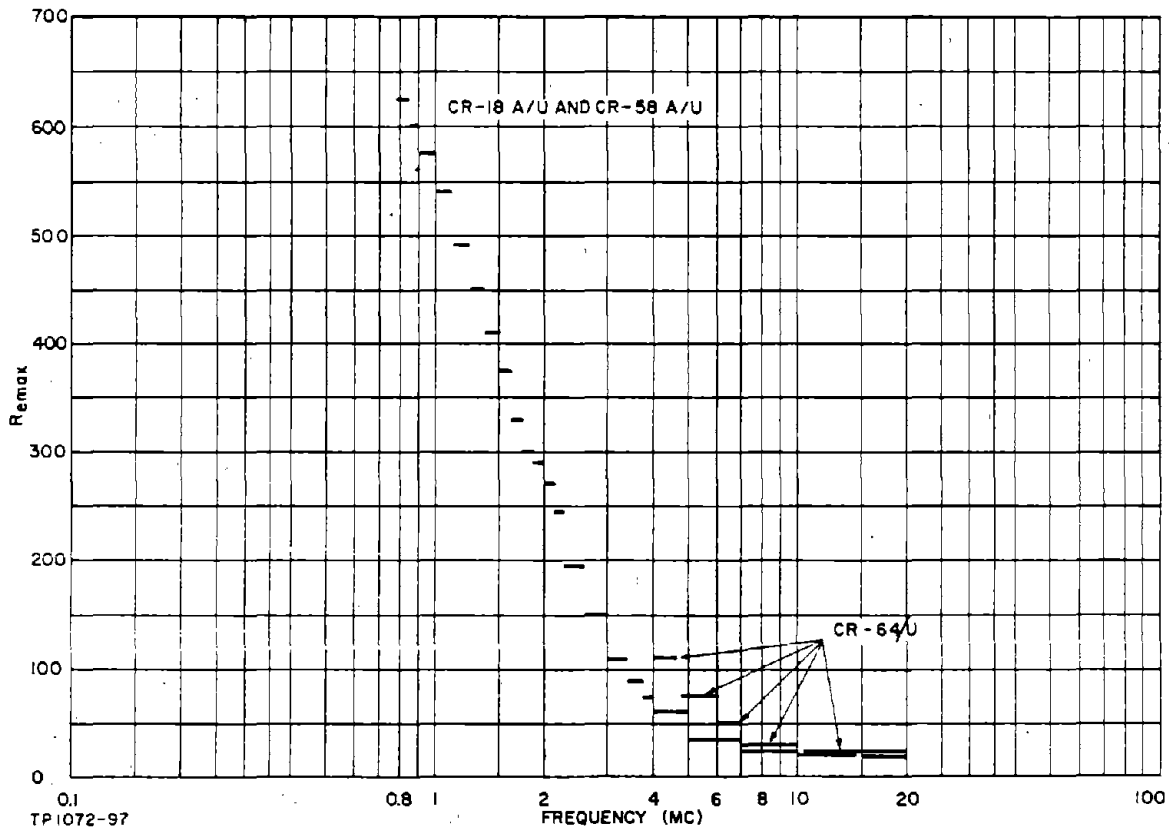


Figure 9-2. Variation of $R_{e \text{ max}}$ With Frequency

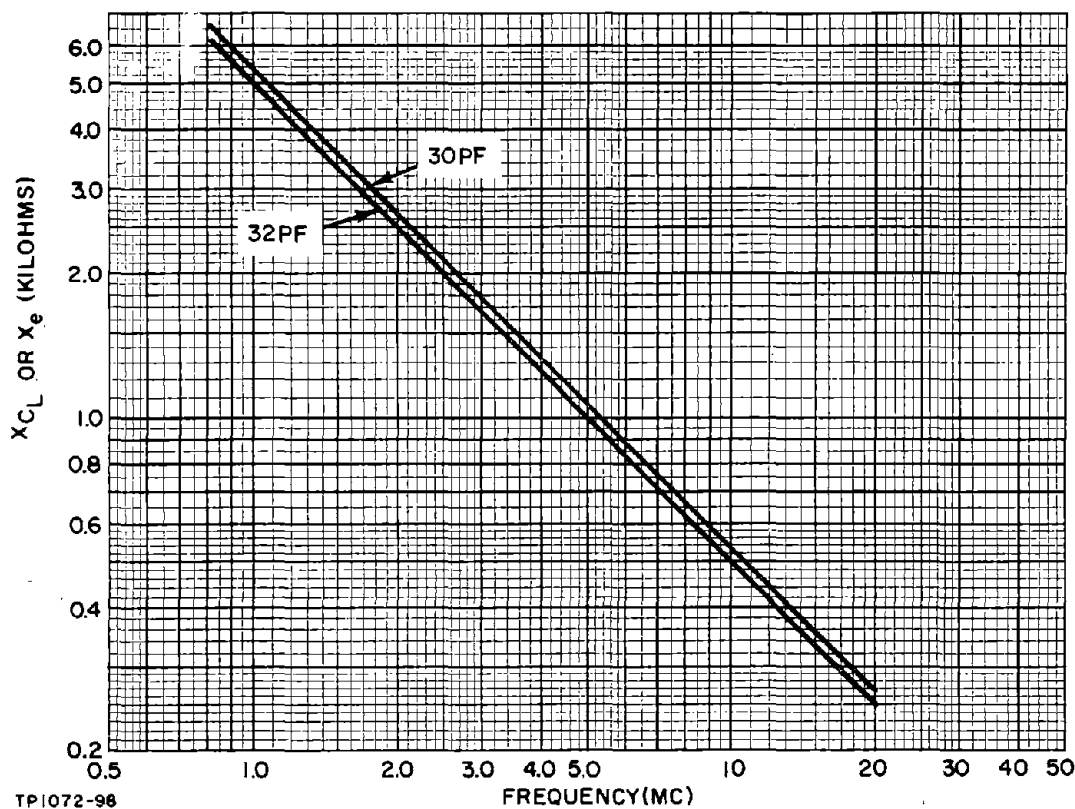


Figure 9-3. Value of X_{CL} or X_e for a 30 or 32 PF Loading Capacitor

The actual anti-resonance frequency f'_a of the crystal unit and loading capacitance combination is critically determined by the value of C_L . In practice, a part of C_L is contributed by the amplifier portion of the oscillator circuit, and this part varies in response to changes in the circuit operating conditions. It is therefore desirable to know the sensitivity of the anti-resonance frequency to changes in C_L in order to assess the precautions to be taken to hold the change of f'_a to a suitable value. This relationship was determined experimentally for several CR-18A/U crystal units using a CI meter, and the results are given in Table 9-2. It appears from these results that, over the greater part of the frequency range, a change of f'_a of 3 PPM per percent change in C_L can be expected. This appears to decrease by a factor of 3 at the very low frequencies of the range.

The asterisks in Table 9-2 denote simulated "worst-case" crystal units where the equivalent resistance is made up to the maximum value $R_{e \max}$ by the addition of a series resistance. At the lower frequencies this had no noticeable effect on the frequency change obtained, but at 20 MC a marked increase resulted. However, the introduction of a series resistance when testing with the CI meter at this frequency is rather cumbersome since the loading capacitor is in the form of a plug-in unit into which, in turn, the crystal is designed to plug. Adding

TABLE 9-2. CHANGE IN f_a' DUE TO C_L CHANGE

Crystal Unit Frequency (MC)	R_e (Ohms)	Change in f_a' (PPM) for 1-PF Change in C_L (32 PF Nominal)	Change in f_a' (PPM) Per Percent Change in C_L
1	230	3	1
* 1	600	3	1
3	35	6	2
3	14	8	3
5	24	9	3
* 5	60	8	2.7
13	9	8	2.7
20	8	8	2.7
*20	20	12 - 21	4 - 7
* Artificially constructed "worst-case" units			

the makeup resistor into this circuit as a temporary measure inevitably involves long lead lengths, and it is suspected that this influenced the results obtained, since the frequency change varied over the range indicated in Table 9-2 depending on the sequence of the added resistor, the crystal unit, and the loading capacitor in the circuit. This set of values should therefore be discounted, and it appears probable that a 3 PPM change in f_a' per percent change of C_L can also be expected at this frequency.

It is evident from the values quoted for the sensitivity of f_a' to changes in C_L that the latter should not vary appreciably if the miscorrelation between crystal unit and oscillator frequencies is to be small. A 4 percent change in C_L will cause a frequency miscorrelation of approximately 12 PPM. This will probably be adequate when a ± 50 PPM crystal unit is employed. When a ± 25 PPM crystal unit is used, however, it may, in many cases, be desirable to substantially reduce this error in order to obtain maximum benefit from the decreased tolerance. The method used to reduce the effect of that part of C_L contributed by the amplifier is to introduce a relatively large parallel swamping capacitor which reduces the variations of C_L .

The remaining portion of C_L is made up of physical capacitors, and it is desirable that these should be silver mica or other stable, low temperature coefficient type capacitors if the temperature characteristics of the oscillator are to approach those of the crystal unit.

An important design parameter is the ratio $\frac{X_{Leff}}{R_{e\ max}}$. X_{Leff} must always be smaller than X_e , and therefore $\frac{X_e}{R_{e\ max}}$ represents the limiting value of $\frac{X_{Leff}}{R_{e\ max}}$. A plot of the former is given in Figure 9-4 for the CR-18A/U crystal unit for subsequent reference.

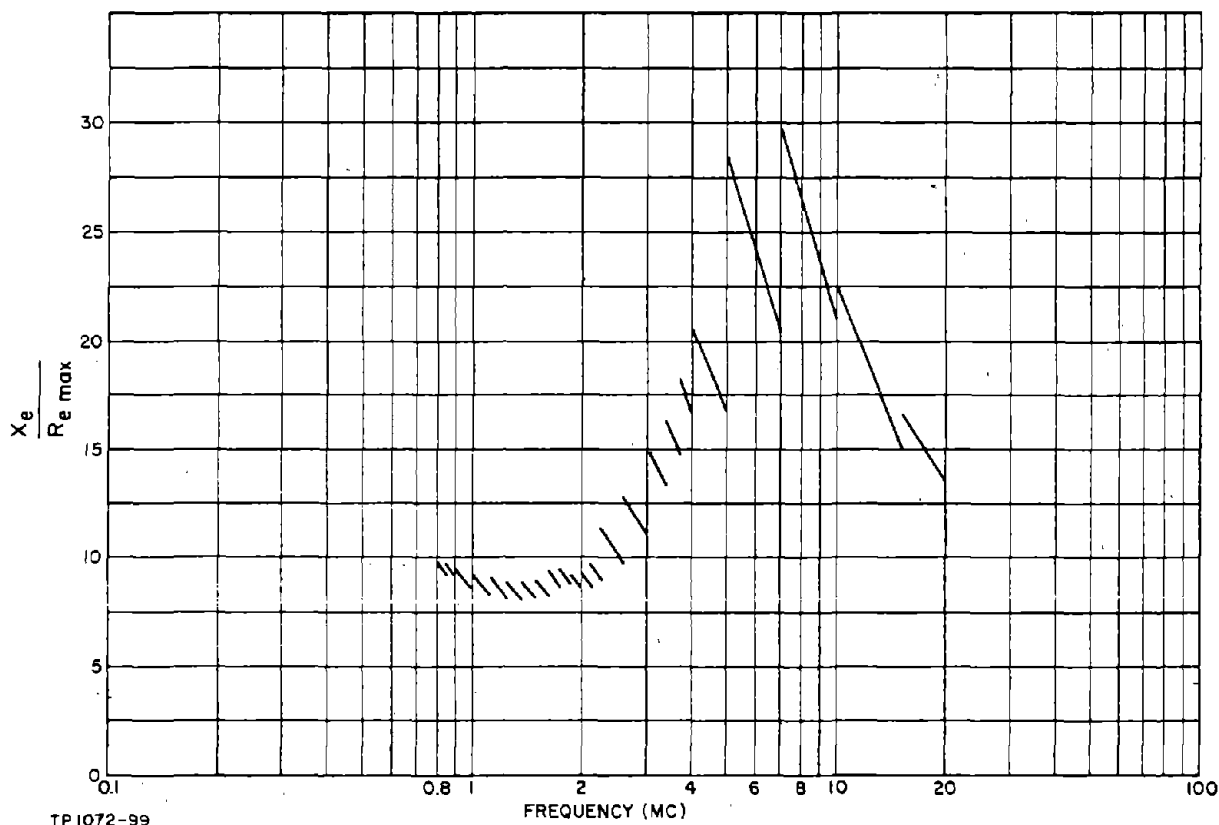


Figure 9-4. Variation of $\frac{X_e}{R_{e\ max}}$ With Frequency for a CR-18A/U Crystal Unit

9-4. Oscillator Configuration

The relatively low allowable crystal unit drive voltage and the inherently large linear signal handling capabilities of a vacuum tube amplifier make the design of a basic Pierce type oscillator difficult at all but the lowest frequencies

of this range if crystal unit overdrive is to be avoided. To illustrate this, the crystal π network analysis of Paragraph 1-10 shows that the allowable plate signal voltage in a basic Pierce circuit for the given loading conditions is:

$$V_{\pi A} = \sqrt{P_{C\text{MAX}} \cdot R_{e \text{ max}} \left[1 + \left(\frac{X_{\text{Leff}}}{R_{e \text{ max}}} \right)^2 \right]} \quad (9-1)$$

The characteristics of the CR-18A/U crystal unit are representative of the other applicable crystal types, and substituting the values of $P_{C\text{MAX}}$ and $R_{e \text{ max}}$ given in the specification sheet into Equation (9-1) for various values of $\frac{X_{\text{Leff}}}{R_{e \text{ max}}}$ results in the values of $V_{\pi A}$ given in Table 9-3.

TABLE 9-3. VALUES OF $V_{\pi A}$ FOR A CR-18A/U CRYSTAL UNIT
AT VARIOUS FREQUENCIES AS A FUNCTION OF $\frac{X_{\text{Leff}}}{R_{e \text{ max}}}$

$\frac{X_{\text{Leff}}}{R_{e \text{ max}}}$	$V_{\pi A}$ (RMS)					
	800 KC	2 MC	3 MC	5 MC	10 MC	20 MC
2	5.6					
5	12.7	8.5	6.3	4	2.5	1.6
6		10.5	7.5	4.8	3.0	1.9
8			8.4	6.3	4.0	2.6
10			10.5	7.8	4.9	3.2
13				10	4.5	4.1
20					7.0	

The largest ratios of $\frac{X_{\text{Leff}}}{R_{e \text{ max}}}$ for which values of $V_{\pi A}$ are given approach the ratios of $\frac{X_e}{R_{e \text{ max}}}$ plotted in Figure 9-4 and are therefore representative of the maximum usable values, since X_{Leff} is always smaller than X_e . Therefore, the largest values of $V_{\pi A}$ given in any column of Table 9-1 is indicative of the maximum allowable plate signal voltage at that particular frequency. In the range up to 10 MC, therefore, the permissible plate signal voltage is approximately 8 to 10 VRMS. Above 10 MC, this decreases further due to both $P_{C\text{MAX}}$ and $R_{e \text{ max}}$ decreasing, and at 20 MC the allowable plate signal voltage is reduced to 4 VRMS. The relatively large DC plate voltage levels required in conventional vacuum tubes makes it difficult to bias the tube so that limiting holds the plate signal voltage to these levels. To do this it is necessary to

operate the tube under very low DC plate voltage conditions where the variability of characteristics between individual tubes of the same type is likely to be large.

At all frequencies, therefore, the basic Pierce circuit will require critical amplifier biasing if conventional tubes are employed. It does not appear possible to determine the bias conditions that will be required from data sheets, and consequently the design approach must be largely experimental. This is not a desirable basis on which to develop a design procedure.

The alternatives are:

- (a) To use a diode circuit to provide plate signal voltage limiting.
- (b) To use low voltage tubes where the ratio of plate bias voltage to signal voltage will be reduced, resulting in good limiting at these levels.
- (c) To use the isolating resistor Pierce circuit which relaxes the limitation on plate voltage swing and also allows a considerable increase in oscillator output power, if desired.

Alternative (a) requires additional circuitry and a relatively expensive diode, particularly above 10 MC, if operation above 80°C is contemplated. Alternative (b) requires the use of 28 V subminiature tubes which also require a 28 V filament supply. These tubes are relatively expensive, and quite often a 28 V filament supply will not be available. Alternative (c) requires an additional tuned circuit.

The relative merits of these alternative approaches will depend greatly on the application. Both (a) and (b) are restricted to output voltage levels of less than $V_{\pi A}$, and for the given crystal loading, to power outputs of less than one-half of the crystal dissipation rating. Alternative (c) is capable of an output voltage of twice $V_{\pi A}$ and greatly increased power output for the same crystal loading or, alternatively, for power outputs comparable to the basic Pierce, the crystal loading can be reduced. Therefore, in general, alternative (c) gives increased design flexibility, and this is the design approach presented. The oscillator circuit is then of the form shown in Figure 9-5.

9-5. Grounded-Cathode Triode Amplifier Characteristics

a. Voltage Gain

The small signal voltage gain of a tuned-plate grounded-cathode triode amplifier is:

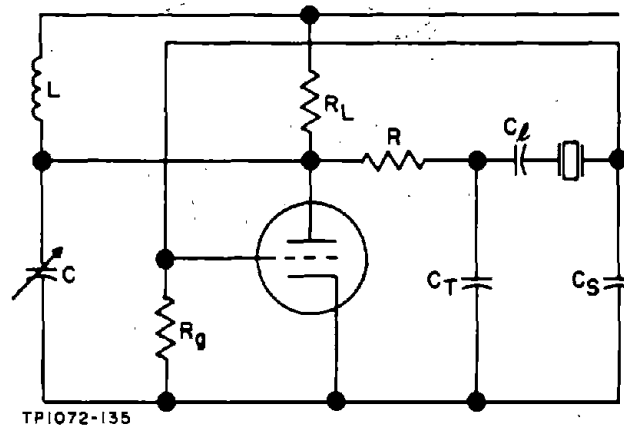


Figure 9-5. Isolating Resistor Pierce Triode Oscillator

$$G_V = \frac{\mu R_T}{R_p + R_T} \quad (9-2)$$

where μ is the tube amplification factor, R_p the plate resistance, and R_T is the total plate circuit resistance.

b. Input Impedance

The input impedance appearing at the tube control grid consists of three parts, one of which is due to feedback from the plate to the grid via the grid-to-plate capacitance C_{pg} . The other two parts consist of the grid leak resistor R_g and the grid-to-cathode capacitance C_{gk} . For the low power types of triode suitable for use in Pierce type oscillators, the grid-cathode capacitance is normally in the range of 2 to 5 PF, and the maximum permissible grid leak resistor value is generally 1 megohm, and occasionally 2 megohms.

The third and most important part of the grid input impedance is reactive if the plate signal is in phase opposition to the grid voltage, but has a resistive component if the voltage phase angle deviates from this value. This behavior of the amplifier is termed the "Miller effect" and can be analyzed with the aid of Figure 9-6. Assuming that the reactance of C_{pg} is large relative to the plate circuit impedance consisting of the parallel combination of the tuning elements, the reflected total oscillator load R_T , and the plate resistance of the tube R_p , the current flowing through C_{pg} is:

$$I_{C_{pg}} = (V_{in} - V_o) \cdot j\omega C_{pg} \quad (9-3)$$

But

$$V_o = G_V \cdot V_{in} \quad (9-4)$$

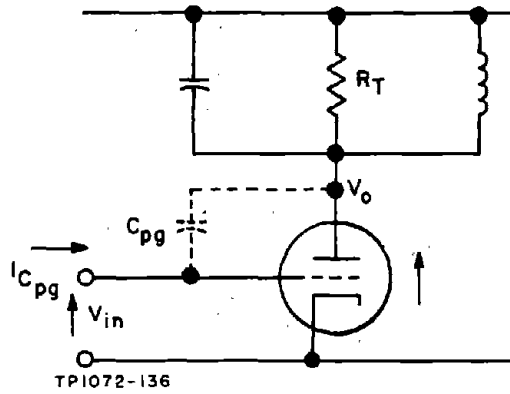


Figure 9-6. Circuit Illustrating Miller Effect

where G_v is the voltage gain from grid to plate.

Therefore:

$$I_{C_{pg}} = V_{in} (1 - G_v) \cdot j\omega C_{pg} \quad (9-5)$$

The input admittance of the amplifier due to feedback is then:

$$Y_M = (1 - G_v) \cdot j\omega C_{pg} \quad (9-6)$$

When the plate voltage is in phase opposition to V_{in} , G_v is a real negative quantity and the amplifier input admittance due to feedback is then:

$$Y_M = (1 + |G_v|) \cdot j\omega C_{pg} \quad (9-7)$$

That is, a capacitance C_M approximately equal to $G_v \cdot C_{pg}$ appears across the amplifier input terminals due to the feedback effect.

If the plate voltage deviates by an angle ϕ from phase opposition to V_{in} , the amplifier input admittance is then:

$$Y_M = [1 + |G_v| (\cos \phi + j \sin \phi)] \cdot j\omega C_{pg} \quad (9-8)$$

Assuming that $G_v \gg 1$ and that ϕ is 10 degrees or less, Equation (9-8) can be approximated as:

$$Y_M \approx |G_v| (1 + j\phi) \cdot j\omega C_{pg} \quad (9-9)$$

where ϕ is in radians.

Equation (9-9) shows that when the plate signal deviates from phase opposition to V_{in} , a parallel input resistive component R_M appears across the amplifier input, in addition to the capacitive component. The value of this resistance is:

$$R_M \approx \frac{1}{\phi |G_V| \cdot \omega C_{pg}} = \frac{X_{C_{pg}}}{\phi |G_V|} \quad (9-10)$$

The relative values of these parallel impedance components can be obtained by noting that X_{CM} , the parallel reactive component, is:

$$X_{CM} \approx \frac{X_{C_{pg}}}{G_V} \quad (9-11)$$

Therefore:

$$\frac{X_{CM}}{R_M} \approx \phi \text{ (radians)} \quad (9-12)$$

Therefore, for plate voltage phase deviation of 6 and 10 degrees, R_M will be approximately $10 X_{CM}$ and $6.5 X_{CM}$, respectively.

The amplifier input impedance therefore consists of four parallel components: C_M , C_{gk} , R_g , and R_M . C_M and C_{gk} form part of the π network terminating capacitance C_s , and R_g and R_M load the π network. These effects are subsequently discussed in detail.

c. Output Impedance

The output impedance of the amplifier as seen by the plate circuit consists of the tube plate resistance R_p in parallel with the grid-plate capacitance C_{pg} , the plate-cathode capacitance C_{pk} , and stray and tube socket capacitance.

9-6. Crystal π Network Characteristics

The crystal π network analysis of Section 1 gives the following relationships between the π network parameters for the specified crystal unit loading conditions.

The voltage attenuation is:

$$A_V = - \frac{X_{C_s}}{K_A \cdot X_{Leff}} \quad (9-13)$$

where

$$K_A = 1 + \frac{R}{X_{CT}} \cdot \frac{R_{e \text{ max}}}{X_{Leff}} \quad (9-14)$$

The value of the isolating resistor R relative to the crystal unit maximum equivalent resistance $R_{e \max}$ is:

$$\frac{R}{R_{e \max}} = \frac{X_{Leff}}{R_{e \max}} \cdot \frac{R}{X_{CT}} - 1 \quad (9-15)$$

X_{CS} , the reactance of the π network capacitor appearing at the amplifier input, is related to the amplifier input resistance by the smaller of the values of the following equations:

$$X_{CS} \leq \frac{R_{in}}{6} \quad (9-16)$$

or

$$X_{CS} \leq \sqrt{0.1 R_{e \max} \cdot R_{in}} \quad (9-17)$$

where R_{in} is the resistance appearing in parallel with the amplifier input terminals. The transition condition from Equation (9-16) to (9-17) is $R_{in} > 3.6 R_{e \max}$. R_{in} can always be made greater than $3.6 R_{e \max}$, and therefore Equation (9-17) is the one to be employed.

The maximum allowable plate signal voltage before crystal unit overdrive occurs is:

$$V_{o \max} \approx 3.8 \frac{X_{Leff}}{R_{e \max}} \sqrt{P_{CMAX} \cdot R_{e \max}} \quad (9-18)$$

The values of K_A , $\frac{R}{R_{e \max}}$, and $\frac{X_{CT}}{R}$ are shown in Figure 9-7 as functions of $\frac{X_{Leff}}{R_{e \max}}$.

9-7. Limiting Design Factors

There are several factors which dictate the usable range of π network impedance ratios. Of major importance are the conditions imposed by the requirement that the oscillator frequency tolerance should not be significantly larger than the crystal unit tolerance if the circuit is to perform to its best advantage. Another requirement is to ensure that the crystal unit dissipation does not exceed its rating. Conflicting with the latter is the condition that the plate signal voltage will need to be a minimum of, say, 10 V RMS and preferably much larger because of the difficulty of providing amplifier limiting at lower levels. Thirdly, the network component values must be such that its input impedance (which for the given loading conditions lies in the range of R to $1.3 R$ for all values of $X_{Leff}/R_{e \max}$) should provide a suitable load for the tube. If the oscillator external loading is negligible, this simply means that R , which will then essentially constitute the entire amplifier load, should be sufficiently

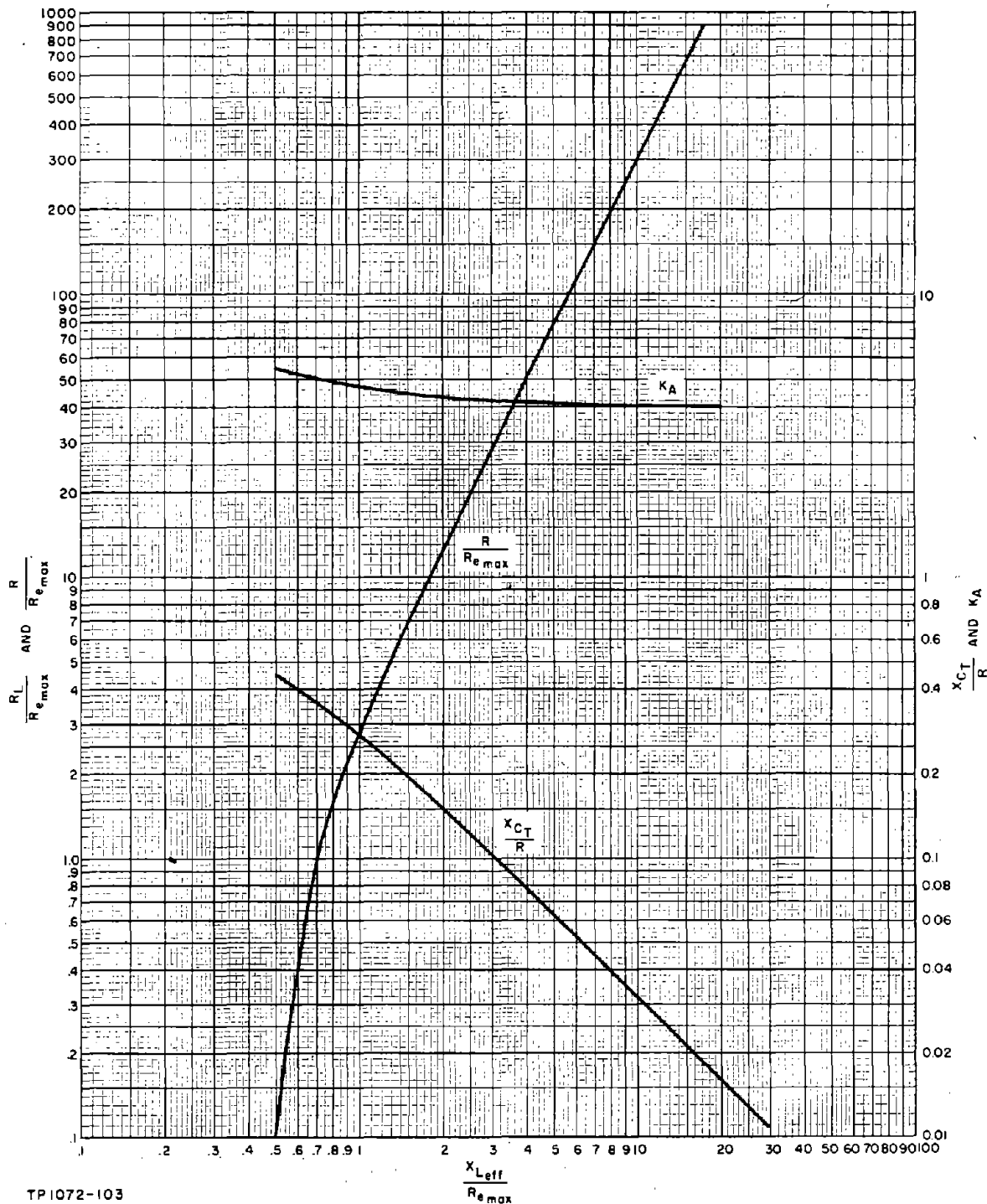


Figure 9-7. K_A , $\frac{R}{R_{e\max}}$, and $\frac{X_{CT}}{R}$ as Functions of $\frac{X_{Leff}}{R_{e\max}}$

large that an adequate loop gain is obtained. If the external oscillator loading is heavy, however, and a large output power relative to the crystal unit dissipation is required, the value of R must be large relative to R_L to provide the necessary degree of power division between load and feedback network.

The limitations imposed on the π network by the restriction of the plate voltage for a worst-case design to 10 V RMS or greater can be determined from Equation (9-18) which can be rearranged as:

$$\frac{X_{Leff}}{R_{e \max}} = \frac{V_{o \max}}{3.8 \sqrt{P_{C\max}} \cdot R_{e \max}} \quad (9-19)$$

Equation (9-18) was derived assuming that the π network drive voltage would remain constant independent of the value of the equivalent resistance of the crystal unit in circuit. This is not the case in practice, for a reduction of R_e results in a decrease in the π network attenuation which causes a larger amplifier drive signal. Due to the non-ideal limiting characteristic of the tube, this in turn causes an increase in the plate signal voltage. For the given loading conditions, a maximum crystal unit dissipation occurs when the crystal equivalent resistance is approximately $1/3 R_{e \max}$ and, consequently, when the plate signal will be larger than for a worst-case design. In addition variations in the limiting characteristics between individual tubes, in oscillator loading, and in power supply voltages may also cause increases in the plate signal voltage. Judging from experimental results, a 50 percent increase due to all causes may occur, and a suitable value of $V_{o \max}$ to use in Equation (9-19) to determine the minimum usable $\frac{X_{Leff}}{R_{e \max}}$ ratio is 15 V RMS, giving:

$$\frac{X_{Leff}}{R_{e \max}} \geq \frac{4}{\sqrt{P_{C\max}} \cdot R_{e \max}} \quad (9-20)$$

Since $R_{e \max}$ and to a lesser extent $P_{C\max}$ are functions of frequency, the usable values of $\frac{X_{Leff}}{R_{e \max}}$ change with the design frequency. For the CR-18A/U crystal unit, which is reasonably representative of other types, the minimum usable values of $\frac{X_{Leff}}{R_{e \max}}$ at various frequencies are as indicated in Table

9-4. Comparison of these values with the plot of $\frac{X_e}{R_{e \max}}$ given in Figure 9-4 shows that over the greater part of the frequency range the latter values are considerably larger and allow considerable choice in the selection of the value of $\frac{X_{Leff}}{R_{e \max}}$. At 20 MC, however, the two ratios are equal, resulting in an impractical condition. It is then necessary either to use another means of limiting such as a diode to attempt to obtain tube limiting below 10 V signal level or resort to a modified approach, which will subsequently be described, to arrive at a feasible design.

TABLE 9-4. MINIMUM RATIOS OF $\frac{X_{Leff}}{R_{e \max}}$ PERMITTED IN π NETWORK

Drive Voltage Considerations For CR-18A/U Assuming a 10 VRMS Plate Signal for a Worst-Case Design			
Frequency (MC)	$R_{e \max}$ (ohms)	$P_{C\text{MAX}}$ (MW)	Minimum $\frac{X_{Leff}}{R_{e \max}}$
0.8	625	10	1.6
1	575	10	1.7
3	150	10	2.1
4+ to 5 MC	60	10	3.3
7+ to 10 MC	24	10	8.2
10+ to 15 MC	22	5	12
15+ to 20 MC	20	5	12.6

9-8. Relationship Between Oscillator Frequency Mismatch and R_e

Once the oscillator is placed in service it is desirable that its frequency should stay within its tolerance over extended periods of time without the need for adjustments. The continuous drift of crystal unit frequency with aging will cause the oscillator frequency to change over a period of time, and this cannot be counteracted. However, changes in the crystal unit equivalent resistance with time can also introduce an appreciable additional oscillator frequency change which can be minimized if suitable precautions are taken in the design.

It is also desirable in many instances that, once the oscillator is initially aligned, the two most likely components to fail (the crystal unit and the tube) should be capable of replacement without having to retune the oscillator to frequency, and with a negligible resultant mismatch of oscillator and crystal unit frequencies.

Of these two requirements, the latter is the most demanding, and an oscillator fulfilling these conditions will adequately satisfy the former. The characteristics of tubes and crystal units are such that the fulfillment of these requirements is practicable and this is therefore adopted as a design goal.

An insight into what is entailed in stabilizing the oscillator frequency against the change of these components can be obtained from consideration of the phase angle requirements of the π network. The condition required for the π network to give a 180-degree phase shift from input to output is given in Section 1 as:

$$R (X_e - X_{C_L} - X_{C_S} - X_{C_T}) = R_e \cdot X_{C_T} \quad (9-21)$$

This expression can be rearranged as:

$$X_e = X_{C_L} + X_{C_S} + \left(1 + \frac{R_e}{R}\right) X_{C_T} \quad (9-22)$$

R , X_{C_L} , and X_{C_T} consist wholly of physical components and can therefore be made as stable in value as required, but R_e and that part of X_{C_S} contributed by the amplifier are variable with crystal unit and tube changes and can consequently change the value of the right-hand side of Equation (9-22). To maintain oscillation, this will then require a similar change of X_e which can only occur if the frequency of oscillation changes. Reference to Table 9-3 shows that over most of the frequency range the effect of a 1 percent change in C_L (and hence X_e) causes a frequency change of approximately 3 PPM. It is therefore desirable that the variation of C_S and R_e should not, at the most, result in a total change of X_e of more than, say, 4 percent if the increase in overall oscillator tolerance due to this cause is to be comparatively small.

To determine what is involved in meeting this requirement, it is necessary to consider the worst possible effects on the circuit of changing a crystal unit or a tube. If crystal units ranging over the extremes of characteristics are inserted in the circuit, the crystal equivalent resistance may possibly vary over a 9-to-1 range. One effect of this will be to vary the attenuation of the π network which will then cause a compensating change of the amplifier voltage gain in order to maintain unity loop gain. This, in turn, will cause a change in the Miller effect input capacitance of the amplifier and, consequently, in C_S . The change in the π network attenuation between extreme values of R_e will be from 2 to 3 times, and C_M will vary accordingly by a similar amount.

The effect of the variation of C_M on oscillator frequency can be studied and an estimate of the possible oscillator frequency shift obtained by assigning values to X_{C_S} relative to X_e and determining the required amplifier gain, assuming X_{C_L} to be zero, $K_A = 4$, and $C_L = 32$ PF. Then, assuming a typical value of C_{pg} of 2 PF and an amplifier voltage gain variation of 3 to 1, approximate values of C_M for the extreme amplifier gain conditions can be calculated. From this, the required change of X_e and the resultant oscillator frequency change can be obtained, assuming a 3 PPM frequency change for a 1 percent change in X_e . The equations used in these calculations are:

$$X_{Leff} = X_e - X_{CS} \quad (9-23)$$

$$C_S = \frac{X_e}{X_{CS}} \cdot X_{CL} \quad (9-24)$$

$$A_V = - \frac{X_{CS}}{K_A \cdot X_{Leff}} = - \frac{X_{CS}}{4 \cdot X_{Leff}} \quad (9-25)$$

$$G'_V = A_V \quad (9-26)$$

where G'_V is the actual amplifier voltage gain under operating conditions when limiting is occurring.

$$C_{M(max)} = G'_V \cdot C_{pg} \quad (9-27)$$

$$C_{M(min)} = \frac{C_{M(max)}}{3} \quad (9-28)$$

These calculations are given in tabular form in Table 9-5 (a) and show that for the assumed conditions, the variations of X_e to be expected range from 4.5 percent for $X_{CS} = 0.5 X_e$ and $G'_V = 4$, to 1.8 percent for $X_{CS} = 0.1 X_e$ and $G'_V = 36$, corresponding to oscillator frequency changes of perhaps 14 and 5 PPM, respectively.

The set of values for X_{CS} equal to $0.1 X_e$ are close to the practical minimum obtainable since an operating amplifier voltage gain of 36 corresponds to a required small signal gain of about 50. This approaches the maximum gain obtainable, disregarding all other requirements. Other aspects which reduce the voltage gain of the amplifier have to be considered, and the values for $X_{CS} = 0.2 X_e$, $G'_V = 16$, where the frequency change is approximately 9 PPM, are therefore more representative of what can be achieved in practice with this configuration.

An improvement in the constancy of X_{CS} together with a beneficial reduction in the required amplifier voltage gain can be obtained by introducing the term X_{C_e} . This is shown in Table 9-5 (b) where calculations similar to those given in Table 9-5 (a) but introducing values of X_{C_e} are presented. These show that the required voltage gain is then markedly reduced while the changes in X_e caused by variations of X_{CM} are, in the majority of cases, decreased by an order of magnitude or more.

TABLE 9-5. CALCULATION OF OSCILLATOR FREQUENCY SHIFT DUE TO MILLER CAPACITANCE CHANGE

Assumptions: $K_A = 4 \left(\frac{X_{Leff}}{R_{e\max}} > 3 \right)$, $X_{C_L} = 0$, $C_L = 32 \text{ PF}$, $C_{pg} = 2 \text{ PF}$, $\Delta G'_V = 3$, and $\Delta f \text{ (PPM)} = 300 \frac{\Delta X_e}{X_e}$											
(a)											
X_{CS}	X_{C_L}	X_{Leff}	C_S (PF)	G'_V $\left(\frac{1}{AV} \right)$	C_M (PF)		ΔC_S (PF)	$C_S - \Delta C_S$ (PF)	$X_{CS} + \Delta X_{CS}$	ΔX_{CS} (ΔX_e)	Δf (PPM)
					max	min					
0.5 X_e	0	0.5 X_e	64	4	8	2.7	5.3	58.7	0.545 X_e	0.045 X_e	14
0.33 X_e	0	0.67 X_e	96	8	16	5.3	10.7	85.3	0.372 X_e	0.042 X_e	13
0.25 X_e	0	0.75 X_e	128	12	24	8	16	112	0.286 X_e	0.036 X_e	11
0.2 X_e	0	0.8 X_e	160	16	32	10.7	21.3	138.7	0.231 X_e	0.031 X_e	9
0.1 X_e	0	0.9 X_e	320	36	72	24	48	272	0.118 X_e	0.018 X_e	5
(b)											
0.33 X_e	0.34 X_e	0.33 X_e	96	4	8	2.7	5.3	90.7	0.35 X_e	0.02 X_e	6
0.33 X_e	0.56 X_e	0.11 X_e	96	1.33	2.66	0.89	1.77	94.2	0.336 X_e	0.006 X_e	2
0.25 X_e	0.5 X_e	0.25 X_e	128	4	8	2.7	5.3	122.7	0.261 X_e	0.011 X_e	3
0.25 X_e	0.65 X_e	0.1 X_e	128	1.6	3.2	1.1	2.1	126	0.254 X_e	0.004 X_e	1
0.2 X_e	0.4 X_e	0.4 X_e	160	8	16	5.3	10.7	149	0.214 X_e	0.014 X_e	4
0.2 X_e	0.6 X_e	0.2 X_e	160	4	8	2.7	5.3	155	0.207 X_e	0.007 X_e	2
0.1 X_e	0.5 X_e	0.4 X_e	320	16	32	10.7	21.3	299	0.107 X_e	0.007 X_e	2
0.1 X_e	0.8 X_e	0.1 X_e	320	4	8	2.7	5.3	315	0.102 X_e	0.002 X_e	1

The variations of R_e will also cause changes in the term $\left(1 + \frac{R_e}{R}\right)$, giving rise to a further variation in the right-hand side of Equation (9-22). The extent of this effect can be determined from the plot of $\frac{R}{R_{e \max}}$ given in Figure 9-7.

This plot shows that $\frac{R_{e \max}}{R}$ has values of 0.13, 0.07, 0.02, and 0.009 for $\frac{X_{Leff}}{R_{e \max}}$ ratios of 1.6, 2, 4, and 6, respectively; and since R_e is assumed to vary over a 9-to-1 range, these values are indicative of the total fractional change in the term $\left(1 + \frac{R_e}{R}\right)$ that will occur. X_{CT} can therefore be regarded as being changed by these amounts which, as shown, can be appreciable at low values of $\frac{X_{Leff}}{R_{e \max}}$. Reference to Equation (9-22) and the quoted values of $\frac{R_{e \max}}{R}$ shows that for $\frac{X_{Leff}}{R_{e \max}}$ ratios greater than 1.6, the range of values of the effective values of X_{CT} is:

$$X_{Leff} < \left(1 + \frac{R_e}{R}\right) X_{CT} \leq 1.13 X_{Leff} \quad (9-29)$$

where

$$X_{Leff} = X_e - X_{C_e} - X_{C_S} \quad (9-30)$$

The value of $\left(1 + \frac{R_e}{R}\right) X_{CT}$ approaches X_{Leff} as the term $\frac{R_e}{R}$ decreases with increasing values of $\frac{X_{Leff}}{R_{e \max}}$.

Therefore, the effect on the oscillator frequency of the changes in effective X_{CT} caused by variations in R_e is a function of the relative values of X_{Leff} and X_e as well as a function of X_{Leff} relative to $R_{e \max}$. For example, using values that can be attained in practice, if $X_{Leff} = 0.1 X_e$ and $\frac{X_{Leff}}{R_{e \max}} = 1.6$, the approximate effective change in X_{CT} and the required change in X_e are 13 percent and 1.3 percent, respectively. Alternatively, if $X_{Leff} = 0.5 X_e$ and $\frac{X_{Leff}}{R_{e \max}} = 6$, the effective change in X_{CT} is 0.9 percent and the required change in X_e is 0.45 percent. This effect is therefore relatively small in the majority of cases relative to that caused by the variation of C_M .

The effect of changing tubes is not likely to be as severe as that of changing crystal units. Differences of the grid-plate capacitance will cause relatively minor variations of C_M , and differences of the tube plate capacitance may cause changes in the amplifier phase angle which will also require the oscillator frequency to change. This can be minimized, however, by making the

plate circuit tuning capacitance large relative to the tube capacitance, and by ensuring that the Q of the circuit is low. Except for these precautions, therefore, the effect of tube variations need not be considered.

The sense of the miscorrelation errors can be determined in the following way. A decrease in R_e causes an increase in X_{C_S} and a resultant increase in X_e and oscillator frequency. It also causes a decrease in the term $\left(1 + \frac{R_e}{R}\right)$, causing a decrease in X_e and oscillator frequency. The two effects therefore act in opposition, and some degree of cancellation can be expected if the two effects are of comparable magnitude.

9-9. Effect of Amplifier Phase Angle on Oscillator Frequency Miscorrelation

Another possible cause of oscillator frequency miscorrelation is a shift of the amplifier phase angle. Any change in the amplifier phase angle will require a complementary change of the π network phase angle to maintain a zero loop phase angle. This can only occur if the effective inductance of the crystal unit changes which, in turn, necessitates a change of oscillator frequency.

In a triode amplifier the only likely cause of an appreciable change in the phase angle will be the variation of the LC product of the plate tank circuit as a function of temperature. Any drift in the LC product will cause the tank circuit to resonate at a frequency higher or lower than the crystal unit frequency, and consequently it will introduce either a phase lead or lag at the oscillator frequency. The magnitude of the phase shift is also a function of the loaded Q of the tank circuit, a low Q circuit causing a smaller phase shift for a given change in the LC product than would a higher Q circuit.

The relationship between the oscillator miscorrelation and amplifier phase angle can be approximately determined from the operating characteristics of the π network, and the results can then be used to obtain desirable tank circuit Q values.

Equation (1-85) can be rewritten as follows for phase angles of 10 degrees or less, assigning to R_e its maximum value:

$$\phi \approx \frac{\frac{X_{Leff} - X_{CT}}{R_{e \max}} - \frac{X_{CT}}{R}}{1 + \frac{X_{CT}}{R} \cdot \frac{X_{Leff}}{R_{e \max}}} \quad (9-31)$$

where ϕ is in radians.

Reference to column 2 of Table 1-7 shows that the term $\frac{X_{CT}}{R} \cdot \frac{X_{Leff}}{R_{e \max}}$ in the denominator of Equation (9-31) is always less than 0.33 for all values of $\frac{X_{Leff}}{R_{e \max}}$, and therefore the π network phase angle expression can be crudely approximated as:

$$\phi \approx \frac{X_{Leff}}{R_{e \max}} - \frac{X_{CT}}{R_{e \max}} - \frac{X_{CT}}{R} \quad (9-32)$$

The value of $\frac{X_{CT}}{R_{e \max}}$ is obtained by setting ϕ equal to 0, giving:

$$\frac{X_{CT}}{R_{e \max}} = \frac{X_{Leff}}{R_{e \max}} - \frac{X_{CT}}{R} \quad (9-33)$$

These are the π network parameter relationships when the amplifier phase shift is 180 degrees. Referring to Equation (9-32), if an amplifier phase change occurs, the only quantity on the right-hand side of this expression that can change to satisfy the equation is X_{Leff} . Denoting the new value as $(1 + \Delta) X_{Leff}$, the fractional change in X_{Leff} is then:

$$\frac{\Delta X_{Leff}}{X_{Leff}} = \frac{\phi}{\frac{X_{CT}}{R} + \frac{X_{CT}}{R_{e \max}}} \quad (9-34)$$

But

$$\frac{\Delta X_e}{\Delta X_{Leff}} = \frac{X_{Leff}}{X_e} \quad (9-35)$$

Therefore:

$$\begin{aligned} \frac{\Delta X_e}{X_e} &\approx \phi \cdot \left(\frac{X_{Leff}}{X_e} \right)^2 \cdot \frac{1}{\frac{X_{CT}}{R} + \frac{X_{CT}}{R_{e \max}}} \\ &= \phi \cdot \frac{X_{Leff}}{X_e} \cdot \frac{R_{e \max}}{X_e} \end{aligned} \quad (9-36)$$

The fractional change in X_e for a given phase angle is, therefore, directly proportional to $\frac{X_{Leff}}{X_e}$, and the smaller the value of X_{Leff} is relative to X_e , the smaller will be the resulting oscillator frequency change due to a change in the loop phase shift.

The extent of the effect on oscillator miscorrelation can be judged from Table 9-6 which gives values of $\frac{\Delta X_e}{X_e}$ calculated from Equation (9-36) for a 10-degree amplifier phase change and the resulting estimated oscillator frequency change. It appears from these values that the amplifier phase change should be limited to 10 or 15 degrees if the oscillator frequency miscorrelation due to this cause is to be kept within reasonable bounds.

TABLE 9-6. OSCILLATOR MISCORRELATION CAUSED BY A 10-DEGREE AMPLIFIER PHASE CHANGE

$\phi = 0.17$ radian (approximately 10 degrees)			
$\frac{X_{Leff}}{X_e}$	$\frac{X_e}{R_{e \max}}$	$\frac{\Delta X_e}{X_e}$ (%)	Δf (PPM)
0.9	20	0.76	2
0.9	10	1.5	5
0.8	20	0.68	2
0.8	10	1.4	4
0.6	12	0.51	2
0.6	6	1.0	3
0.4	10	0.7	2
0.4	5	1.4	4
0.2	4	0.85	2
0.2	2	1.7	5
0.1	2	0.85	2

9-10. Maximum Plate Circuit Q

The plate circuit of the tube can be regarded as a parallel combination of R_T and R_p and the tuning reactances L and C . The admittance of this network

is therefore:

$$\begin{aligned} Y &= \frac{R_T + R_p}{R_T \cdot R_p} + j \left(\omega C - \frac{1}{\omega L} \right) \\ &= \frac{R_T + R_p}{R_T \cdot R_p} + j \omega C \left[1 - \left(\frac{\omega_0}{\omega} \right)^2 \right] \end{aligned} \quad (9-37)$$

where ω is the oscillator frequency and:

$$\omega_0^2 = \frac{1}{LC} \quad (9-38)$$

Therefore, for small phase angles:

$$\begin{aligned} \phi &\approx \frac{R_T \cdot R_p}{R_T + R_p} \cdot \omega C \left[1 - \left(\frac{\omega_0}{\omega} \right)^2 \right] \\ &= Q_L \left[1 - \left(\frac{\omega_0}{\omega} \right)^2 \right] \end{aligned} \quad (9-39)$$

where Q_L is the tank circuit loaded Q .

When ferrite cores are used in inductors, it is difficult to obtain an LC product stability of better than 250 PPM per degree C unless temperature compensation is employed. Over the temperature range of -55°C to $+105^\circ\text{C}$ this constitutes about a ± 2 percent change in LC and a ± 1 percent change in resonant frequency. Introducing this variation of ω_0 into Equation (9-39) together with $\phi = 10$ degrees and transposing gives the maximum value of Q_L as:

$$\text{Maximum } Q_L = 17 \quad (9-40)$$

That is, the plate circuit Q should not be greater than 17 if the oscillator mis-correlation error is not to increase unduly due to temperature effects in the plate tank circuit. This is close to the upper limit if compensation techniques are not to be used, and a preferable value would be, say, 10. This would then make the selection of the tuning elements uncritical.

Operation of the tank circuit under low Q conditions often requires that the tuning capacitance be relatively small. If it is made too small, however, the variations of output capacitance between tubes will introduce a mis-correlation error. A total tuning capacitance of around 15 to 20 PF appears sufficient to swamp these variations adequately and can be considered as a suitable minimum value.

9-11. Relationship Between C_S and the Amplifier Input Impedance

The effect of the Miller capacitance C_M on the value of C_S has been previously discussed in detail, and attention is confined here to the relationship between X_{CS} , R_g , and R_M . From Equation (9-17) the value of amplifier input resistance that will cause negligible crystal unit loading is:

$$R_{in} \geq \frac{10 X_{CS}^2}{R_{e \max}} \quad (9-41)$$

where R_{in} is the parallel combination of R_g and R_M .

That part of R_{in} contributed by the grid leak resistor can always be made sufficiently large to have a negligible effect by assigning to R_g a value of, say:

$$R_g \geq \frac{30 X_{CS}^2}{R_{e \max}} \quad (9-42)$$

This component can then be ignored, and the condition placed on R_M is that:

$$R_M \geq \frac{10 X_{CS}^2}{R_{e \max}} \quad (9-43)$$

Or, substituting for R_M into Equation (9-12), the allowable amplifier phase angle is:

$$\phi \leq \frac{X_{CM} \cdot R_{e \max}}{10 X_{CS}^2} \quad (9-44)$$

For the majority of designs the allowable amplifier phase angle dictated by oscillator miscorrelation will be smaller than the value given by Equation (9-44). In some cases, however, this may not be the case, and the plate circuit loaded Q will then need to be reduced accordingly to meet this requirement if the crystal unit loading due to R_M is to be negligible.

9-12. BASIC DESIGN APPROACH

Reference to the fourth line of Table 9-5 (a) shows that for $X_{CS} = 0.2 X_e$ and $C_{pg} = 2$ PF, G_V is 16 and the expected change of frequency due to changes of C_S is approximately 10 PPM. This is indicative of the total frequency shift expected, since for these conditions $\frac{X_{Leff}}{R_{e \max}}$ is always greater than 6 and the change in the term $\left(1 + \frac{R_e}{R}\right) \times X_{CT}$ will be 1 percent or less. For any practical

value of X_{CT} , therefore, the resultant frequency change will be less than 3 PPM and, because this change is in the opposite sense to that caused by changes in C_S , it will tend to reduce rather than increase the frequency shift.

This expected total frequency miscorrelation of approximately 10 PPM is confirmed by experimental results obtained for oscillators operating under these conditions, which show miscorrelations of from 4 to 7 PPM for a 3-to-1 range of values of R_e . This can be expected to double for the assumed 9-to-1 range of R_e .

For these conditions the required closed loop amplifier voltage gain is 16, requiring a small signal amplifier gain of 20 or more to ensure oscillation. This is within the capabilities of the high μ , low R_p tubes, and this set of oscillator relationships is therefore practicable.

In many applications an overall oscillator frequency tolerance of ± 60 PPM will be adequate, and this will be possible in a circuit having the relationships given in the fourth line of Table 9-5 (a), using a crystal unit with a ± 50 PPM overall frequency tolerance. This approach results in a simple design procedure which is applicable at all frequencies of the range, except possibly at the very highest frequencies where the limitations placed on the amplifier plate signal voltage may cause difficulties.

If the required overall oscillator frequency tolerance lies between ± 35 and ± 50 PPM, this can be obtained with the basic approach at frequencies above 3 MC using the ± 25 PPM tolerance CR-66/U or CR-69/U crystal units. But if a smaller tolerance approaching more closely that of the crystal unit is required, it will be necessary to introduce the series capacitor C_e into the design. The design procedure is then complicated by the addition of another variable, and this can probably best be treated as a modification of the basic approach; the basic design first being determined to serve as a starting point, followed by a modifying process to introduce the component changes necessary to reduce the frequency miscorrelation. This is the approach subsequently adopted. This is also the approach to be adopted below 10 MC if for some reason an intermediate μ triode is preferred for the design. In this case C_e is used in order to reduce the π network attenuation to a value compatible with the available amplifier voltage gain.

9-13. BASIC DESIGN PROCEDURE

Step 1

Select the crystal unit type on the basis of its overall frequency tolerance, noting that the overall oscillator tolerance can be expected to be from, say, ± 3 PPM to ± 10 PPM larger depending on the sophistication of the final design.

Tabulate the values of $R_{e \max}$, $P_{C \max}$, and C_L , and calculate:

$$X_e (= X_{C_L})$$

$$\frac{X_e}{R_{e \max}}$$

Step 2

The values of X_{C_S} and X_{C_L} are selected as $0.2 X_e$ ($C_S = 160$ PF) and 0, respectively. If a closer oscillator frequency tolerance than the selected crystal unit tolerance ± 10 PPM is necessary or an intermediate μ tube is to be used, this will only be a preliminary selection. Calculate:

$$X_{Leff} = X_e - X_{C_S} = 0.8 X_e \quad (9-45)$$

$$\frac{X_{Leff}}{R_{e \max}} = \frac{0.8 X_e}{R_{e \max}} \quad (9-46)$$

The allowable plate signal voltage for a worst-case design is:

$$V_o'_{\max} = 2.5 \frac{X_{Leff}}{R_{e \max}} \sqrt{P_{C \max} \cdot R_{e \max}} \quad (9-47)$$

$$R = 3 \frac{X_{Leff}^2}{R_{e \max}} \quad (9-48)$$

(R can also be obtained from the curve of $\frac{R}{R_{e \max}}$ plotted in Figure 9-7 at the appropriate value of $\frac{X_{Leff}}{R_{e \max}}$.)

The π network input resistance will be:

$$R_{FB} = 1.33 R \quad (9-49)$$

$$X_{C_T} = X_{Leff} / \left(1 + \frac{R_{e \max}}{R}\right) \quad (9-50)$$

(X_{C_T} will be within 1 percent of X_{Leff} , and therefore C_T will be approximately 40 PF.)

Step 3

Select a triode on the following basis:

- (a) The μ of the tube should preferably be at least 50.
- (b) In general, in order that the amplifier will be capable of driving the feedback network and a reasonable external load, the plate resistance at the chosen operating point should be less than 30 K for design frequencies of 2 MC or less, 20 K or less at design frequencies between 2 and 5 MC, 15 K or less from 5 to 10 MC, and less than 10 K above 10 MC. The quoted values are based on the load presented by the feedback network to the amplifier. If high power output is required, lower values of plate resistance will probably be needed.
- (c) The grid-plate capacitance should be as small as possible. This procedure is based on a maximum C_{pg} (including strays) of 2 PF. The use of a tube with a larger C_{pg} will probably result in a wider overall oscillator frequency tolerance.

At frequencies below 10 MC a large number of tube types are suitable since the requirements placed on the tube are not stringent. The allowable plate signal voltage is then sufficiently large that the triode DC plate and grid bias voltage can be selected to optimize the plate resistance and amplifier gain, and it is a relatively easy matter to meet the amplifier requirements. Above 10 MC, however, the allowable plate signal voltage decreases rapidly, and it becomes increasingly difficult to obtain sufficient limiting action. This entails operating the tube at low DC plate voltage which tends to increase the plate resistance, making it then more difficult to obtain the required amplifier gain, particularly since the feedback network input resistance is relatively small at these frequencies. Above 10 MC it is therefore necessary that the plate resistance be small, and this severely restricts the number of tube types available for selection. It is possible to gain relief in this respect at the expense of a larger oscillator miscorrelation by increasing R and X_{CS} , thereby allowing higher R_p tubes to be employed. This is treated in Paragraph 9-19.

Table 9-7 gives a listing of triode types and their typical characteristics to illustrate the range of characteristics available.

Step 4

From the tube characteristic curves given in the data sheet, determine a suitable working point and the total plate load R_T which will result in an amplifier small signal voltage gain of from 20 to 24, using the formula:

$$G_V = \frac{\mu R_T}{R_T + R_p}$$

(9-51)

Several possible plate voltage and grid bias points will probably have to be investigated before a suitable operating point is found.

TABLE 9-7
TYPICAL TRIODE CHARACTERISTICS

TUBE TYPE	U	R _p (K)	I _p (MA)	V _P	C _{gp} (PF)
<u>Sub-Miniature</u>					
5977	16	3.6	10	100	1.3
*6111	20	4	8.5	100	1.5
*5798	24	7	2	30	1.7
5718	27	4.7	9	100	1.3
5635	38	10	5	100	1.2
6169	55	8.5	11	180	1.6
6112	70	28	2	150	1
<u>Miniature</u>					
6072	16	10	4	140	1.5
*5687	17	2	23	180	4
6135 (6C4)	17	8	11	250	1.4
6350	18	4	11	150	3.2
*5963	21	7	9	70	1.5
5844	28	8	5	100	2.7
*5964	39	7	9.5	100	1.3
*5965	47	7	9	150	3
6193	55	8.5	12	180	1.5
6201					
(12AT7)	60	14	3	100	1.6
6CW4	60	6	8	110	0.9
6ES4	57	9	5	150	0.4
5751					
(12AX7)	70	58	0.8	100	1.4
*Dual Triodes					

The worst-case design plate voltage swing, and hence the tube operating point, can be estimated with reasonable accuracy from a load line with a slope of $-R_T$ drawn on the plate characteristic of the tube if the plate voltage negative peak swing is more than, say, 20 volts. The expected peak negative voltage swing is then the voltage difference between the quiescent plate bias point and the intersection of the load line, with the plate characteristic curve for V_G equal to 0.

The positive plate voltage swing will be of similar amplitude due to the action of the plate tank circuit and, since the limiting is only slight in a worst-case design, the plate RMS voltage is approximately 0.7 times the negative peak swing. When designing for lower plate signal voltages, the accuracy with which the plate voltage swing can be estimated decreases rapidly. The tube operating conditions determined as described above should then only be regarded as an approximate indication of where the tube should be operated. In all probability it will then be necessary to experimentally adjust the tube bias conditions to obtain the required plate signal voltage.

At design frequencies above 10 MC it will probably be necessary to confine attention to the region of plate voltages of 70 to 120 VDC and grid bias voltages in the vicinity of -1 VDC, the former being dictated by the signal limiting requirements and the latter by the need to minimize R_p in order to obtain the required gain.

The value of R_T must, of course, be smaller than R_{FB} for a feasible design and should be much smaller if high oscillator power output is desired. The value of the external oscillator load resistance reflected into the plate circuit is:

$$R_L = \frac{R_T \cdot R_{FB}}{R_{FB} - R_T} \quad (9-52)$$

The estimated oscillator power output is then:

$$P_L = \frac{V_o^2}{R_L} \quad (9-53)$$

Step 5

The remaining amplifier component values are calculated as follows:

The minimum grid leak resistor value is:

$$\text{Minimum } R_g = \frac{10 X_{CS}^2}{R_{e \max}} \quad (9-54)$$

Larger values of R_g are permissible, and varying R_g is a convenient method of adjusting the plate signal voltage amplitude when this is critical. Increasing R_g tends to decrease the plate signal voltage amplitude.

The allowable maximum amplifier phase angle before R_M significantly loads the crystal unit can be rearranged for the basic approach by substituting for the relative values of C_M , C_S , and C_L as:

$$\phi \leq \frac{5}{C_{pg}} \cdot \frac{R_{e \max}}{X_e} \quad (9-55)$$

where C_{pg} is in picofarads.

The minimum value of $\frac{R_{e \max}}{X_e}$ will be 0.125 and therefore for C_{pg} values of 2 PF or less, the allowable plate phase angle is:

$$\phi \leq 0.31 \text{ radian}$$

This is much larger than the value of ϕ dictated by oscillator frequency miscorrelation effects, and therefore the loading due to R_M will be negligible. For the modified design approach described in Paragraph 9-14 this may not be the case if X_{CS} is reduced significantly.

The cathode biasing resistor value is obtained from:

$$R_K = \frac{V_G}{I_p} \quad (9-56)$$

This is the maximum value of R_K , and smaller values are permissible if increased amplifier voltage is found to be necessary during the design evaluation. The minimum value of R_K is determined by considerations of the tube dissipation. It is desirable that the tube should not be damaged if oscillation ceases due either to a crystal unit failure or to the withdrawal of the crystal unit from the circuit. R_K should, therefore, always be sufficiently large to ensure that neither the maximum plate current nor dissipation ratings are exceeded under quiescent conditions.

The resistance appearing at the cathode of the tube is R_K in parallel with the cathode input resistance of the tube. The value of the latter is:

$$r_K = \frac{R_p + R_T}{\mu + 1} \quad (9-57)$$

The total cathode input resistance is then:

$$r'_K = \frac{r_K \cdot R_K}{r_K + R_K} \quad (9-58)$$

The reactance of the cathode decoupling capacitor should be small compared to R_K to avoid causing a phase shift of the amplifier output voltage relative to $-V_{in}$. This effect will be negligible if the reactance of the decoupling capacitor satisfies the following relationship:

$$X_K \leq \frac{r'_K}{50} \quad (9-59)$$

The value of the capacitor placed in parallel with the amplifier input to give a total C_S equal to 160 PF is approximately:

$$\text{Physical } C_S \approx 160 - (G'_V + 1) C_{pg} - C_{gK} \quad (9-60)$$

where G'_V is equal to A_V .

This calculated value is only approximate, and an adjustment of its value will probably be required during the design evaluation to give correlation of oscillator and crystal unit frequencies.

The plate circuit tuning inductance is calculated by assuming a value for the total tuning capacitance. A value of 10 to 15 PF is a suitable minimum value of tuning capacitance for this calculation. The Q of the inductor should be sufficiently large that the effective parallel resistance of the coil is at least 30 times R_T . If a lower Q coil is used, it will be necessary to correct for this by appropriately increasing R_L to maintain R_T constant at the calculated value. The loaded plate circuit Q should preferably be less than 17 unless either a more stable inductor or temperature compensation is used.

The basic design procedure is now complete. If the assumed oscillator frequency tolerance of ± 10 PPM larger than that of the selected crystal unit type is adequate and the estimated minimum output power is reasonably close to that required, refer to Step 6 which deals with experimental aspects of the design. If these conditions are not adequate, refer to Step 7.

Step 6

Construct a breadboard circuit of the oscillator using the calculated component values.

Determine the equivalent resistance and anti-resonance frequency of several crystal units. This is preferably done using the appropriate crystal impedance meter, but if a CI meter is unobtainable, one of the other methods outlined in Section 1 may be used.

Construct a worst-case crystal unit by adding a resistor in series with one of the crystal units to increase its equivalent resistance to $R_e \text{ max}$.

Insert one of the lower R_e crystal units into the circuit and tune the plate circuit to obtain oscillation.

After obtaining satisfactory oscillation, insert the simulated worst-case unit into the circuit and retune the plate circuit if necessary. If oscillation is not obtained, the amplifier gain is probably inadequate. This can be remedied by decreasing the cathode bias resistor, providing the tube ratings are not exceeded.

When oscillation is established with the worst-case crystal unit, several tubes should be substituted into the amplifier and the plate signal voltages noted. If they are larger than the allowable value previously calculated, it may be possible to reduce the plate voltage to a safe value by increasing the grid bias resistor. If this method is not satisfactory, it will be necessary to re-bias the tube at a lower plate voltage.

When satisfactory limiting is obtained, the oscillator miscorrelation error is dealt with by adjusting the value of C_S . With the plate circuit tuned to resonance, adjustments are made to C_S until the miscorrelation error is reduced to a few parts per million. The other crystal units are then substituted into the circuit and a final adjustment made to C_S to optimize the miscorrelation error for all crystal units.

Step 7

If a lower overall oscillator frequency miscorrelation than that given by the basic design is required, this can be obtained by introducing a capacitor in series with the crystal unit, providing that the allowable plate signal voltage is then still sufficiently large.

Table 9-5(b) gives sets of data for various relative values of X_{C_1} including the predicted frequency shift in parts per million. To design this type of oscillator it will be necessary to perform similar but extended calculations to give the values of R , the predicted frequency change due to the term $(1 + \frac{R_e}{R})$, and the allowable plate signal voltage, to arrive at a suitable set of π network relationships.

Taking the CR-18A/U crystal unit as representative of the other types, reference to Tables 9-4 and 9-5(b) and to Figure 9-4 shows that up to 10 MC there is a wide choice in the selection of the ratio $\frac{X_{Leff}}{R_{e\ max}}$. Above 10 MC, however, the minimum value of $\frac{X_{Leff}}{R_{e\ max}}$ dictated by plate signal voltage considerations approaches $\frac{X_e}{R_{e\ max}}$ and the series capacitor cannot then be used to decrease the frequency miscorrelation except by limiting the plate voltage swing to less than 10 VRMS. It will then probably be necessary to introduce a limiting circuit to prevent crystal overdrive. One circuit which is suitable for this purpose consists of a diode connected as shown in Figure 9-8. The diode is reverse-biased by the voltage drop across the resistor R' and only conducts when the instantaneous signal voltage equals the reverse bias voltage. When conduction occurs, the diode loads the amplifier heavily, stabilizing the signal amplitude. The diode reverse-bias voltage should therefore be approximately equal to the required peak signal voltage.

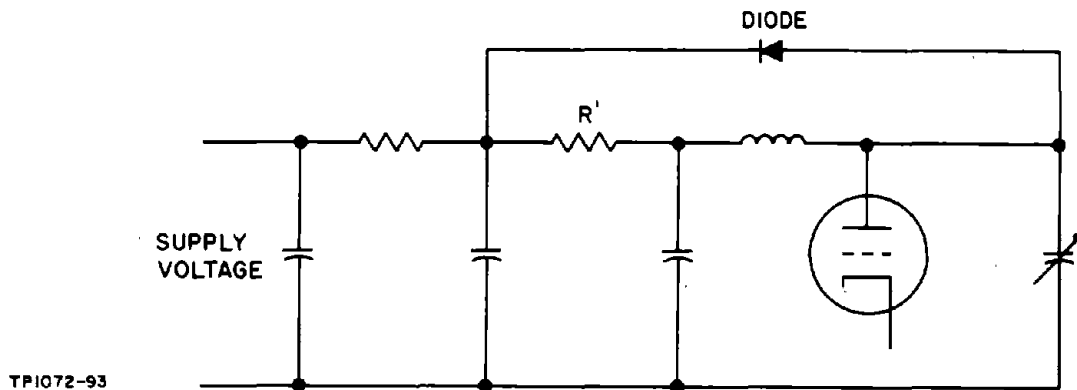


Figure 9-8. Diode Limiter Circuit

Referring to Table 9-5(b) the π network conditions given in the fifth or seventh lines should give acceptable miscorrelation errors when using the lower tolerance crystal units in the mid-range frequencies and also at the higher frequencies if diode limiting is used. The π network conditions given in the fifth line would also be particularly applicable when either a larger oscillator output power is required or if the use of an intermediate μ triode is contemplated, since an amplifier small signal gain of only 11 or 12 is required.

The design procedure is the same as the basic procedure once a selection of π network parameters has been made. The following examples illustrate the process.

9-14. DESIGN CALCULATION EXAMPLES

9-15. 1-MC Design Example (Basic Design Procedure)

Crystal Unit Characteristics, CR-18A/U

$R_{e \max} = 575 \text{ ohms}$	$\frac{X_{Leff}}{R_{e \max}} = 7$
$P_{C\text{MAX}} = 10 \text{ MW}$	$V'_{o \max} = 42 \text{ V RMS}$
$C_L = 32 \text{ PF}$	$R = 84 \text{ K}$
$X_e = 5 \text{ K}$	$R_{FB} = 112 \text{ K}$
$\frac{X_e}{R_{e \max}} = 8.7$	$X_{CT} = 4 \text{ K}$
$X_{Leff} = 4 \text{ K}$	$C_T = 40 \text{ PF}$
$X_{CS} = 1 \text{ K}$	

Tube Characteristics, 12AT7

For $E_p = 200 \text{ VDC}$ and $I_p = 6 \text{ MA}$, $V_G = -2 \text{ VDC}$, $R_p = 14 \text{ K}$, $\mu = 60$. Then for $R_T = 8 \text{ K}$, $G_V = 22$, and the estimated worst-case design plate signal voltage is 37 V RMS . Then, $R_L = 8.6 \text{ K}$, $P_L \approx 160 \text{ MW}$, $R_g \geq 50 \text{ K}$, $R_K = 330 \text{ ohms}$, $r_K = 370 \text{ ohms}$, $r'_K = 170 \text{ ohms}$, $X_K \leq 3.5 \text{ ohms}$, $C_K = 0.1 \text{ UF}$. Physical $C_S \approx 130 \text{ PF}$.

9-16. 5-MC Design Example (Basic Design Procedure)

Crystal Unit Characteristics, CR-18A/U

$R_{e \max} = 60 \text{ ohms}$	$X_{Leff} = 800 \text{ ohms}$
$P_{C\text{MAX}} = 10 \text{ MW}$	$X_{CS} = 1 \text{ K}$
$C_L = 32 \text{ PF}$	$\frac{X_{Leff}}{R_{e \max}} = 13.33$
$X_e = 1 \text{ K}$	$V'_{o \max} = 26 \text{ V RMS}$
$\frac{X_e}{R_{e \max}} = 16.7$	$V_{o \max} = 39 \text{ V RMS}$

Crystal Unit Characteristics, CR-18A/U (Cont)

$$\begin{array}{ll} R = 32 \text{ K} & X_{CT} = 800 \text{ ohms} \\ R_{FB} = 43 \text{ K} & C_T = 40 \text{ PF} \end{array}$$

Tube Characteristics, 12AT7

For $E_p = 150 \text{ VDC}$, $I_p = 4 \text{ MA}$, $V_G = -1.6 \text{ V}$, $\mu = 60$, $R_p = 15 \text{ K}$.
For $R_T = 7.5 \text{ K}$, $G_V = 20$. The estimated worst-case design plate signal voltage is 25 V RMS . $R_L = 9.5 \text{ K}$, $P_L \approx 70 \text{ MW}$, $R_g \geq 24 \text{ K}$, $R_K = 400 \text{ ohms}$.
 $r_K = 370 \text{ ohms}$, $r'_K = 190 \text{ ohms}$, $X_K \leq 4 \text{ ohms}$. $C_K \geq 0.01 \text{ UF}$.

9-17. 20-MC Design Example (Basic Design Procedure)

Crystal Unit Characteristics, CR-18A/U

$$\begin{array}{ll} R_{e \text{ max}} = 20 \text{ ohms} & \frac{X_{Leff}}{R_{e \text{ max}}} = 10 \\ P_{C \text{ MAX}} = 5 \text{ MW} & V'_{o \text{ max}} = 8 \text{ V RMS} \\ C_L = 32 \text{ PF} & R = 6 \text{ K} \\ X_e = 250 \text{ ohms} & R_{FB} = 8 \text{ K} \\ \frac{X_e}{R_{e \text{ max}}} = 12.5 & X_{CT} = 200 \text{ ohms} \\ X_{Leff} = 200 \text{ ohms} & C_T = 40 \text{ PF} \\ X_{CS} = 50 \text{ ohms} & \end{array}$$

Tube Characteristics, 6CW4

For $E_p = 75 \text{ VDC}$ and $I_p = 5 \text{ MA}$, $V_G = -0.7 \text{ VDC}$, $\mu = 60$, $R_p = 7 \text{ K}$.
Then for $R_T = 3.5 \text{ K}$, $G_V = 20$, and the estimated worst-case design plate signal voltage is 13 V RMS . This is larger than $V'_{o \text{ max}}$ and will necessitate bias adjustment to reduce it to the required level. Then, $R_L = 6.2 \text{ K}$. P_L (when V_o reduced to $V'_{o \text{ max}}$) = 10 MW , $R_g \geq 4 \text{ K}$, $R_K = 140 \text{ ohms}$, $r_K = 175 \text{ ohms}$, $r'_K = 80 \text{ ohms}$, $X_K \leq 1.6 \text{ ohms}$, $C_K = 0.01 \text{ UF}$. Physical $C_S \approx 140 \text{ PF}$.

9-18. 5-MC Design Calculation (Low Miscorrelation)

Crystal Unit Characteristics, CR-66/U

$$R_{e \max} = 50$$

$$X_e = 1060 \text{ ohms}$$

$$P_{C\text{MAX}} = 10 \text{ MW}$$

$$\frac{X_e}{R_{e \max}} = 21$$

$$C_L = 30 \text{ PF}$$

π network conditions:

$$X_{L\text{eff}} = 0.4 X_e = 424 \text{ ohms}$$

$$X_{C_L} = 0.5 X_e = 530 \text{ ohms}$$

$$X_{C_S} = 0.1 X_e = 106 \text{ ohms } (C_L = 60 \text{ PF}, C_S = 300 \text{ PF})$$

$$X_{C_T} = 0.4 X_e$$

$$V'_{o \max} = 15 \text{ V RMS}$$

$$C_T = 75 \text{ PF}$$

$$R = 10.7 \text{ K}$$

$$\frac{X_{L\text{eff}}}{R_{e \max}} = 8.4$$

$$R_{FB} = 14 \text{ K}$$

Tube Characteristics, 6CW4

For $E_p = 100 \text{ VDC}$ and $I_p = 8 \text{ MADC}$, $V_G = -0.7 \text{ VDC}$, $R_p = 6 \text{ K}$, $\mu = 65$. $C_{pg} = 1 \text{ PF}$. Then for $R_T = 3.5 \text{ K}$, $G_V = 24$, and the worst-case design plate signal voltage is 14 V RMS . Then $R_L = 4.7 \text{ K}$, $P_L = 42 \text{ MW}$, $R_g \geq 7 \text{ K}$, $R_K = 90 \text{ ohms}$, $r_K = 150 \text{ ohms}$, $r'_K = 56 \text{ ohms}$, $X_K = 1 \text{ ohm}$, $C_K \geq 0.03 \text{ UF}$. Physical $C_S \approx 300 \text{ PF}$.

Estimated Δf due to $C_M \approx 1 \text{ PPM}$

Estimated Δf due to $\frac{R_e}{R} \approx 1 \text{ PPM}$

9-19. A METHOD OF RELAXING AMPLIFIER REQUIREMENTS AT HIGH FREQUENCIES

At the extreme high frequencies of the range only the very low R_p tubes having R_p 's below, say, 8 K are suitable for use in an oscillator designed according to the basic design procedure. Higher R_p tubes, when operated with plate voltages below 100 VDC (which appear necessary to provide the required limiting), are forced to operate under low current and hence high R_p conditions. It is then usually impossible to obtain the required amplifier gain because of the low feedback network input resistance, unless the external oscillator loading is negligible.

If it is desired to use such a tube at these frequencies, it is possible to increase the allowable plate signal voltage by increasing the values of R and X_{CS} calculated in the basic procedure while decreasing X_{Leff} , thereby maintaining the π network constant. The resulting benefits are twofold. The allowable plate signal voltage is increased which, in turn, allows the DC plate voltage and current to be increased, decreasing R_p . The feedback network input resistance is increased, thereby reducing its loading effect. The disadvantage is that the oscillator overall frequency tolerance is increased due to the increase in X_{CS} .

The justification for this approach is as follows: Reference to Equation (1-108) shows that the allowable π network input voltage may be expressed as:

$$V_{omax} = 2\sqrt{R \cdot P_{C_{MAX}}} \quad (9-61)$$

Therefore, an increase in R results in a smaller increase in V_{omax} . Since it is a square root function, the increase in V_{omax} is not large for moderate changes in R . However, even small changes in V_{omax} can be worthwhile for the conditions described.

The new feedback network attenuation expression can be determined by reference to Equations (9-13) and (9-22), and to Figure 9-7. The plot of $\frac{R}{R_{e \max}}$ shows that for all values of $\frac{X_{Leff}}{R_{e \max}}$ larger than 2.5, $\frac{R}{R_{e \max}}$ will be 0.05 or less. From Equation (9-22) it can then be seen that X_{CT} will be within 5 percent of X_{Leff} . Substituting X_{Leff} for X_{CT} in Equation (9-13) and rearranging gives:

$$A_V = -\frac{X_{CS}}{X_{Leff}} \cdot \frac{\frac{X_{Leff}^2}{R_{e \max}}}{\frac{X_{Leff}^2}{R_{e \max}} + R} \quad (9-62)$$

But $\frac{X_{Leff}^2}{R_{e \max}}$ is the input resistance of the π network $R_{\pi \min}$ as viewed across C_T (see Paragraph 1-16) when $\frac{X_{Leff}}{R_{e \max}}$ is 3 or larger.

Therefore:

$$A_V = -\frac{X_{CS}}{X_{Leff}} \cdot \frac{R_{\pi \min}}{R_{\pi \min} + R} \quad (9-63)$$

The π network attenuation calculation can now be conveniently treated in two parts and the effects of changing R readily appreciated.

Equation (9-61) gives the allowable π network input voltage when R_{π} equals R . That is, when R_e is less than $R_{e \max}$ and, consequently, when the loop gain is much greater than 1. Because of the non-ideal limiting action of the tube, it is therefore necessary to introduce a correction factor for a worst-case design. The allowable plate voltage is then:

$$V_{o \max} = 1.4 \sqrt{R \cdot P_{C \max}} \quad (9-64)$$

The remainder of the design process is the same as for the basic design procedure, except that the plate circuit loaded Q may be dictated by the value of R_M . The following examples illustrate this approach.

9-20. DESIGN EXAMPLES USING THE MODIFIED APPROACH

9-21. 20-MC, 12AT7 Oscillator (Modified Approach)

Crystal Unit Characteristics, CR-18A/U

$R_{e \max} = 20 \text{ ohms}$	$C_L = 32 \text{ PF}$
$P_{C \max} = 5 \text{ MW}$	$X_e = 250 \text{ ohms}$
If $X_{Leff} = 150 \text{ ohms}$, then:	
$X_{CS} = 100 \Omega$	$X_{CT} = 150 \text{ ohms}$
$C_S = 80 \text{ PF}$	$C_T = 53 \text{ PF}$
$\frac{X_{Leff}}{R_{e \max}} = 7.5$	$R_{\pi \min} = 1.1 \text{ K}$

Let $R = 10 \text{ K}$, then $A_V = \frac{1}{15}$, $R_{FB} = 11 \text{ K}$, $V'_{o \max} = 10 \text{ V RMS}$.

Tube Characteristics, 12AT7

For $E_p = 100$ VDC and $I_p = 4$ MADC, $V_G = -1$ VDC, $\mu = 60$, $R_p = 15$ K. Then for $R_T = 7.5$ K, $G_V = 20$, and the estimated worst-case design plate signal voltage is 11 V RMS. Then $R_L = 22$ K, $P_L = 4.5$ MW, $R_g \geq 15$ K, $\phi \approx 4$ degrees, $Q_L < 7$, $R_K = 250$ ohms, $r_K = 360$ ohms, $r'_K = 150$ ohms, $X_K \leq 1.5$ ohms, $C_K \geq 0.005$ UF. Physical $C_S \approx 55$ PF.

9-22. 20-MC, 6CW4 Oscillator (Modified Approach)

Crystal Unit Characteristics, CR-18A/U

$$R_{e \max} = 20 \text{ ohms}$$

$$C_L = 32 \text{ PF}$$

$$P_{C\text{MAX}} = 5 \text{ MW}$$

$$X_e = 250 \text{ ohms.}$$

If $X_{Leff} = 150$ ohms, then:

$$X_{C_S} = 100 \text{ ohms}$$

$$X_{C_T} = 150 \text{ ohms}$$

$$C_S = 80 \text{ PF}$$

$$C_T = 53 \text{ PF}$$

$$\frac{X_{Leff}}{R_{e \max}} = 7.5$$

$$R_{\pi \min} = 1.1 \text{ K}$$

Let $R = 10$ K, then: $A_V = \frac{1}{15}$, $R_{FB} = 11$ K, $V'_{o \max} = 10$ V RMS.

Tube Characteristics, 6CW4

For $E_p = 100$ VDC and $I_p = 8$ MA, $V_G = -0.7$ VDC, $R_p = .6$ K, $\mu = 65$. Then for $R_T = 3.5$ K, $G_V = 24$, and the estimated worst-case design plate signal voltage is 14 V RMS. Then $R_L = 5.1$ K, $P_L = 20$ MW, $R_g \geq 15$ K, $\phi = 8$ degrees, $Q_L < 13$, $R_K = 90$ ohms, $r_K = 150$ ohms, $r'_K = 56$ ohms, $X_K = 1$ ohm, $C_K \geq 0.01$ UF. Physical $C_S \approx 60$ PF.

9-23. OSCILLATOR DESIGN EVALUATIONS

The five oscillators for which evaluation data are presented are those designs given as examples of the basic design procedure. The external effects for which data are given are:

- (a) DC supply voltage variation (+15, -20 percent)
- (b) Heater supply voltage variation (± 10 percent)
- (c) Oscillator load changes (± 10 percent)
- (d) Ambient temperature variation (-55 to +105 degrees Centigrade).

The internal effects for which data are given are:

- (e) Crystal interchange
- (f) Tube interchange
- (g) Changes in C_T and C_S , the π network terminating capacitors
- (h) The increment of oscillator instability with temperature due to the oscillator components other than the crystal unit (crystal unit positioned outside of temperature chamber, remainder of oscillator circuit subject to temperature change)

With the exceptions of (e), all test data were obtained using an artificial worst-case crystal unit. A suitable value of resistance was connected in series with a crystal unit to increase the equivalent resistance of the combination to $R_{e \max}$. The characteristics of this worst-case crystal, as measured in a CI meter, are given in the list of crystals contained in each design evaluation. Similarly, with the exception of (f), the test data were obtained using one of the triodes having the lowest gain of the small batches of each type available. All these test results, therefore, are for a combination of a worst-case crystal and an inferior tube and should be indicative of the worst oscillator performance likely to be encountered in practice.

The test frequencies of 1, 5, and 20 MC cover virtually the entire frequency range under investigation and were chosen to show the changing influence of tube and crystal unit characteristics over the range. Oscillator design at 20 MC is particularly emphasized because this is the frequency at which design conditions are most critical, due to the combination of low crystal π network

input impedance and low allowable crystal dissipation. The three 20-MC oscillator design examples are intended to show the relative circuit design requirements when using moderately high and low plate resistance triodes at this frequency and also to show some of the possible compromises in design. The design procedure is such that there should be no difficulty in developing similar designs at frequencies other than those for which test data were obtained.

Fixed capacitors were used in these evaluation oscillators. In practice a small variable capacitor would form part of C_S to facilitate the initial adjustment of the oscillator.

Certain general conclusions can be drawn from the evaluation results:

- (a) The worst characteristics of all the oscillators was the variation of oscillator output power as a function of B^+ supply voltage. This characteristic is very poor, particularly for the 20-MC oscillators. This is due primarily to the low loop gains existing in the evaluation oscillators because of the combination of low triode gain and worst-case crystal units. In the case of the 20-MC oscillators, this is further complicated by the necessity of using low plate voltages to prevent crystal overdrive. In general, with more typical crystal units and tube combinations, the performance can be expected to be considerably better under more typical conditions. But if this characteristic is important, it would be advisable to divorce the limiting action from the tube by using a suitably biased diode to perform this function. Using diode limiting, the resulting oscillator would have considerably more stable power output under all conditions.

At frequencies below 10 MC, the advantages to be gained are not as great, since crystal dissipation does not limit the allowable plate voltage to the same extent. Nevertheless, considerable improvement in power output stability could be expected, particularly if a zener diode plus limiter diode combination is used to determine the limiting voltage level.

- (b) Using appropriately chosen values of crystal π network terminating capacitors, oscillator frequency miscorrelation errors can be expected to be below ± 7 PPM under all conditions of tube and crystal characteristics.
- (c) The effect of the oscillator circuit other than the crystal on the oscillator overall frequency tolerance with temperature change is less than ± 3 PPM for the five oscillators evaluated. This level of

performance was obtained without applying any special precautions with regard to the plate circuit tuning, other than ensuring low loaded Q.

- (d) In view of the frequency errors indicated in (b) and (c), the oscillator overall frequency tolerance is likely to be no more than ± 10 PPM greater than that of the crystal unit.

9-24. 1-MC Triode (12AT7) Isolating Resistor Pierce Oscillator Evaluation Data

This design was performed before the design procedure was finalized, and the value of R employed is larger than that obtained in the design calculation. The value of R used was equal to $4 \frac{X_{Leff}^2}{R_{e \max}}$ (112 K) compared with the $3 \frac{X_{Leff}^2}{R_{e \max}}$ (84 K) given in the design calculation, increasing the required ampli-

fier small signal gain to 28. The tube DC operating conditions were the same, and the increase in gain was obtained by using a total load resistance of 14 K, giving $R_L = 15$ K. All other aspects of the evaluation oscillator are the same as given in the design example, except that the allowable worst-case design plate signal voltage is increased to 47 VRMS due to the increase in R. The evaluation data presented should therefore be indicative of the performance expected of an oscillator constructed according to the design example.

The major difficulty occurring in the design evaluation was due to the poor quality of the available crystals. These all exhibited large variations of R_e when subjected to temperature changes. The effect was so bad when they were used as worst-case units that oscillation ceased due to insufficient loop gain as the temperature was increased or in some cases decreased, depending on which crystal unit was in circuit. Having determined that the effect was not due to the remainder of the oscillator circuit, qualitative temperature tests were run to determine the variation of R_e occurring. These tests showed that the crystal R_e 's were increasing almost 100 percent; that is, approximately 200 to 300 ohms. In the temperature tests, the crystal units were already padded until their effective R_e was 580 ohms ($R_{e \max}$), and this additional increase in crystal R_e therefore represented an increase of approximately 30 percent. This also represented a change in loop gain of at least 30 percent, a sufficient change to cause the oscillation to cease.

The best of the crystals was used to obtain the temperature curves shown in Figure 8-28. Oscillation ceased at approximately $+65^\circ\text{C}$, but the curve shows sufficient agreement with those obtained at other frequencies with crystal units not having the marked variation in R_e with temperature, that it is possible to predict

that, given better crystals, the temperature characteristic of this oscillator will be essentially the same as those shown for the other oscillators evaluated.

The other problem that occurred was due to the characteristics of the poorer tubes of the group available. These operated with DC plate current as low as 3 MA when biased according to calculations based on the manufacturers design curves. R_k was therefore reduced from 330 ohms to 150 ohms to increase the quiescent plate current to approximately 6 MA with the poorer tubes in circuit. This resulted in approximately 9 MA of quiescent plate current with the best tube in circuit. The plate current under oscillating conditions was in the 3 to 6 MA region, depending on the tube and crystal qualities.

CRYSTAL UNITS (CR-18A/U)	PARALLEL RESONANT FREQUENCY (MC)	R_e (ohms)
(1)	1.000003	270
(2) (Unit (1) with 300-ohm series resistor added)	1.000003	580
(3)	0.999999	220
(4)	1.000003	250

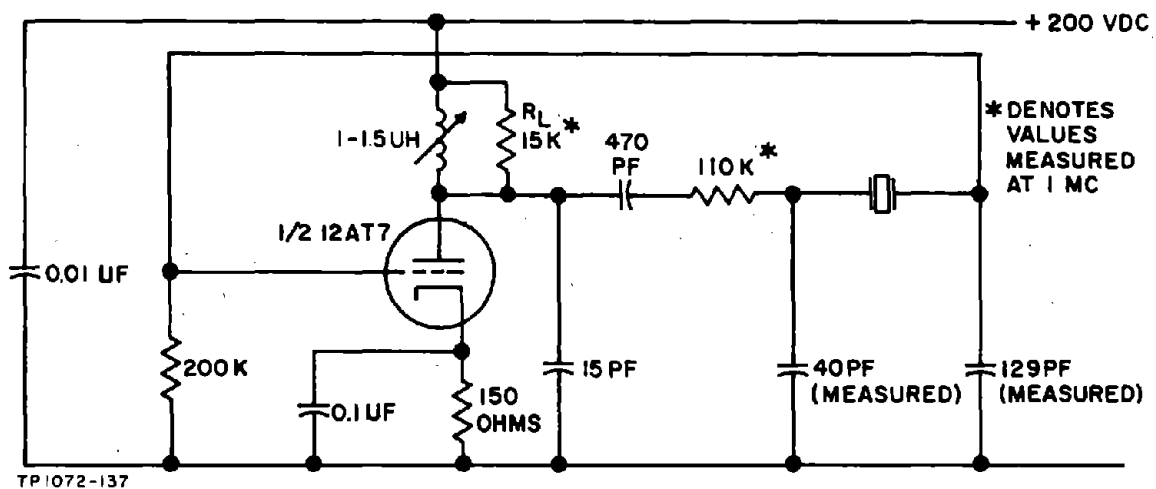


Figure 9-9. 1-MC Triode Pierce Oscillator, Schematic Diagram

Nominal $V_o = 37$ VRMS Nominal Oscillator Frequency = 1.000003 MC

Results Obtained Using Worst-Case Crystal

Effect Of	Change	Test Conditions
+15% B+ Change on Oscillator } Frequency V_o	1 PPM $\Delta V_o = +22\%$	$R_L = 15$ K, $E_f = 6.3$ V
-20% B+ Change on Oscillator } Frequency V_o	1 PPM $\Delta V_o = -35\%$	$R_L = 15$ K, $E_f = 6.3$ V
$\pm 10\%$ Change in E_f on Oscillator } Frequency V_o	± 1 PPM $\Delta V_o = \pm 3\%$	$R_L = 15$ K, $E_{bb} = 200$ V
$\pm 10\%$ Change in R_L on Oscillator } Frequency V_o	± 1 PPM $\Delta V_o = \pm 12\%$	$E_f = 6.3$ V, $E_{bb} = 200$ V
-55°C to $+105^\circ\text{C}$ Change in T_A on Oscillator } Frequency V_o	See Figure 9-10 (Extrapolated as ± 20 PPM)	$E_f = 6.3$ V, $E_{bb} = 200$ V, $R_L = 15$ K
Contribution of Oscil- lator Circuit to Fre- quency Deviation in Temperature Test	See Figure 9-10 (Extrapolated as ± 3 PPM)	

Effect of Tube Changes (Crystal Unit (2))

Tube No.	Oscillator Frequency (MC)	Output Voltage
1	1.000002	37
2	1.000002	33
3	1.000002	40
4	1.000002	38
5	1.000001	42
6	1.000001	38
7	1.000001	42
8	1.000002	39

Effect of Crystal Changes (Tube No. 1)

Crystal No.	Crystal Frequency (MC)	Oscillator Frequency (MC)	Error (PPM)	Output Voltage
1	1.000003	1.000006	+3	52
2	1.000003	1.000002	-1	37
3	0.999999	1.000004	+5	52
4	1.000003	1.000004	+1	52

Effect of C_T and C_S Variations

Increasing C_S by 1 PF results in a frequency change of 2 PPM.

Increasing C_T by 1 PF results in a frequency change of 4 PPM.

Power Output Range

90 to 180 MW

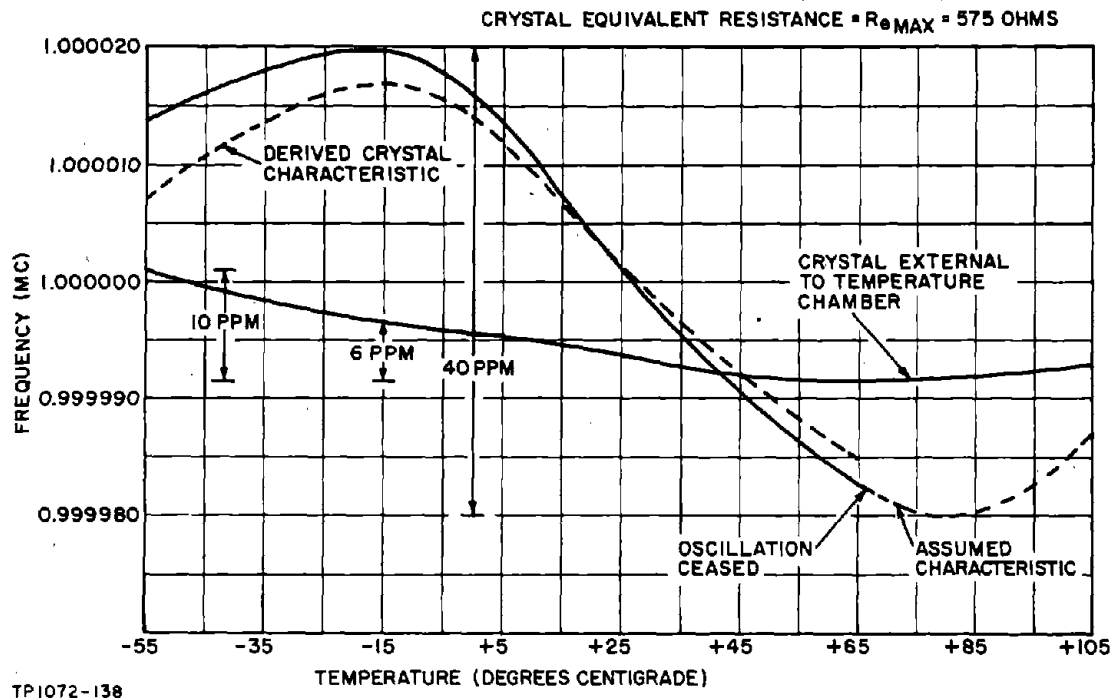


Figure 9-10. Crystal Temperature Curves, 1-MC Triode Pierce Oscillator

9-25. 5-MC Triode (12AT7) Isolating Resistor Pierce Oscillator Evaluation Data

<u>CRYSTAL UNITS</u> <u>(CR-18A/U)</u>	<u>PARALLEL RESONANT</u> <u>FREQUENCY (MC)</u>	<u>R_e (ohms)</u>
(1)	4.999956	16
(2)	4.999924	15
(3)	4.999973	24
(4) (Unit (3) with 36-ohm series resistor added)	4.999952	60

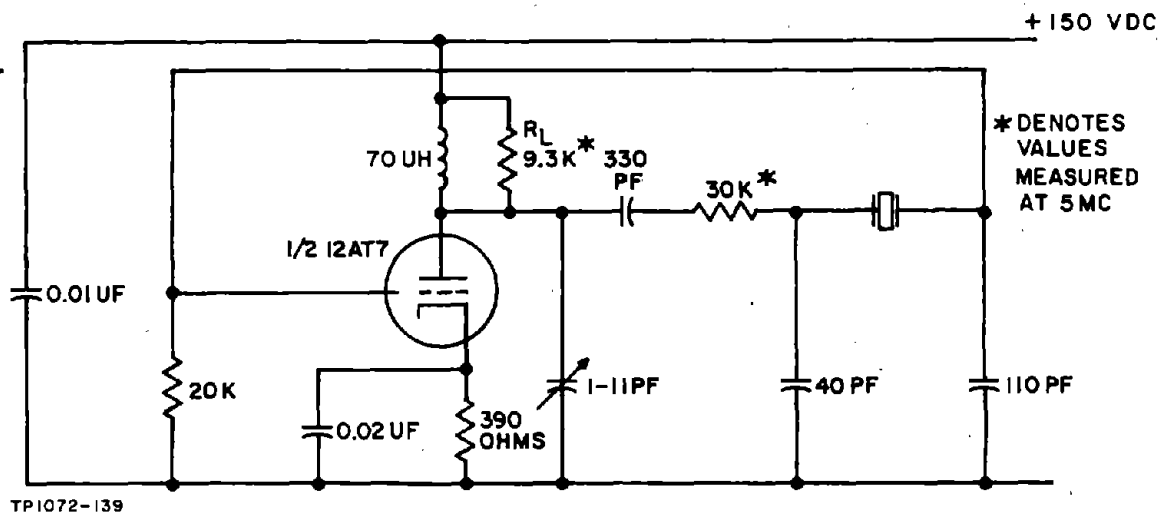


Figure 9-11. 5-MC Triode Pierce Oscillator, Schematic Diagram

Nominal $V_o = 24.5$ V Nominal Oscillator Frequency = 4.999943 MC

All Results Obtained Using Limit Crystal (No. 5)

Effect Of	Change	Test Conditions
+15% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = +10\%$ $R_L = 9.3$ K, $E_f = 6.3$ V
-20% B+ Change on Oscillator	Frequency V_o	< 1 PPM $\Delta V_o = -27\%$ $R_L = 9.3$ K, $E_f = 6.3$ V
$\pm 10\%$ Change in E_f on Oscillator	Frequency V_o	$< \pm 1$ PPM $\Delta V_o = \pm 3\%$ $R_L = 9.3$ K, $E_{bb} = 150$ V
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o	$< \pm 1$ PPM $\Delta V_o = \pm 10\%$ $E_f = 6.3$ V, $E_{bb} = 150$ V
-55°C to $+105^\circ\text{C}$ Change in T_A on Oscillator	Frequency V_o	$< \pm 11$ PPM $\Delta V_o = \pm 3\%$ $E_f = 6.3$ V, $E_{bb} = 150$ V, $R_L = 9.3$ K

Nominal $V_o = 24.5$ V Nominal Oscillator Frequency = 4.999943 MC

All Results Obtained Using Limit Crystal (No. 5) (Cont)

Effect Of	Change	Test Conditions
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test	$< \pm 2$ PPM	

Effect of Tube Changes (Crystal Unit (4))

Tube No.	Oscillator Frequency (MC)	Output Voltage
1 (Used in preceding tests)	4.999942	25
2	4.999943	23
3	4.999948	23.5
4	4.999946	24.5
5	4.999942	28
6	4.999944	25
7	4.999946	27
8	4.999950	25

Effect of Crystal Changes (Tube No. 1)

Crystal No.	Crystal Frequency (MC)	Oscillator Frequency (MC)	Error (PPM)	Output Voltage
1	4.999956	4.999970	+3	28
2	4.999924	4.999935	+2	28
3	4.999973	4.999991	+4	27
4	4.999952	4.999942	-2	24

Effect of C_T and C_S Variations

Increasing C_S by 1 PF results in a frequency change of -1 PPM
Increasing C_T by 1 PF results in a frequency change of -4 PPM

Power Output Range

57 to 100 MW

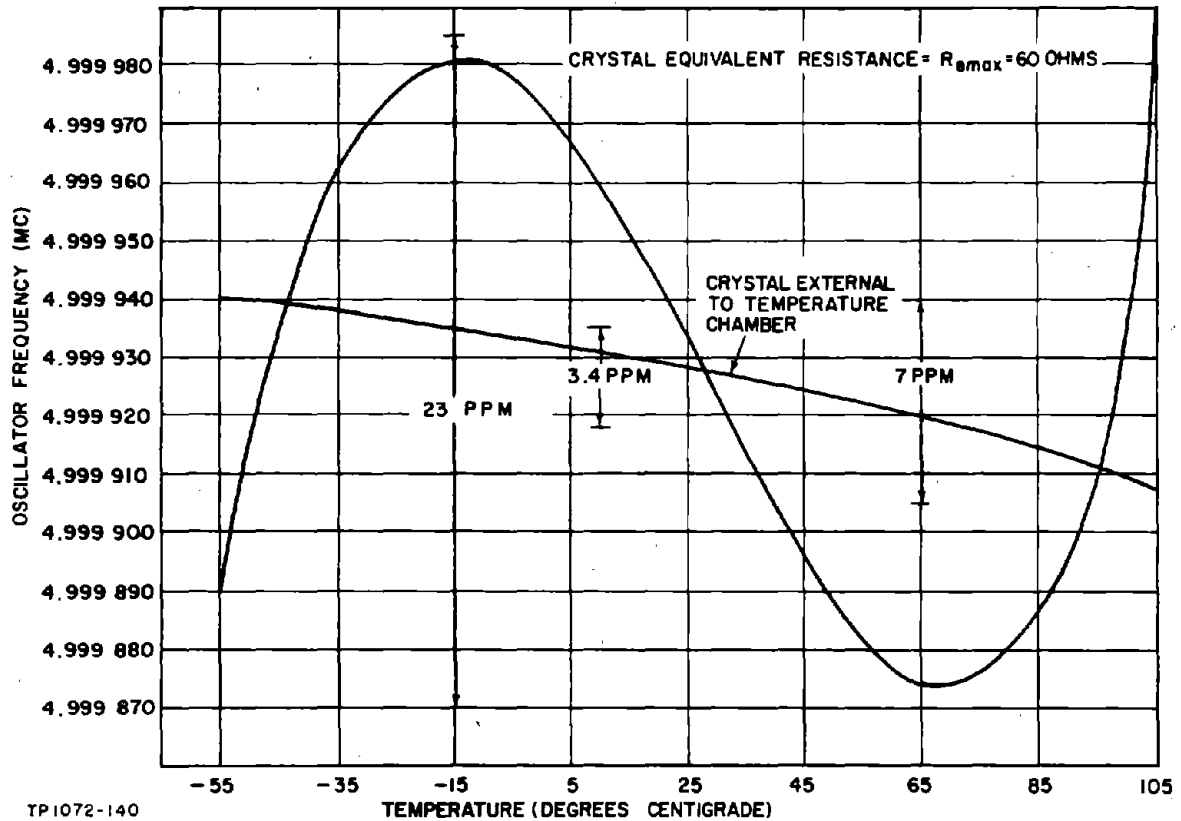


Figure 9-12. Crystal Temperature Curves, 5-MC Triode Pierce Oscillator

9-26. 20-MC Triode (6CW4) Isolating Resistor Pierce Oscillator Evaluation Data

CRYSTAL UNITS (CR-18A/U)	PARALLEL RESONANT FREQUENCY (MC)	R_e (ohms)
(1)	20.000270	7
(2)	20.000600	8
(3)	20.000400	7
(4)	20.000200	8
(5) (Unit (4) with 12-ohm series resistor added)	20.000000	20

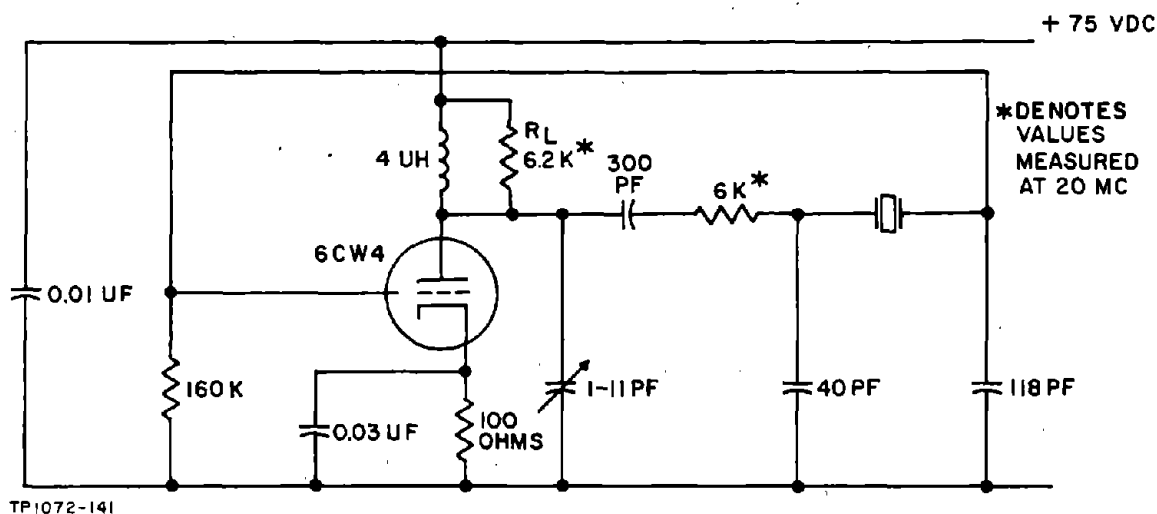


Figure 9-13. 20-MC Triode Pierce Oscillator, Schematic Diagram

Nominal $V_o = 8$ VRMS Nominal Oscillator Frequency = 19.999910 MC

All Results Obtained Using Limit Crystal (No. 5)

Effect Of	Change	Test Conditions
+15% B+ Change on Oscillator	Frequency V_o 1 PPM $\Delta V_o = +31\%$	$R_L = 6.7$ K, $E_f = 6.3$ V
-20% B+ Change on Oscillator	Frequency V_o -1.5 PPM $\Delta V_o = -44\%$	$R_L = 6.7$ K, $E_f = 6.3$ V
$\pm 10\%$ Change in E_f on Oscillator	Frequency V_o ± 1.5 PPM $\Delta V_o = \pm 6\%$	$R_L = 6.7$ K, $E_{bb} = 75$ V
$\pm 10\%$ R_L Change on Oscillator	Frequency V_o ± 1 PPM $\Delta V_o = \pm 6\%$	$E_f = 6.3$ V, $E_{bb} = 75$ V
-55°C to +105°C Change in T_A on Oscillator	Frequency V_o ± 25 PPM $\Delta V_o = \pm 9\%$	$E_f = 6.3$ V, $E_{bb} = 75$ V, $R_L = 6.3$ V

Nominal $V_o = 8$ VRMS Nominal Oscillator Frequency = 19.999910 MC

All Results Obtained Using Limit Crystal (No. 5) (Cont)

Effect Of	Change	Test Conditions
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test	± 2 PPM	

Effect of Tube Changes

Tube No.	Oscillator Frequency (MC)	Output Voltage
1 (Used in preceding tests)	19.999910	8
2	19.999918	9.6
3	19.999900	8.8
4	19.999910	8.6
5	19.999925	8.6
Total frequency spread is less than 2 PPM.		

Effect of Crystal Changes (Tube No. 1)

Crystal No.	Crystal Frequency (MC)	Oscillator Frequency (MC)	Error (PPM)	Output Voltage
1	20.000270	20.000230	-2	10 V
2	20.000600	20.000610	1	10 V
3	20.000400	20.000350	-2.5	10 V
4	20.000200	20.000200	0	10 V
5	20.000000	19.999910	-4.5	8 V

Effect of C_T and C_S Variations

Increasing C_S by 1 PF results in frequency change of -1.5 PPM
Increasing C_T by 1 PF results in frequency change of -14 PPM

Power Output Range

10 MW to 20 MW

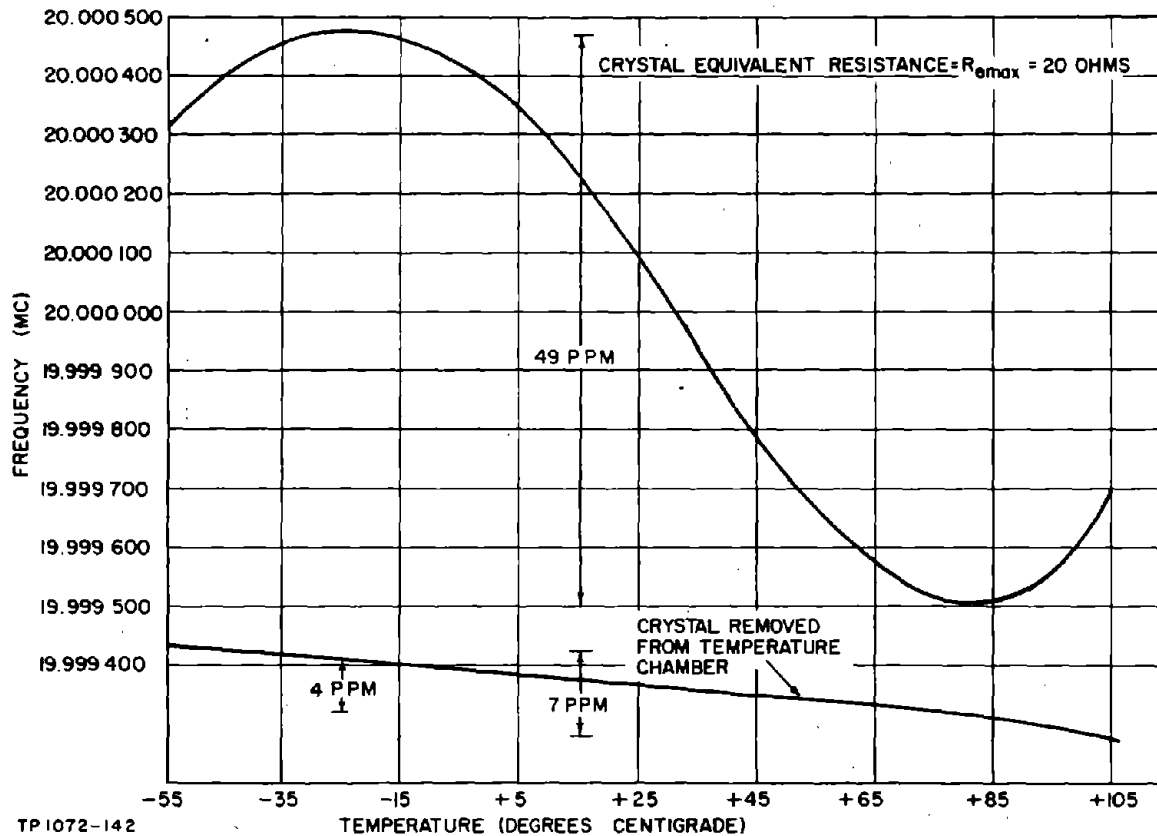


Figure 9-14. Crystal Temperature Curves, 20-MC Triode Pierce Oscillator

9-27. 20-MC Triode (6CW4) Isolating Resistor Pierce Oscillator Evaluation Data (Modified Approach)

CRYSTAL UNITS (CR-18A/U)	PARALLEL RESONANT FREQUENCY (MC)	R_e (ohms)
(1)	20.000270	7
(2)	20.000600	8
(3)	20.000400	7
(4)	20.000200	8
(5) (Unit (4) with 12-ohm series resistor added)	20.000000	20

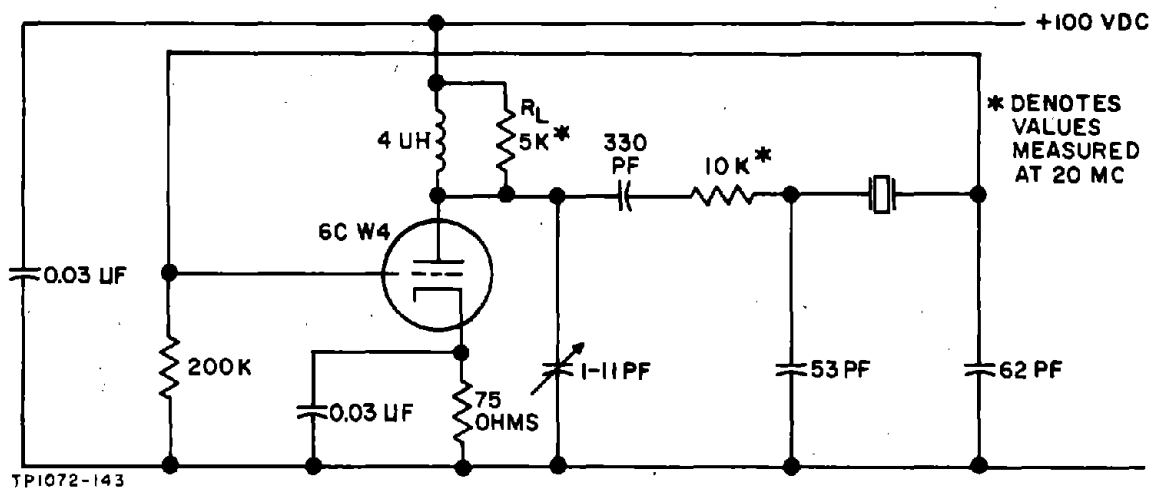


Figure 9-15. 20-MC Triode Pierce Oscillator, Schematic Diagram

Nominal $V_o = 11.4$ VRMS Nominal Oscillator Frequency = 19.999890 MC

All Results Obtained Using Limit Crystal (No. 5)

Effect Of	Change	Test Conditions
+15% B+ Change on Oscillator	Frequency V_o <1 PPM $\Delta V_o = +29\%$	$R_L = 5.1$ K, $E_f = 6.3$ V
-20% B+ Change on Oscillator	Frequency V_o -1 PPM $\Delta V_o = -45\%$	$R_L = 5.1$ K, $E_f = 6.3$ V
$\pm 10\%$ Change in E_f on Oscillator	Frequency V_o < ± 1 PPM $\Delta V_o = \pm 3.5\%$	$R_L = 5.1$ K, $E_{bb} = 100$ V
$\pm 10\%$ Change in R_L on Oscillator	Frequency V_o < ± 1 PPM $\Delta V_o = \pm 3.5\%$	$E_f = 6.3$ V, $E_{bb} = 100$ V
-55°C to +105°C Change in TA on Oscillator	Frequency V_o ± 24 PPM $\Delta V_o = \pm 11\%$	$E_f = 6.3$ V, $E_{bb} = 100$ V, $R_L = 5.1$ K

Nominal $V_0 = 11.4$ VRMS Nominal Oscillator Frequency = 19.999890 MC

All Results Obtained Using Limit Crystal (No. 5) (Cont)

Effect Of	Change	Test Conditions
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test	$< \pm 2$ PPM	

Changes of Tube Changes

Tube No.	Oscillator Frequency (MC)	Output Voltage
1 (Used in preceding tests)	19.999890	11.4
2	19.999880	13.4
3	19.999890	12.2
4	19.999890	12
5	19.999890	11.8

Effect of Crystal Changes (Tube No. 1)

Crystal No.	Crystal Frequency (MC)	Oscillator Frequency (MC)	Error (PPM)	Output Voltage
1	20.000270	20.000260	-1	12.9
2	20.000600	20.000630	+2	12.9
3	20.000400	20.000400	0	13
4	20.000200	20.000230	+2	12.9
5	20.000000	19.999890	-6	11.4

Effect of C_T and C_S Variations

Increasing C_S by 1 PF results in frequency change of -4 PPM
Increasing C_T by 1 PF results in frequency change of -11 PPM

Power Output Range

26 to 45 MW

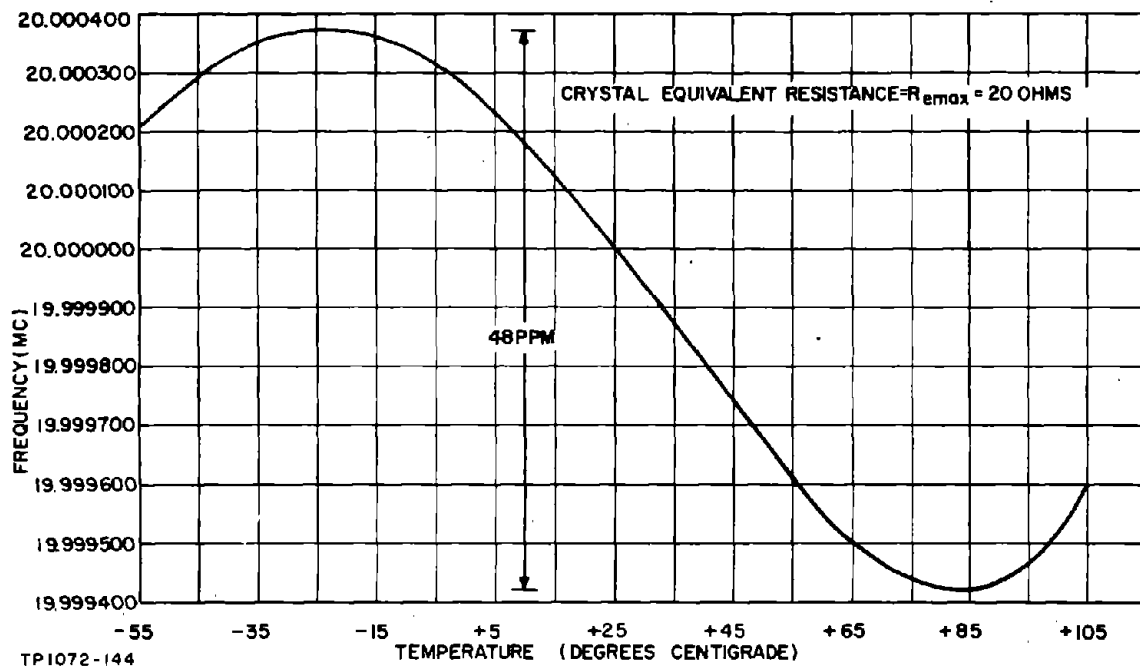


Figure 9-16. Crystal Temperature Curves, 20-MC Triode Pierce Oscillator

9-28. 20-MC Triode (12AT7) Isolating Resistor Pierce Oscillator Evaluation Data (Modified Approach)

CRYSTAL UNITS (CR-18A/U)	PARALLEL RESONANT FREQUENCY (MC)	R_e (ohms)
(1)	20.000270	7
(2)	20.000600	8
(3)	20.000400	7
(4)	20.000200	8
(5) (Unit (4) with 12-ohm series resistor added)	20.000000	20

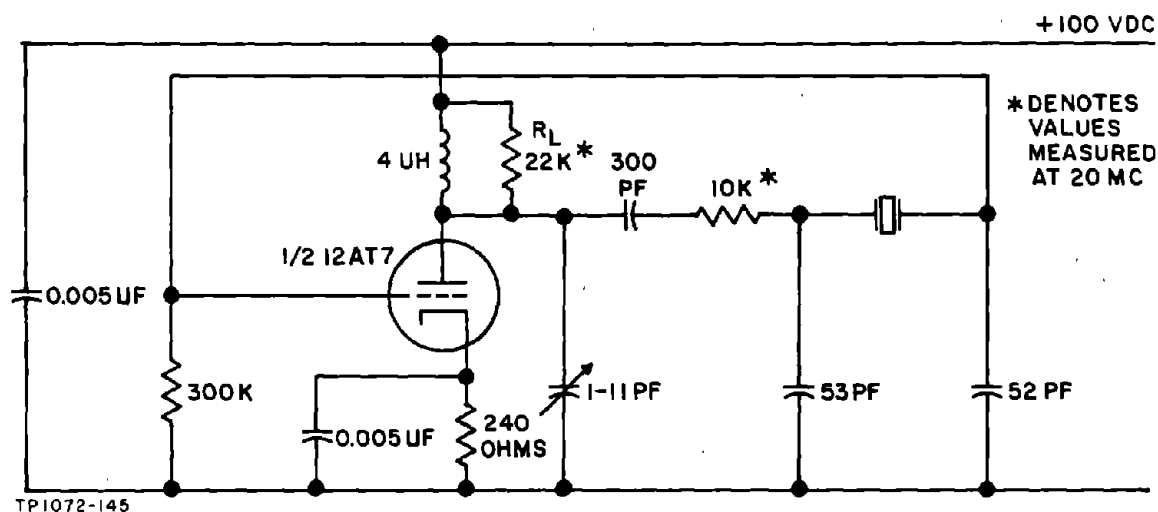


Figure 9-17. 20-MC Triode Pierce Oscillator (12AT7), Schematic Diagram

Nominal $V_o = 10.5$ VRMS Nominal Oscillator Frequency = 19.999990 MC

All Results Obtained Using Limit Crystal (No. 4)

Effect Of	Change	Test Conditions
+15% B+ Change on Oscillator } Frequency V_o	< 1 PPM $\Delta V_o = +26\%$	$R_L = 23$ K, $E_f = 6.3$ V
-20% B+ Change on Oscillator } Frequency V_o	-1 PPM $\Delta V_o = -35\%$	$R_L = 23$ K, $E_f = 6.3$ V
$\pm 10\%$ Change in E_f on Oscillator } Frequency V_o	< 1 PPM $\Delta V_o < \pm 2\%$	$R_L = 23$ K, $E_{bb} = 100$ V
$\pm 10\%$ Change in R_L on Oscillator } Frequency V_o	± 1 PPM $\Delta V_o = \pm 3\%$	$E_f = 6.3$ V, $E_{bb} = 100$ V
-55°C to +105°C Change in T_A on Oscillator } Frequency V_o	± 26 PPM $\Delta V_o = \pm 11\%$	$E_f = 6.3$ V, $E_{bb} = 100$ V, $R_L = 23$ K

Nominal $V_o = 10.5$ VRMS Nominal Oscillator Frequency = 19.999990 MC

All Results Obtained Using Limit Crystal (No. 4) (Cont)

Effect Of	Change	Test Conditions
Contribution of Oscillator Circuit to Frequency Deviations in Temperature Test	± 3 PPM	

Effect of Tube Changes

Tube No.	Oscillator Frequency (MC)	Output Voltage
1 (Used in preceding tests)	19.999990	10.3
2	20.000000	9
3	19.999990	9.2
4	19.999960	10
5	20.000030	12.8
6	19.999960	10.1
7	19.999960	11.1
8	19.999990	10.3

Effect of Crystal Changes (Tube No. 1)

Crystal No.	Crystal Frequency (MC)	Oscillator Frequency (MC)	Error (PPM)	Output Voltage
1	20.000270	20.000260	-1	12.8
2	20.000600	20.000630	+2	12.9
3	20.000400	20.000400	0	12.9
4	20.000200	20.000200	0	12.8
5	20.000000	19.999990	-1	10.2

Effect of C_T and C_S Variations

Increasing C_S by 1 PF results in a frequency change of -4 PPM
Increasing C_T by 1 PF results in a frequency change of -11 PPM

Power Output Range

3.5 to 10 MW

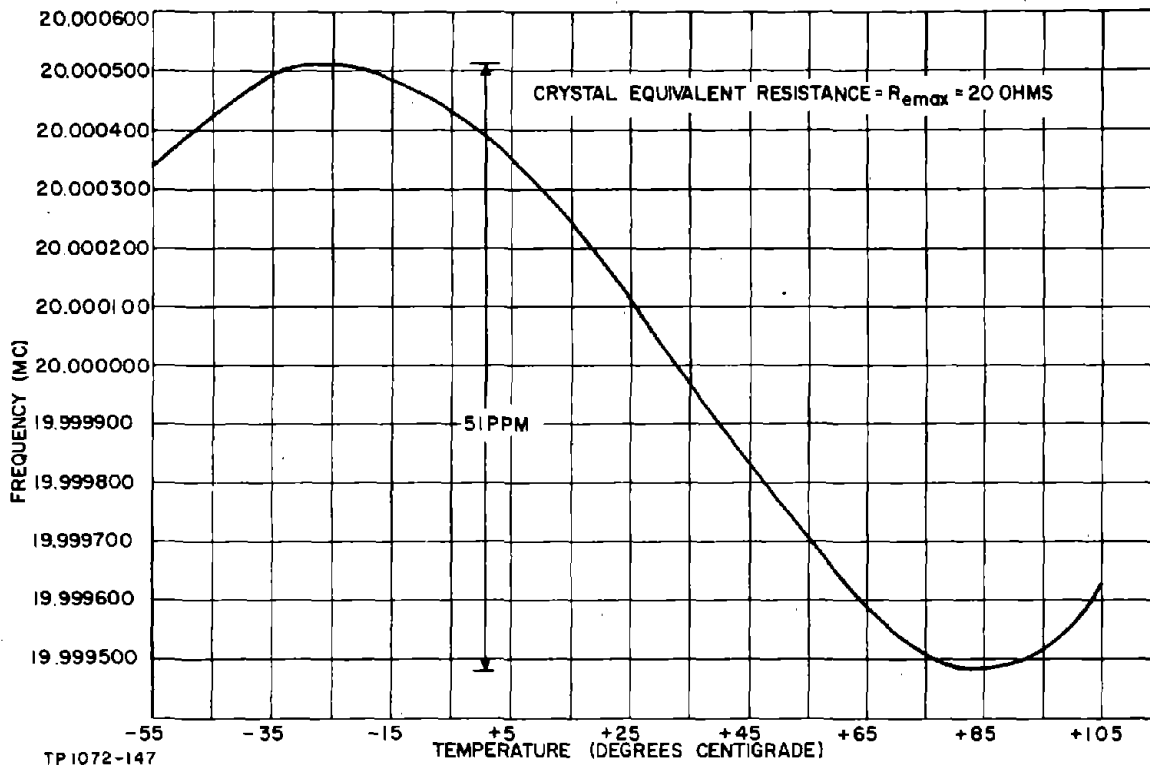


Figure 9-18. Crystal Temperature Curves, 20-MC Triode Pierce Oscillator

9-29. DESIGN NOTES FOR TRIODE ANTI-RESONANCE OSCILLATORS, 1 KC TO 500 KC

No design work has been carried out in this frequency range, and the following discussion should be regarded as a suggestion of how the design process devised for the 0.8 to 20 MC range may be adapted to produce suitable designs at these frequencies.

The major characteristics of the military type anti-resonance crystal units applicable to the 16 to 500 KC range are given in Table 9-8. There are no military anti-resonance crystal units below 16 KC, but crystal units having characteristics similar to those presented in Table 9-8 for the range from 1 to 16 KC are obtainable.

Comparison of the characteristics presented in Table 9-8 with those previously given for the 0.8 to 20 MC range shows that in the 90 to 500 KC range the crystal unit impedance levels are increased by roughly one order of magnitude and the dissipation rating reduced by a factor of 5 relative to those in the 0.8 to 2 MC range. And below 100 KC the relative impedance levels are increased by about 2 orders of magnitude while the dissipation rating is comparably

TABLE 9-8. ANTI-RESONANCE CRYSTAL UNIT CHARACTERISTICS,
1 KC TO 500 KC

Frequency Range (KC)	Temperature Range (°C)	Overall Frequency Tolerance (±%)	Equivalent Resistance (Kilohms)	Dissipation Rating (MW)	Loading Capacitance (PF)	Crystal Unit Type	Crystal Holder Type
1 - 16	-40 to +70	0.015	200	0.01	20	---	---
16 - 100	-40 to +70	0.012	110 to 90	0.1	20	CR-38A/U	HC-13/U
*80 - 200	-40 to +70	0.01	5 to 6	2	32	CR-15B/U	HC-21/U
90 - 250	-40 to +70	0.02	5 and 5.5	2	20	CR-37A/U	HC-13/U
*80 - 860	-30 to +75	0.01	3	2	45	CR-43/U	HC-16/U
*200 - 500	-40 to +85	0.01	5.3 to 8.5	2	20	CR-46A/U	HC-6/U
200 - 500	-55 to +90	0.015	5.3 to 8.5	2	20	CR-63A/U	HC-6/U
TEMPERATURE CONTROLLED TYPES							
*80 - 200	70 to 80	0.002	5 to 6	2	32	CR-29A/U	HC-21/U
90 - 250	70 to 80	0.003	4.5 and 5	2	32	CR-42A/U	HC-13/U
200 - 500	70 to 80	0.002	5.3 to 8.5	2	20	CR-47A/U	HC-6/U
*500	80 to 90	0.001	3	0.5	32	CR-57/U	HC-6/U

*Special Applications

decreased. This in general means that the permissible π network input signal voltage is comparable to that applying in the 0.8 to 20 MC range.

The range of values of the ratio $X_e/R_{e \max}$ is also comparable to that applying in the 0.8 to 20 MC range, although somewhat wider, ranging from 40 to 2.5 in the frequency range of 1 to 16 KC (assuming $C_L = 20$ PF), 4.5 to 0.89 in the 16 to 100 KC range, and 18 to 1.9 in the 90 to 500 KC range.

Judging from scattered measurements, the sensitivity of the anti-resonance frequency to percentage changes in the loading capacitance value is decreased by a factor of 2. This, and the wider crystal unit tolerance, should permit some relaxation of the permissible relative values of C_M and C_S , all other things being equal. However, the relative value of C_L to C_{pg} is decreased, which will tend to increase the effect of changes in C_M , offsetting these beneficial effects. It appears likely, therefore, that the π network proportional values used in the basic approach in the 0.8 to 20 MC range are probably suitable in this range.

In certain frequency ranges the ratio of $X_e/R_{e \max}$ is less than 3, and the feedback network input resistance then falls below $1.33 R$, in the worst case approaching a value of R . When $X_e/R_{e \max}$ is less than 3, the oscillator load should therefore be calculated using this latter value.

The π network will also frequently be operating under output phase angle limiting conditions rather than crystal unit loading conditions, and calculations of R_g based on both Equations (9-16) and (9-18) should be made and the highest value selected.

Three partial design calculations are presented for what appear to be the worst conditions. These indicate that amplifier voltage gains of 24 to 28 will be necessary at these particular frequencies. In the two lower frequency examples, it is also necessary to limit the plate signal voltage to approximately 7 VRMS for a worst-case design. It should be practicable to achieve both the voltage gain and required limiting by using, say, a 12AT7 tube at a DC plate voltage level of perhaps 80 V and at a current level of less than 1 MA.

The following calculations are in similar form to those presented for the basic design approach. Values of K_A , R_L , and X_{CT} are derived from the plots of Figure 9-7.

9-30. 15.99 KC Partial Design Calculation

$$R_{e \max} = 200 \text{ K}, P_{\text{CMAX}} = 10 \text{ UW}, C_L = 20 \text{ PF}$$

$$X_e = 500 \text{ K}, \frac{X_e}{R_{e \max}} = 2.5$$

For

$$X_{CS} = 0.2 X_e = 100 \text{ K}, C_S = 100 \text{ PF}, \frac{X_{\text{Leff}}}{R_{e \max}} = 2,$$

$$X_{\text{Leff}} = 400 \text{ K}, K_A = 4.3, A_V^{-1} = 17.2, R = 2.5 \text{ MEGO},$$

$$R_{FB} \approx 2.5 \text{ MEGO}, V_{\text{omax}} = 10.7 \text{ VRMS}, V'_{\text{omax}} = 7 \text{ VRMS},$$

$$R_g \geq 600 \text{ K}, X_{CT} = 375 \text{ K}, C_T = 27 \text{ PF}, \text{Required } G_V = 24.$$

9-31. 80 KC Partial Design Calculation

$$R_{e \max} = 100 \text{ K}, P_{\text{CMAX}} = 0.1 \text{ MW}, C_L = 20 \text{ PF}, X_e = 100 \text{ K},$$

$$\frac{X_e}{R_{e \max}} = 1.$$

For

$$X_{CS} = 0.2 X_e = 20 \text{ K}, C_S = 100 \text{ PF}, \frac{X_{\text{Leff}}}{R_{e \max}} = 0.8,$$

$$X_{\text{Leff}} = 80 \text{ K}, K_A = 4.9, A_V^{-1} = 19.6, R = 160 \text{ K}, R_{FB} \approx 160 \text{ K},$$

$$V_{\text{omax}} = 9.8 \text{ VRMS}, V'_{\text{omax}} \approx 7 \text{ VRMS}, R_g \geq 120 \text{ K}, X_{CT} = 51 \text{ K},$$

$$C_T = 39 \text{ PF}, \text{Required } G_V = 28.$$

9-32. 500 KC Partial Design Calculation

$$R_{e \max} = 8.5 \text{ K}, P_{\text{CMAX}} = 2 \text{ MW}, C_L = 20 \text{ PF}, X_e = 16 \text{ K},$$

$$\frac{X_e}{R_{e \max}} = 1.9.$$

For

$$X_{CS} = 0.2 X_e = 3.2 \text{ K}, \frac{X_{\text{Leff}}}{R_{e \max}} = 1.5, X_{\text{Leff}} = 12.8 \text{ K}, K_A = 4.4,$$

$$A_V^{-1} = 17.6, R = 60 \text{ K}, R_{FB} \approx 60 \text{ K}, V_{\text{omax}} = 23 \text{ VRMS},$$

$$V'_{\text{omax}} \approx 14 \text{ VRMS}, R_g \geq 19 \text{ K}, X_{CT} = 11.6 \text{ K}, C_T = 28 \text{ PF},$$

$$\text{Required } G_V = 25.$$

SECTION 10
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